

UNIT - II

LOGIC FAMILIES

DIGITAL IC SPECIFICATION TERMINOLOGY :

The digital IC nomenclature and terminology is fairly standardized. Most useful specifications are

1) Threshold Voltage :

The threshold voltage is defined as that voltage at the i/p of a gate which causes a change in the state of the output waveform one logic level to the other.

2) Propagation delay :

A pulse through a gate takes a certain amount of time to propagate from input to output. This interval of time is known as the propagation delay of the gate.

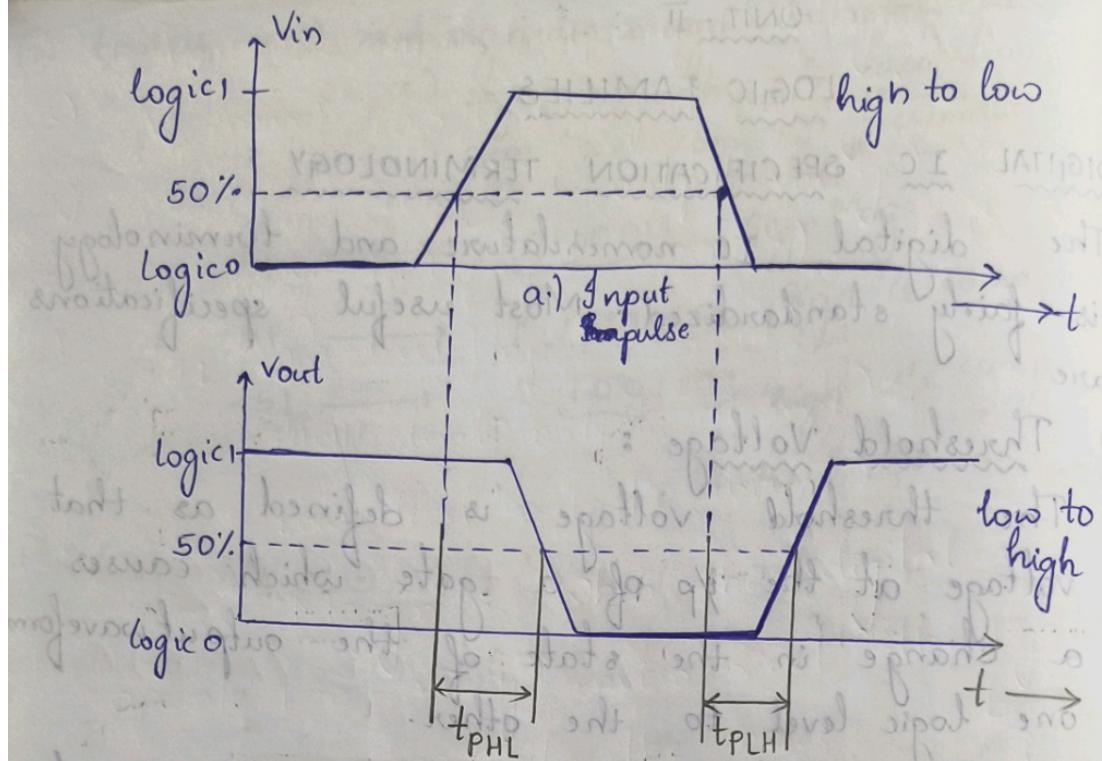
If it is the average transition delay time t_{pd} ,

expressed by,

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$

where t_{PLH} is the signal delay time when the i/p goes from a logic 0 to a logic 1 state & t_{PHL} is the signal delay time when the output goes from a logic 1 to a logic 0 state.

: NI-HAF



a) Output Pulse

Power dissipation: $P_D = V_{cc} \times I_{cc(\text{avg})}/n$

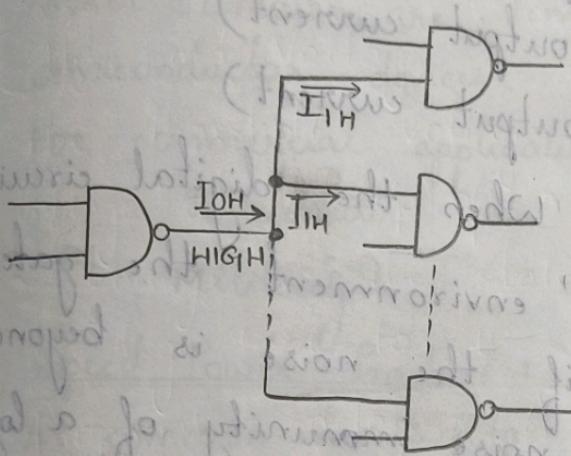
Every logic gate draws some current from the supply for its operation. The current drawn in HIGH state is different from that drawn in LOW state. The power dissipation, P_D , of a logic gate is the power required by the gate to operate with 50% duty cycle at a specified frequency and is expressed in milliwatts. This means that 1 and 0 periods of the output are equal. The power dissipation of a gate is given by $P_D = V_{cc} \times I_{cc(\text{avg})}/n$

FAN-IN:

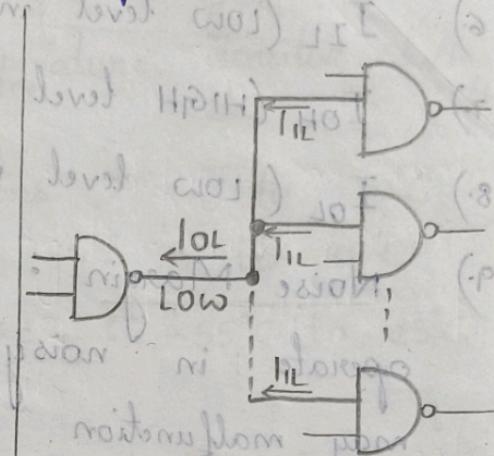
The fan-in of a logic gate is defined as the number of inputs that the

gate is designed to handle.

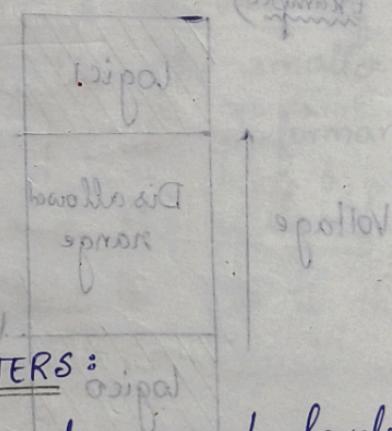
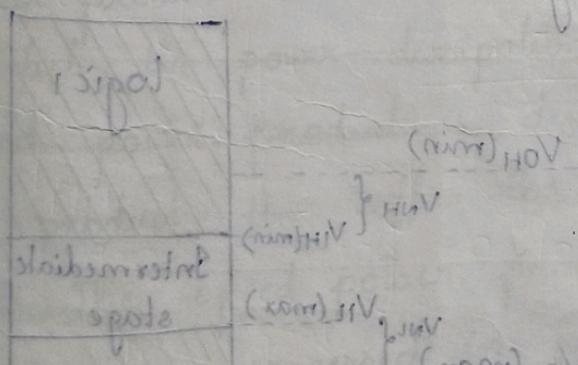
Fan-out: The fan-out of a logic gate is defined as the maximum number of standard loads that the output of the gate can drive without impairing its normal operation.



a) Current sourcing in HIGH state



b.) Current sinking in LOW state



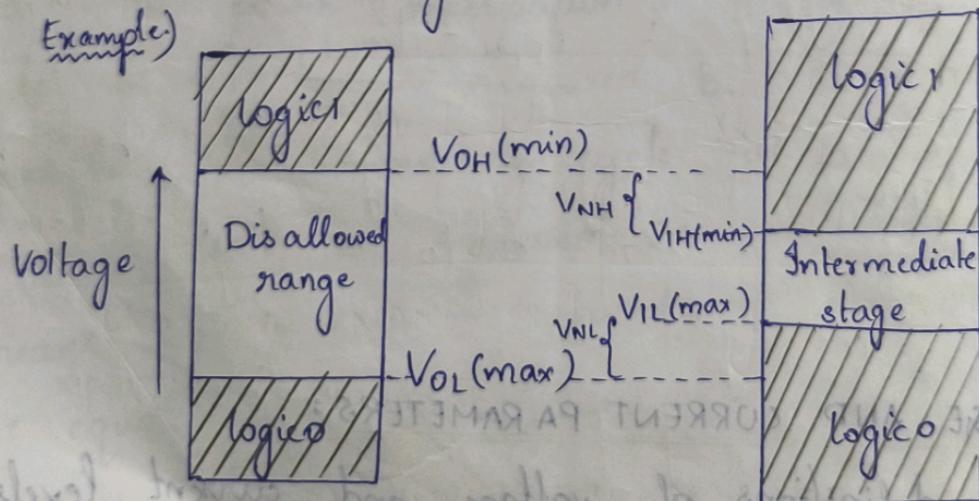
VOLTAGE AND CURRENT PARAMETERS:

The definitions of voltage and current levels corresponding to the logic 0 and logic 1 states are as follows.

- 1) $V_{IH} \text{ (min)}$ (HIGH level input voltage)

- 2.) $V_{OH}(\text{min})$ (HIGH level output voltage)
- 3.) $V_{IL}(\text{max})$ (low level input voltage)
- 4.) $V_{OL}(\text{max})$ (low level output voltage)
- 5.) I_{IH} (HIGH level input current)
- 6.) I_{IL} (low level input current)
- 7.) I_{OH} (HIGH level output current)
- 8.) I_{OL} (low level output current)
- 9.) Noise Margin : When the digital circuits operate in noisy environment the gates may malfunction if the noise is beyond certain limits. The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise voltages at its inputs. A quantitative measure of noise immunity is called noise margin.

Example)



a) Output Voltage ranges b) Input voltage ranges.

Fig) DC Noise Margins

10) High state noise margin (NM_H) is

$$V_{NH} = V_{OH(\min)} - V_{IH(\min)}$$

Low state noise margin (NM_L) is

$$V_{NL} = V_{IL(\max)} - V_{OL(\max)}$$

10.) Operating Temperatures : The IC gates and other circuits are temperature sensitive being semiconductor devices.

For commercial applications : 0 to 70°C

Industrial : 0 to 85°C

Military : -55°C to 125°C

11.) Speed Power Product :

A common means for measuring & comparing the overall performance of an IC family is the speed power product, which is obtained by multiplying the gate propagation delay by the gate power dissipation. A low value of speed power product is desirable. The smaller the product, the power dissipation. A low value of speed power product is desirable. The smaller the speed power product is, the better the overall performance.

The speed power product has units of

The speed power product is expressed in picojoules. It is the energy & is expressed in picojoules. It is the figure of merit of an IC family. Suppose an IC family has an avg propagation delay of 10ns and an avg power dissipation of 5mW,

the speed power product is

$$10\text{ns} \times 5\text{mW} = 50 \times 10^{-12} \text{ watt-sec} = 50 \text{ pico Joule (pJ)}$$

Comparison of logic families

Logic family	Propagation delay time (ns)	Power dissipation per gate (mw)	Noise margin (V)	Fan-in	Fan-out	Cost
Transistor-transistor logic (TTL)	9	10	0.4	8	10	low
Emitter Coupled logic (ECL)	1	50	0.25	5	10	High
MOS	50	0.1	1.5	10	10	low
CMOS	< 50	0.01	5	10	50	low
Injection Integrated logic III	1	0.1	0.35	5	8	Very low

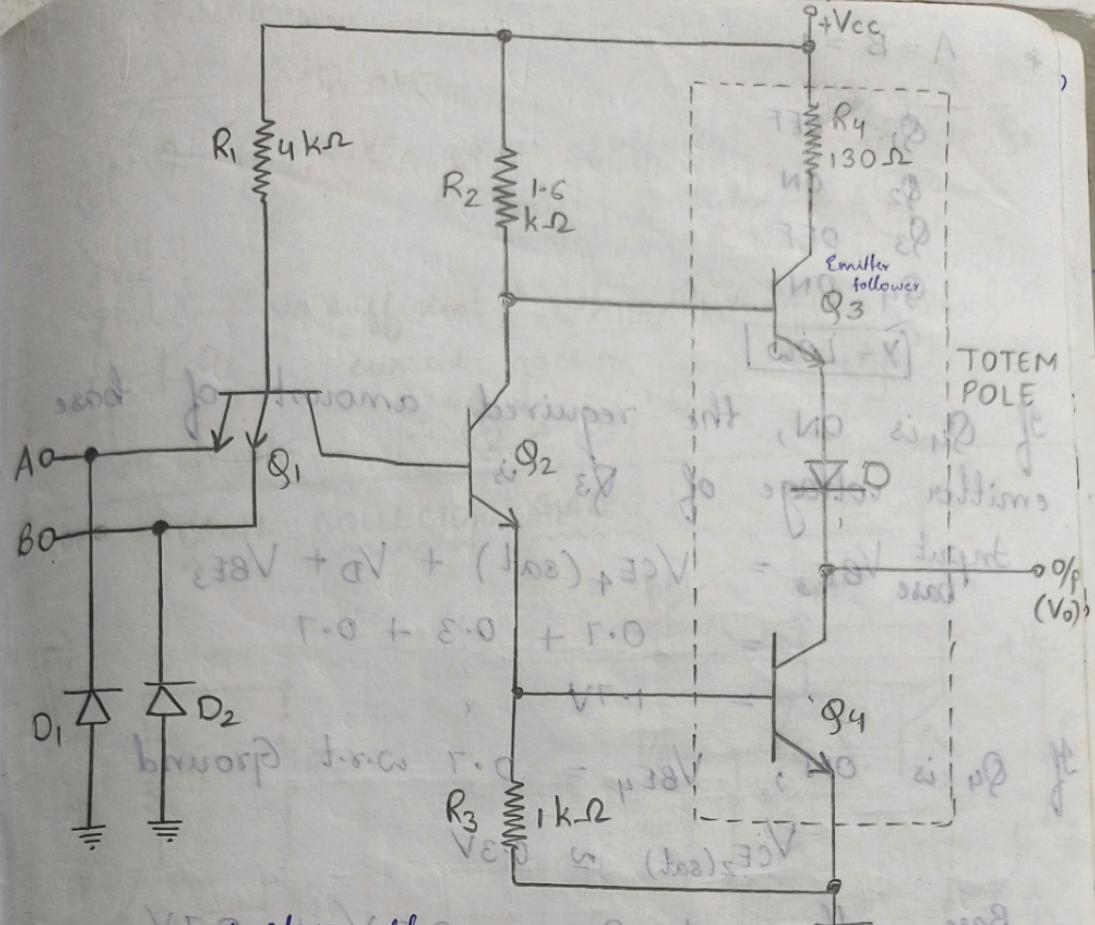
CMOS is the current trending VLSI [small size, cost low, fan-in high, fan-out high]

Q.) Design a NAND Gate using Transistor-transistor logic?

V. Imp. TWO INPUT TTL NAND GATE

Wires for making inputs & output

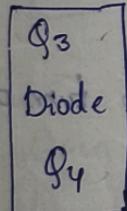
W_{out} = 2ⁿ - 1 where n = W_{in} × 2ⁿ⁻¹



$Q_1 \Rightarrow$ Multi Emitter = eq to npn

$Q_2 \Rightarrow$ Phase Splitter =

$D \Rightarrow$ prevents Q_3 and Q_4 conducts simultaneously



Q_3 & Q_4 \Rightarrow Totem pole connection

$Q_3 \Rightarrow$ Emitter follower

D_1 & $D_2 \Rightarrow$ Protects Q_1 from negative spikes.

* for A B

0	0	Q_1 is ON
1	0	Q_2 is OFF
		Q_4 is OFF

Q_3 ON
O/P is HIGH

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

$$* A = B = 1$$

Q_1 OFF

Q_2 ON

Q_3 OFF

Q_4 ON

$[Y = \text{LOW}]$

If Q_4 is ON, the required amount of base emitter voltage of Q_3 is

$$\begin{aligned} \text{Input base } V_{B1/B2/B3} &= V_{CE4(\text{sat})} + V_D + V_{BE3} \\ &= 0.7 + 0.3 + 0.7 \\ &= 1.7V \end{aligned}$$

If Q_4 is ON, $V_{BE4} = 0.7$ w.r.t Ground

$$V_{CE2(\text{sat})} \approx 0.3V$$

$$\text{Base voltage at } Q_3 = 0.3V + 0.7V$$

OPERATION:

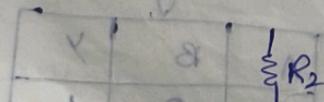
For $\{0, 0\}$ combination

Q_1 transistor ON

So $V_{BC1} \Rightarrow$ is not sufficient to turn off Q_2

* Now Q_2 OFF state \Rightarrow

i.e., for Q_3 only, total current goes

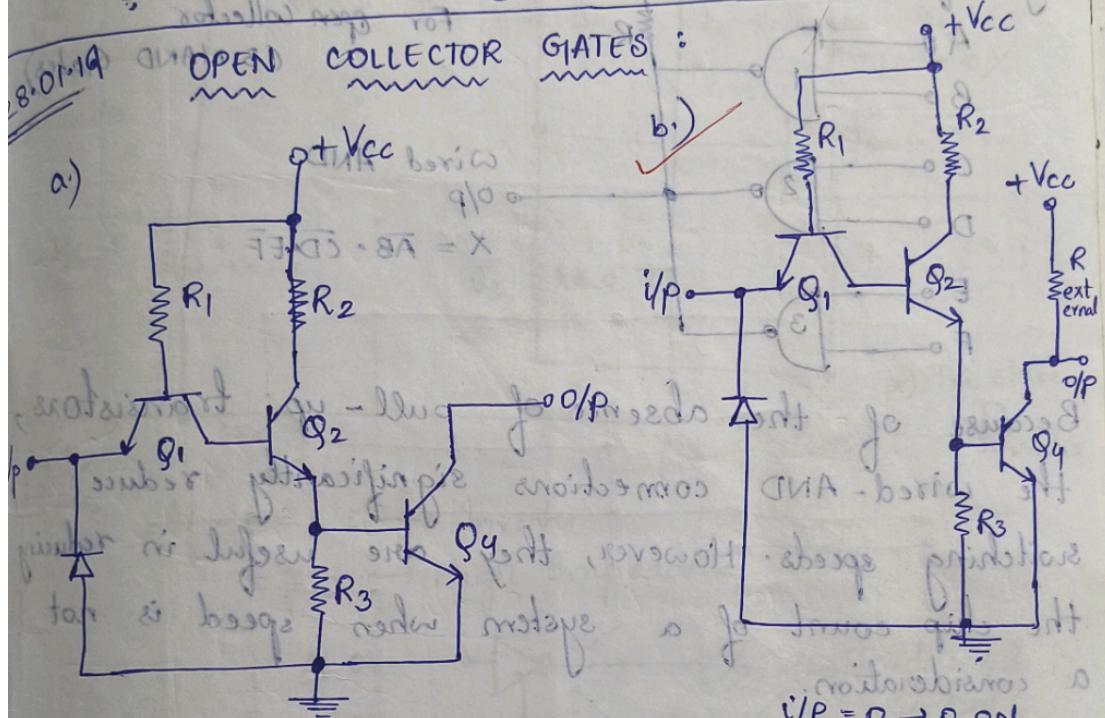
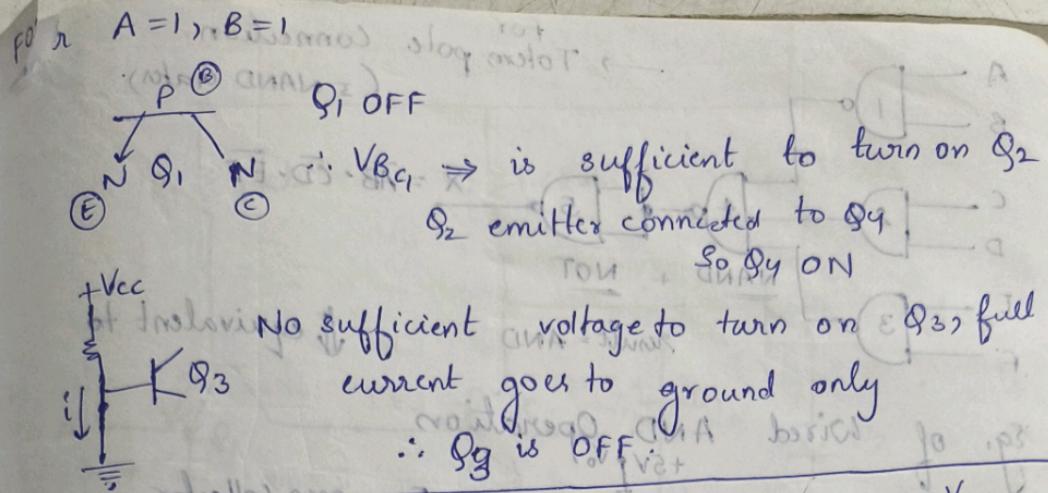


Q_3 ON

Now Q_3 ON \rightarrow i.e., diode ON

Q_2 off means
 Q_4 also off

Q_4 OFF



a) Open Collector inverter

b) External : external pulloff resistor to ground

i/p = 0 → Q1 ON
 not getting suff voltage
 blw B, C terminals

of Q_1, Q_2, Q_3

Q_2 OFF

Q_3 OFF

$O/P = 1$

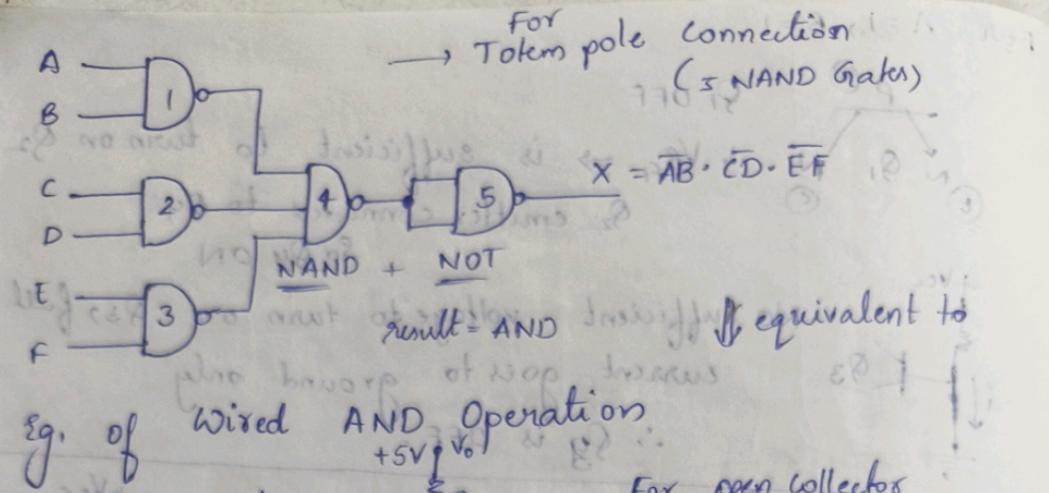
$i/p = 1 \rightarrow O/P = 0$

Advantages of Open Collector Inverter

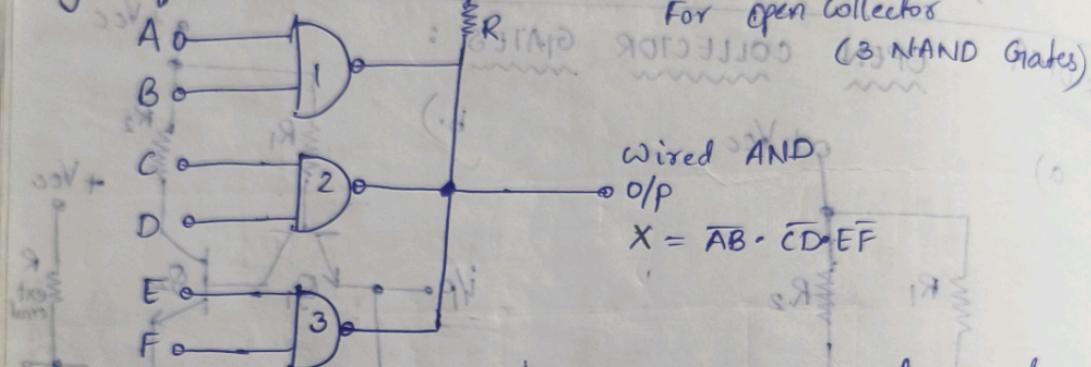
TTL Configuration :

: JFET (state - 8) state - inverter

Advantages of JFET Inverter



Eg. of Wired AND Operation



Because of the absence of pull-up transistors, the wired-AND connections significantly reduce switching speeds. However, they are useful in reducing the chip count of a system when speed is not a consideration.

TTL : ① Totem pole Connection

② Open Collector

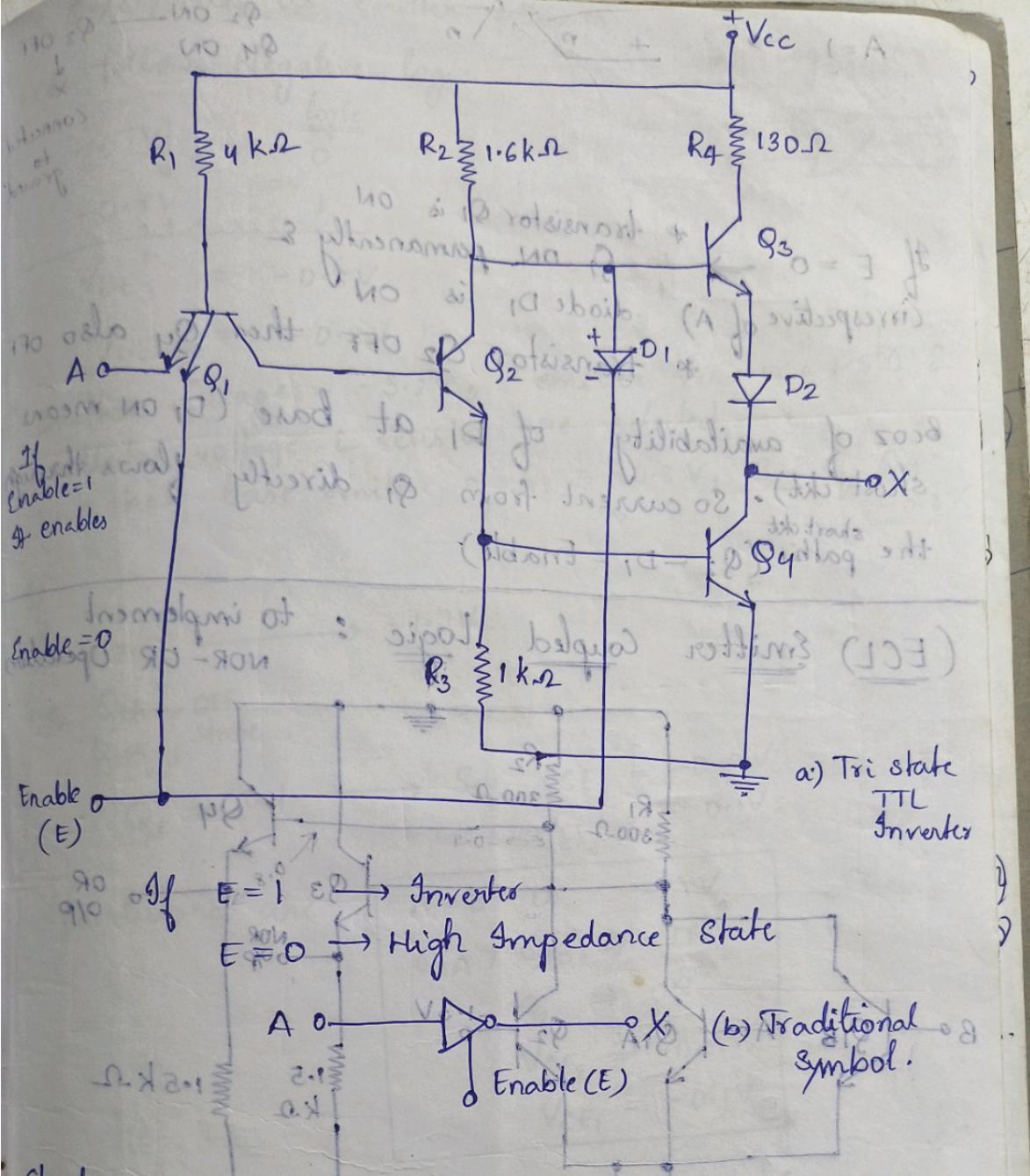
③ Tristate Output

Z (High Impedance State)

O/p is connected neither to +Ve nor ground

Tri-state (3-state) TTL :

The third TTL configuration is the tri-state configuration



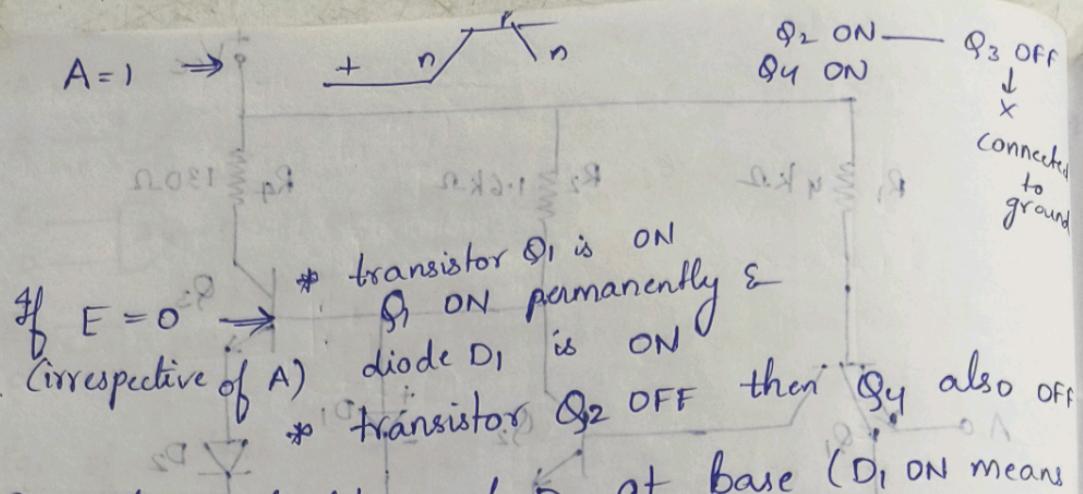
Check

$$\text{if } AE = 0 \text{ } \Rightarrow \text{ } A = 0$$

If $E = 1$ means +ve voltage $\Rightarrow D_1$ OFF state (means +ve connected to -ve of D_1)

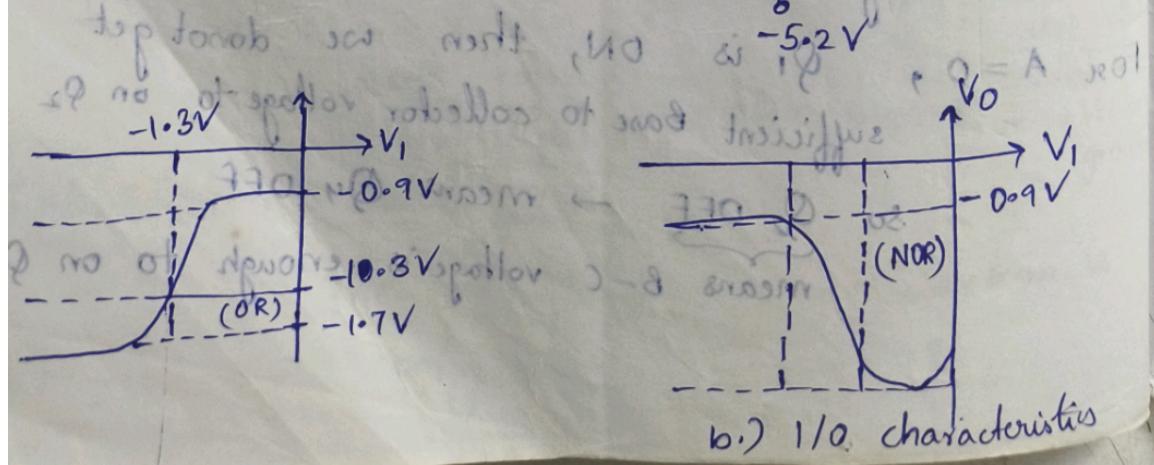
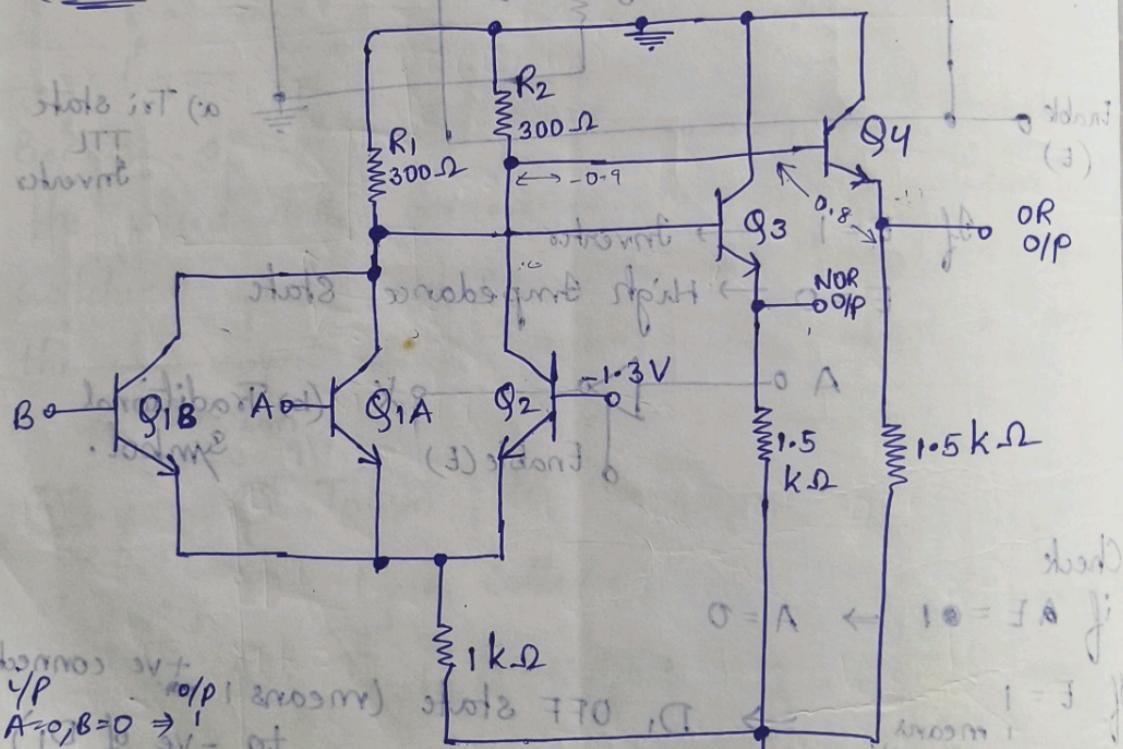
For $A = 0$, Q_1 is ON, then we don't get sufficient base to collector voltage to turn Q_2 ON.

so Q_2 OFF \rightarrow means Q_4 OFF
means B-C voltage is enough to turn Q_3 ON.

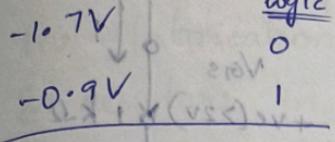


Bcoz of availability of D_1 at base (D_1 ON means short ckt). So current from Q_1 directly flows through the short ckt path (Q_2 - D_1 - Enable)

(ECL) Emitter Coupled Logic : to implement NOR-OR Operations



ECAL follows Negative logic



$$V_{BE3} = -0.8V$$

$$V_{BE4} = -0.8V$$

① Emitter voltage = $-5.2V$, emitter resistor = $1.5k\Omega$
collector voltage & resistor are selected such that base emitter of $Q_3 = -0.8V$, B-E of $Q_4 = -0.8V$

If
 $A=B=0 \rightarrow -1.7V$

i.e., $Q_1A \} \text{OFF}$
 $Q_1B \} \text{state}$

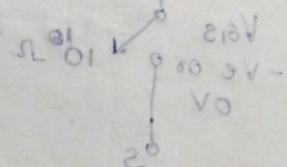
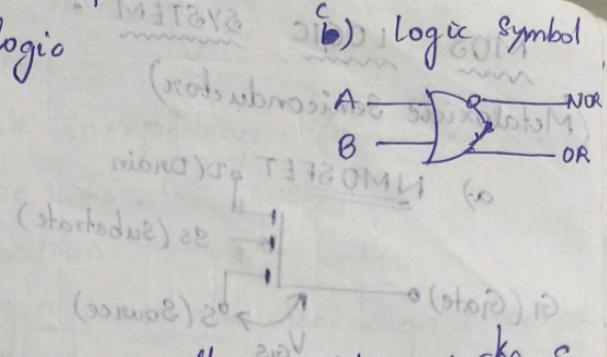
$Q_2 \Rightarrow \text{ON} \rightarrow \text{So } V_{CE2} = -0.9V$
 $V_{CE1} = -0.1V$

∴ Conditions are

$A=B=0$	$-1.7V$	\rightarrow	$(\text{state } 1)$
$Q_1A, Q_1B \Rightarrow \text{OFF}$			
$Q_2 \Rightarrow \text{ON}$			
$V_{CE2} = -0.9V$			
$V_{CE1} = -0.1V$			

For $A=0, B=1 \} \rightarrow$
 $A=1.2V, B=0 \} \rightarrow$
 $A=1, B=1 \} \rightarrow$
 V_O

$Q_1B, Q_1A \text{ off}$
 $Q_2 \text{ ON}$



$$V_{CE2} = -0.9V$$

$$V_{CE1} = -0.1V$$

\rightarrow

$Q_1A/Q_1B \Rightarrow \text{ON}$	$-1.7V$	\rightarrow	$(\text{state } 0)$
$Q_2 \Rightarrow \text{OFF}$			
$V_{CE1} = -0.9V$			
$V_{CE2} = -0.1V$			

30.01.19

MOS LOGIC : Advantages:

1. Circuit is simpler.
2. For fabrication - inexpensive. (Since no diodes & resistors in the IC, less cost)
3. Less power dissipation.
4. Better noise margin (unwanted noise signal mixed with the input)
5. High Fan-Out. (means the capability of the o/p to drive other o/p) ~~No load~~ ~~is able to drive~~
6. It requires much less chip area.
7. Greater Package density.

Disadvantages:

1. Operating speed is low compared with TTL, ECL.

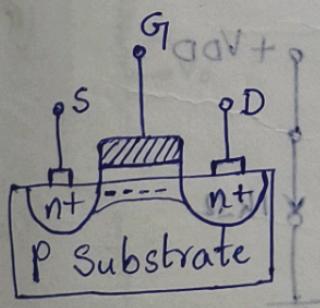
Types of MOSFET: No resistance in short circuit

1. N-type MOSFET / (N MOS)
2. P-type MOSFET / (PMOS)

Ex

NMOS

For PMOS
Gate \rightarrow -ve
Drain \rightarrow -ve



① $G_1 = +$ Voltage

(Apply +ve voltage to Gate then all minority carriers go to P substrate.)

② Apply +ve voltage to drain then electron flow from n+ to n+

flow from n+ to n+ $ddV+$ \rightarrow n^+ \rightarrow n^+

③ channel rigid formed by electrons

when Gate is +ve, $+V_{DD}$ - not split

transistor ON

i.e., switch is closed

When Gate is -ve, transistor off

No channel formation

Device is OFF state

20M9 107

PMOSFET Symbol:

nen
G1 = -ve

The diagram shows a circuit with two transistors. The top terminal of the NMOS transistor (labeled 'NK2') is connected to the output node. The bottom terminal of the NMOS transistor is connected to the drain of the PMOS transistor (labeled 'PK'). The source of the PMOS transistor is connected to ground. The gate of the PMOS transistor is labeled 'G2' and its drain is connected to the top terminal of the NMOS transistor. The top terminal of the NMOS transistor is labeled '+VDD'. The bottom terminal of the NMOS transistor is connected to ground. The entire circuit is enclosed in a box with the label 'inverter' written below it.

when $G_1 = +ve$

$$R = 10^{10} \Omega$$

Conclusion:

For NMOS:

$G_1 = 0$ OFF

$G_1 = 1$ ON

($I_{DS} = 0$)

For PMOS:

$I_{DS} = A$

(170 nA)

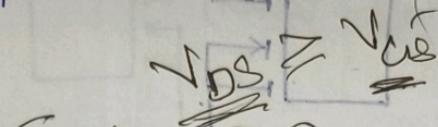
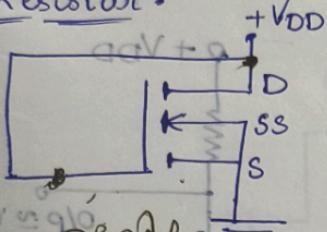
(state)

$G_1 = 0$ ON

$G_1 = 1$ OFF

($V_{GS} = 0$)

Resistor:



Saturation

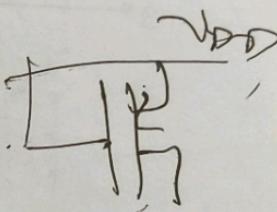
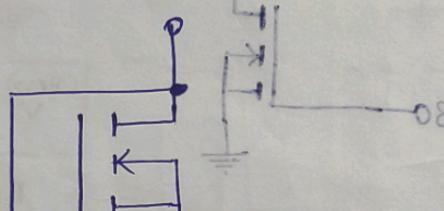
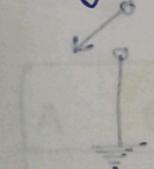
Device $\rightarrow Y_D \approx V_{DS}$

$Y_D = \frac{W}{L} \cdot \mu_0 \cdot V_{DS}$

$Y_D = \frac{W}{L} \cdot \mu_0 \cdot (V_{GS} + V_T)$

$Y_D = \frac{W}{L} \cdot \mu_0 \cdot V_{DS}$

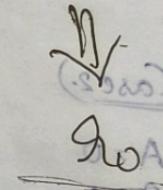
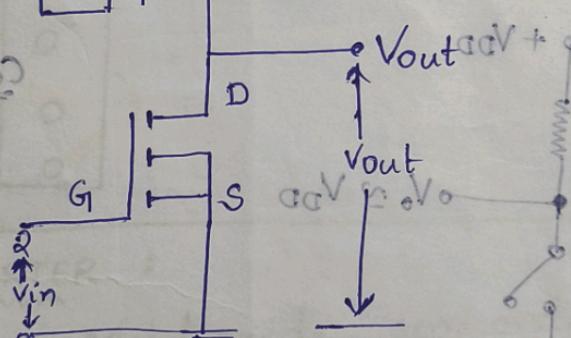
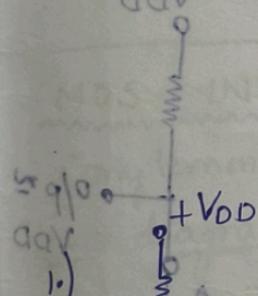
Q1) Design an inverter using NMOSFET.



$I = A$ ($I_{DS} = 0$)

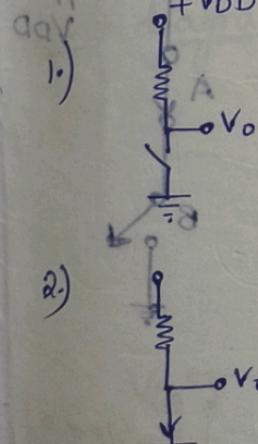
$O = B$

$+V_{DD}$

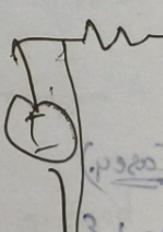
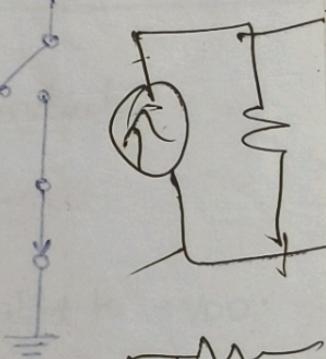


$I = A$ ($I_{DS} = 0$)

$O = B$



V_{in}	V_{out}
0	1
1	0



$I = A$

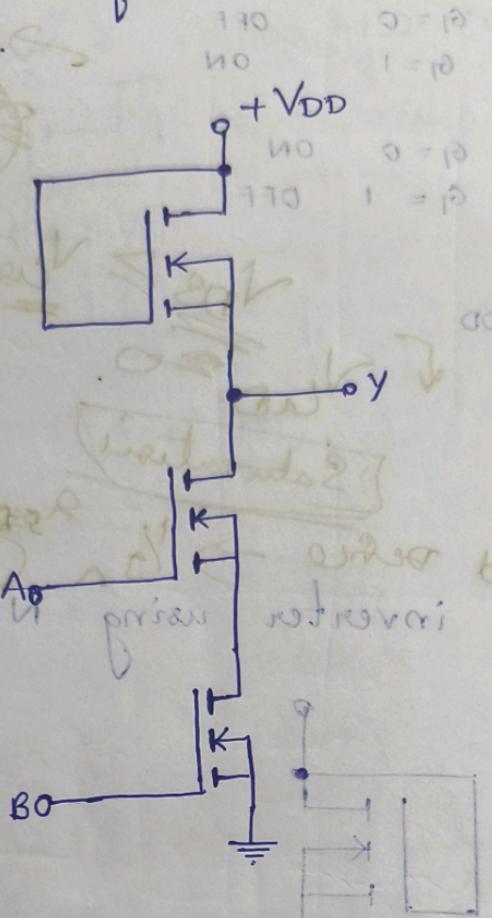
$I = B$

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① Design of logic.

Sol)

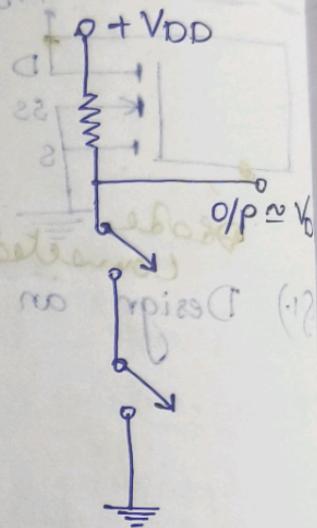
NAND₁ Gate using NMOS



Case 1.)

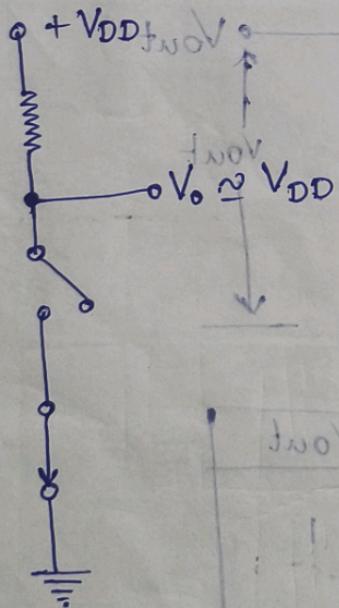
$$A = 0, B = 0$$

(both OFF state)
then

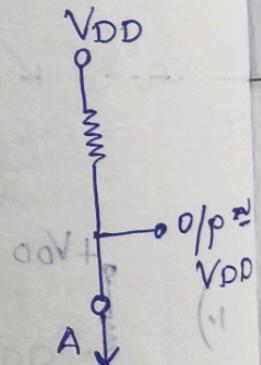


Case 2.)

$$A = 0, B = 1$$

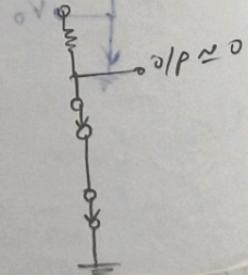
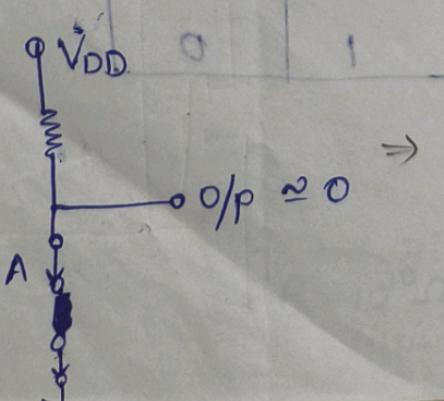


Case 3.) $A = 1, B = 0$

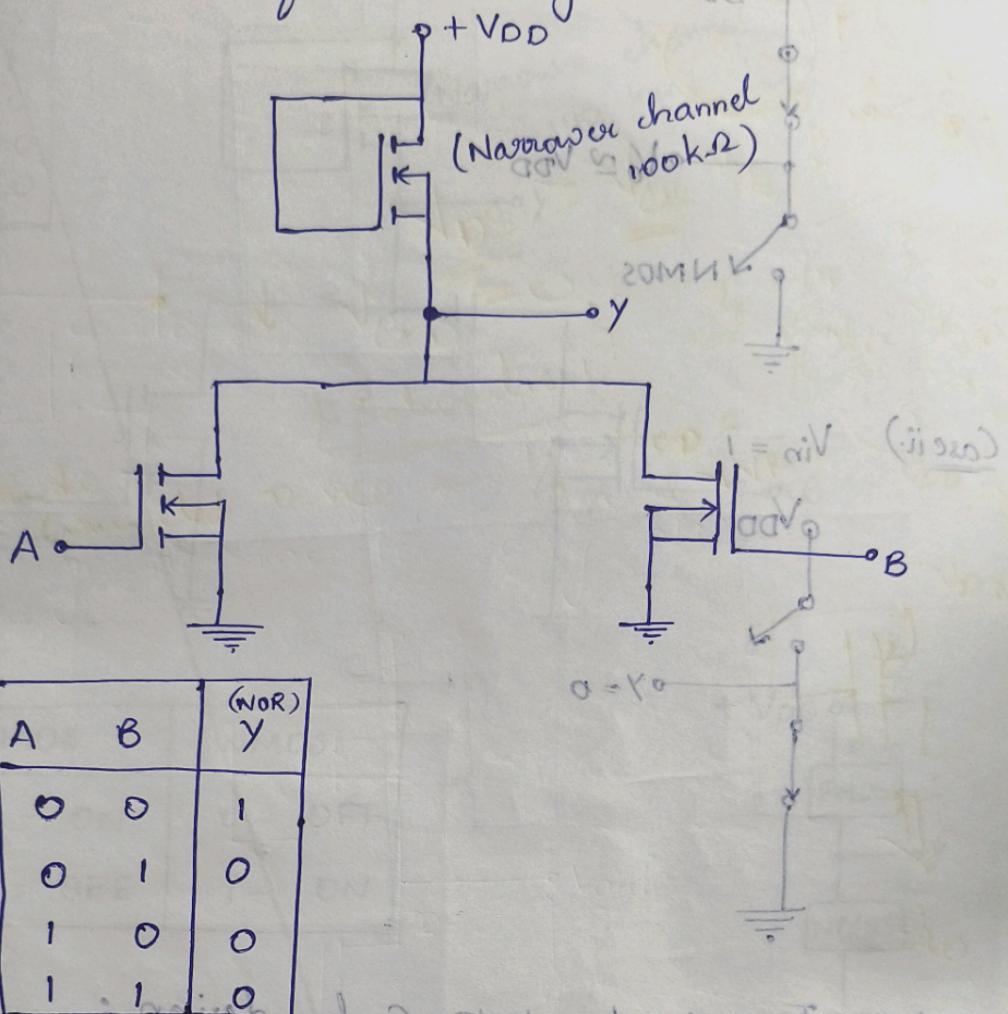


Case 4.)

$$A = 1, B = 1$$

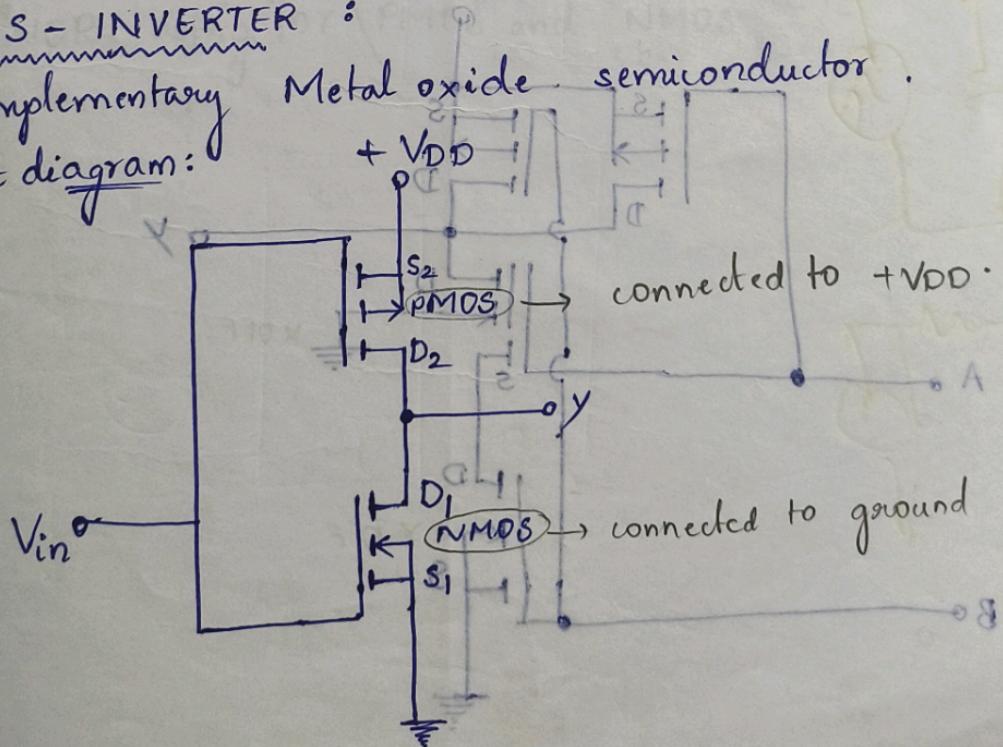


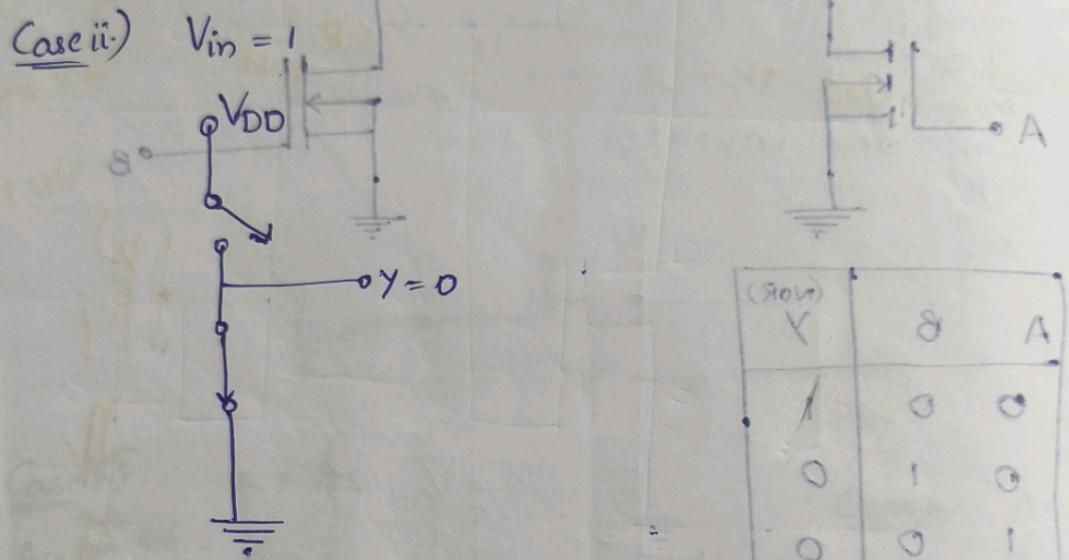
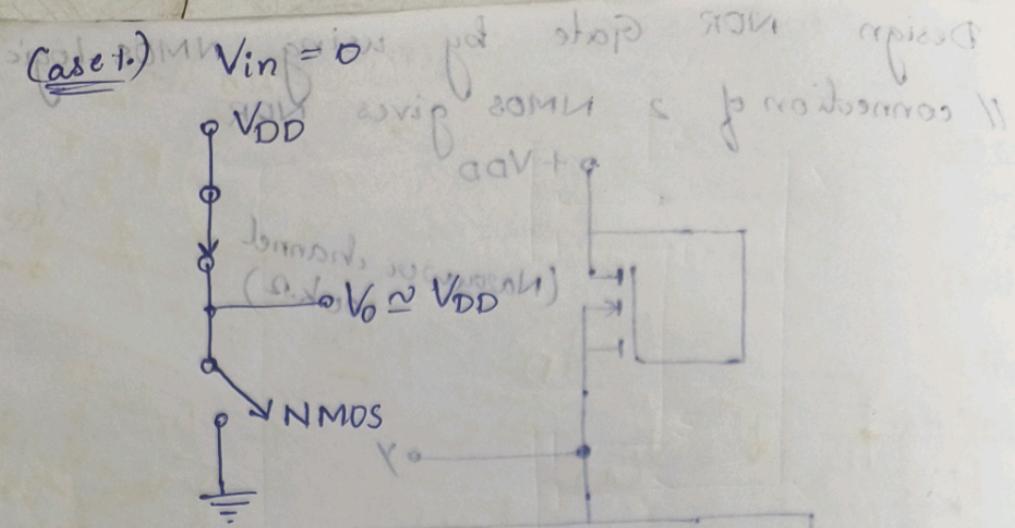
② Design NOR Gate by using NMOS Logic
// connection of 2 NMOS gives NOR



CMOS - INVERTER :

Complementary Metal oxide semiconductor .
Circuit diagram:





(Truth Table)		X	B	A
1	0	0	0	0
0	1	0	1	0
0	0	1	0	1
1	1	1	1	1

CMOS Two input NAND Gate design:

