CS 224 - Hardware Lab

Assignment - 1

Date - 21/01/2025

Group - No - 2
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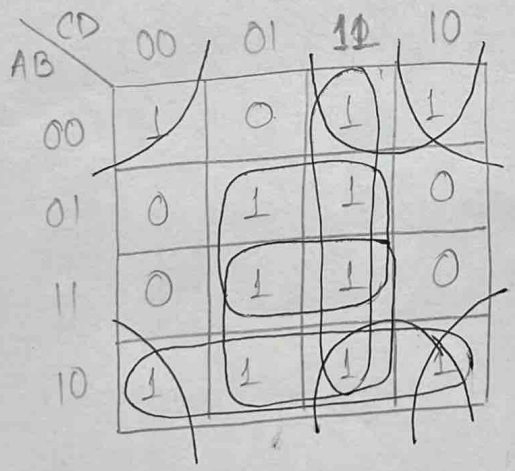
Problem Statement →

Implement the following Boolean function using Breadboard, ICs and hookup wires.

1. $F(A,B,C,D) = \sum(0,2,3,5,7,8,9,10,11,13,15)$

Sol ⇒ IC used = IC 7400 Quad 2-input NAND gates.

K-diagram for the function →



Prime implecants : $A\bar{B}$, $\bar{B}\bar{D}$, $C\bar{B}$, AD, BD, DC.

Essential prime implicants → $\bar{B}\bar{D}$, BD.

Rest are non-essentials.

Using Brute forcing,

$F(A,B,C,D)$ can be implemented as $BD + \bar{B}\bar{D} + \bar{B}A + \bar{B}C$.

Approach 1 : Approach using 10 NAND Gates.

$$F(A,B,C,D) = BD + \overline{B}\,\overline{D} + \overline{B}A + \overline{B}C$$

$$= \text{NAND}\left(B + \overline{A}\,\overline{C}, \overline{(BD + \overline{B}\,\overline{D})}\right)$$

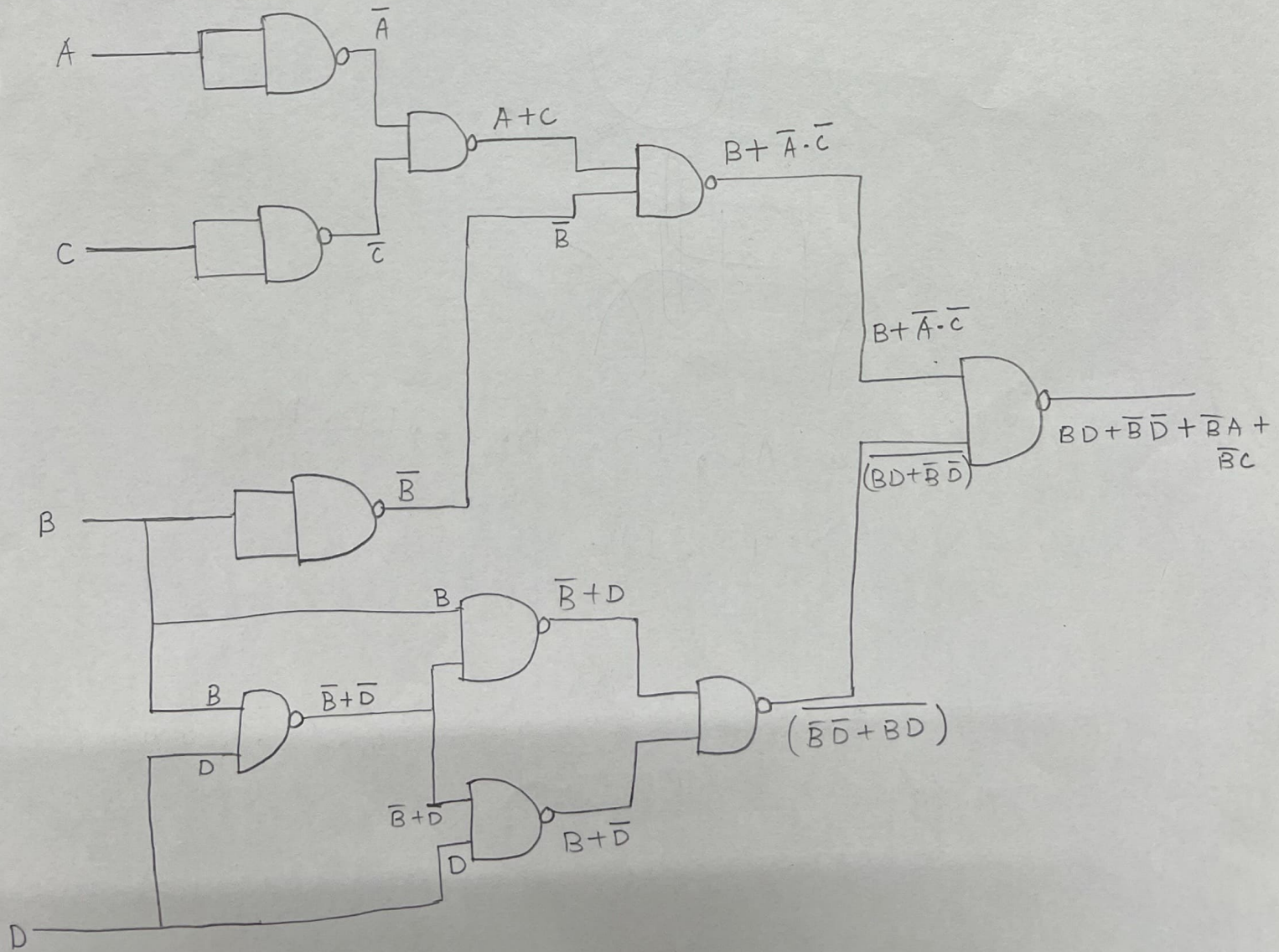
$$= \text{NAND}\left(\text{NAND}(A+C, \overline{B}), \text{NAND}(\overline{B}+D, B+\overline{D})\right)$$

$$= \text{NAND}\left(\text{NAND}(\text{NAND}(\overline{A}, \overline{C}), \overline{B}), \text{NAND}(\text{NAND}(B, \overline{B}+\overline{D}), \text{NAND}(D, \overline{B}+\overline{D}))\right)$$

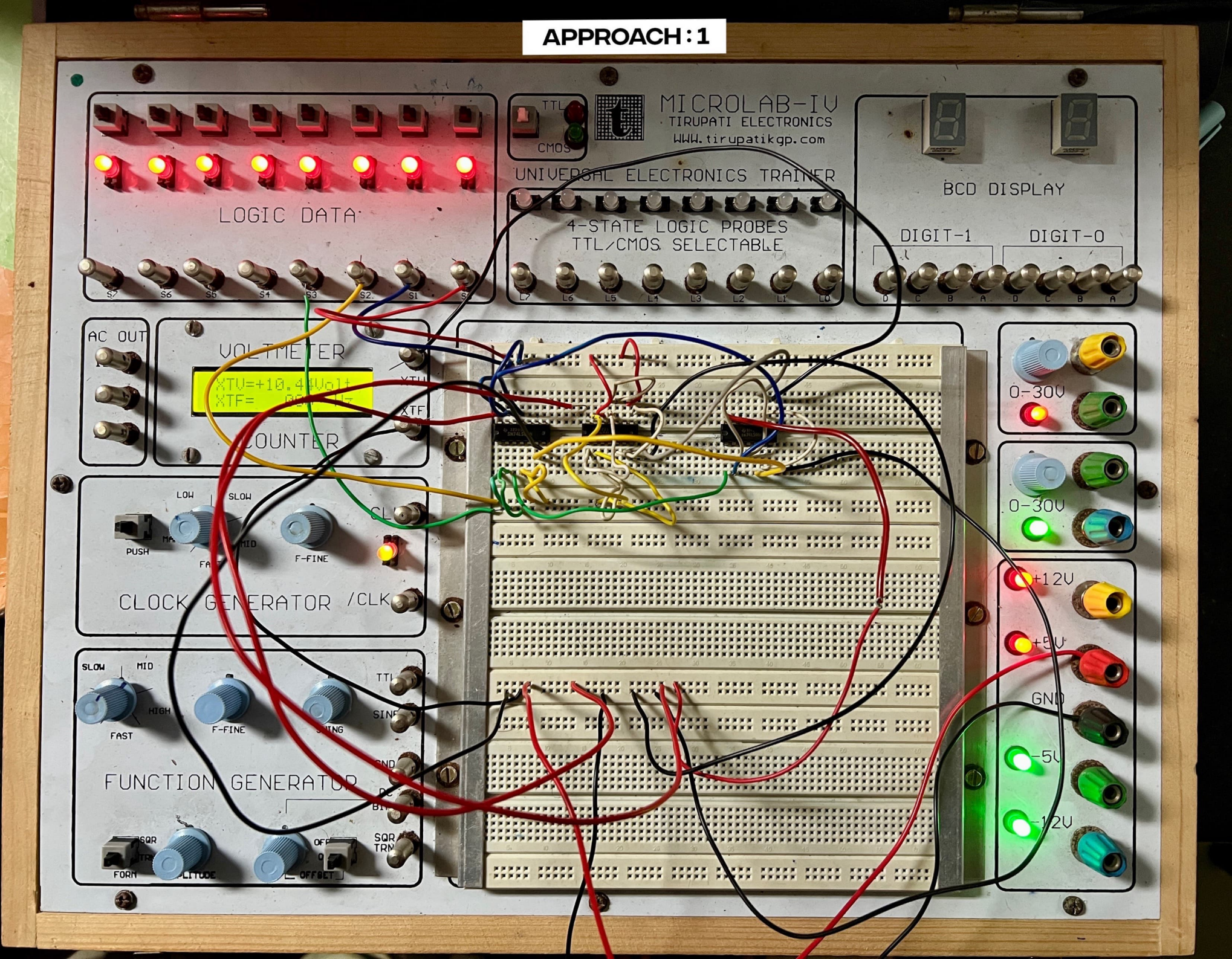
$$= \text{NAND}\left(\text{NAND}(\text{NAND}(\overline{A}, \overline{C}), \overline{B}), \text{NAND}(\text{NAND}(B, \text{NAND}(B, D)), \text{NAND}(D, \text{NAND}(B, D)))\right)$$

→ Approach is using XNOR Gate (realised with 4 NAND Gates)

Circuit Diagram →



APPROACH : 1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DIGIT-1
DIGIT-0
AC OUT
VOLTMETER
XTV=+10.44Volt
XTF=
COUNTER
XTV
XTF
PUSH
LOW
SLOW
MID
F-FINE
CLOCK GENERATOR /CLK
SLOW
MID
HIGH
FAST
F-FINE
TTL
SINE
GND
FUNCTION GENERATOR
FORM
OFFSET
SQR TRN
0-30V
0-30V
+12V
+5V
GND
-5V
-12V

Approach 2: Circuit using 9 NAND Gates

$$F(A,B,C,D) = BD + A\bar{B} + C\bar{B} + \bar{B}\bar{D}$$
$$= BD + \bar{B}(A + C + \bar{D})$$

$$NAND(\bar{A},\bar{B}) = A + B$$

$$NAND(\overline{NAND(\bar{A},\bar{B})},\bar{C}) = A + B + C$$

$$\therefore \quad A + C + \bar{D} = NAND(\overline{NAND(\bar{A},\bar{C})}, D) \quad \text{—— (1)}$$

$$NAND(X,Y) = \overline{XY} \quad \text{—— (2)}$$

$\therefore$ Using (1) & (2)

$$NAND(NAND(\overline{NAND(\bar{A},\bar{C})},D),\bar{B}) = \overline{\bar{B}(A+C+\bar{D})} \quad \text{—— (3)}$$

$$NAND(B,D) = \overline{BD} \quad \text{—— (4)}$$

$$NAND(\bar{X},\bar{Y}) = X + Y \quad \text{—— (5)}$$

Using (3), (4) & (5)

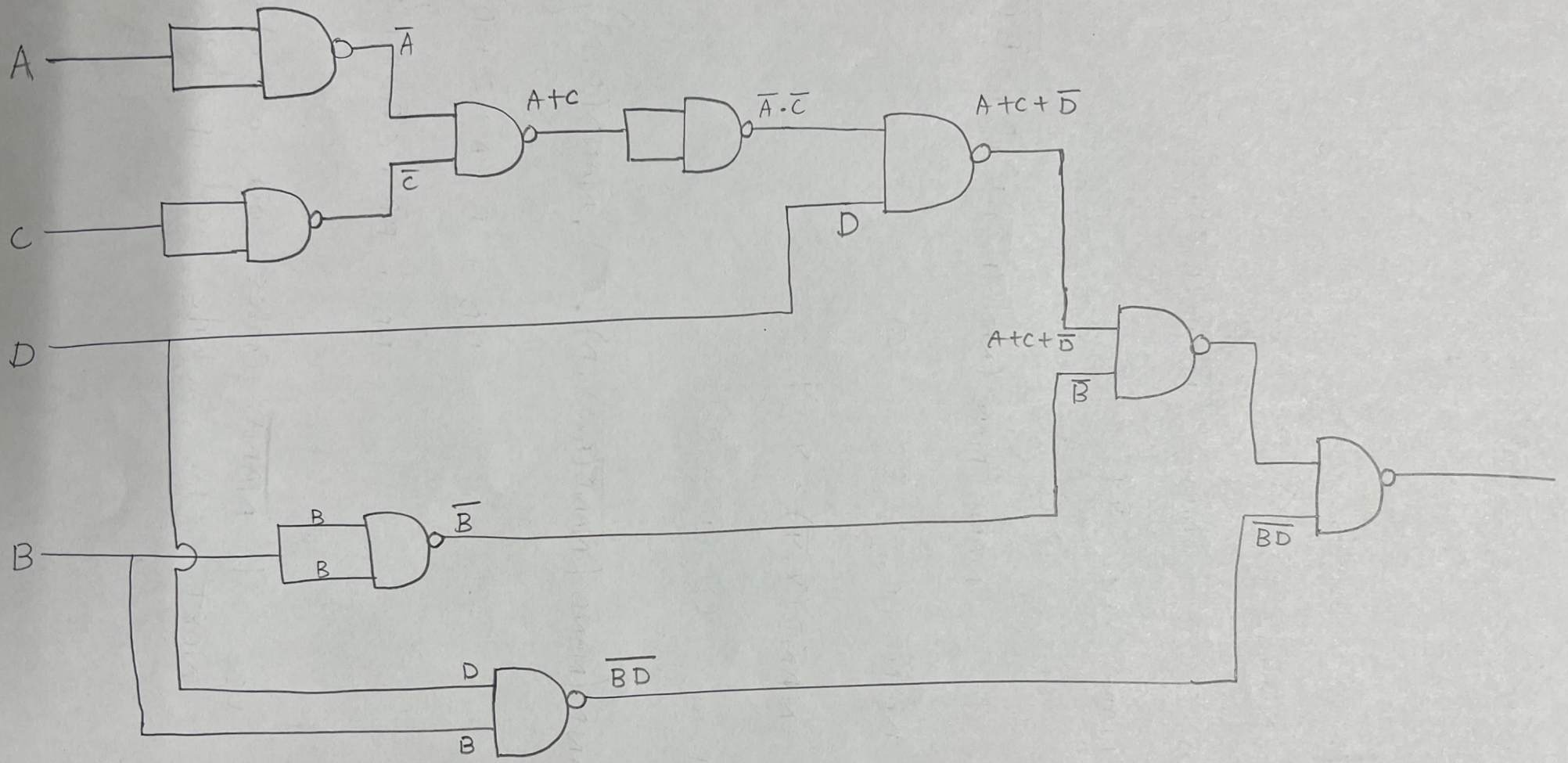
$$NAND\left(NAND\left(NAND\left(\overline{NAND(\bar{A},\bar{C})},D\right),\bar{B}\right),NAND(B,D)\right)$$

$$= BD + \bar{B}(A + C + \bar{D})$$

$$= BD + A\bar{B} + C\bar{B} + \bar{B}\bar{D}$$

Here, we use 9 NAND Gates out of which 4 are used as NOR Gates, while rest perform NAND.

Circuit Diagram



Approach 3 → (optimisation using 8 NAND Gates)

$F(A, B, C, D) = BD + \bar{B}\bar{D} + DC + DA + \bar{B}C + \bar{B}A$

$= NAND(\bar{D} + \bar{B}\bar{C}, B + \bar{A}D)$

$= NAND(NAND(D, B+C), B + \bar{A}D)$

$= NAND(NAND(D, B+C), NAND(A+\bar{D}, \bar{B}))$

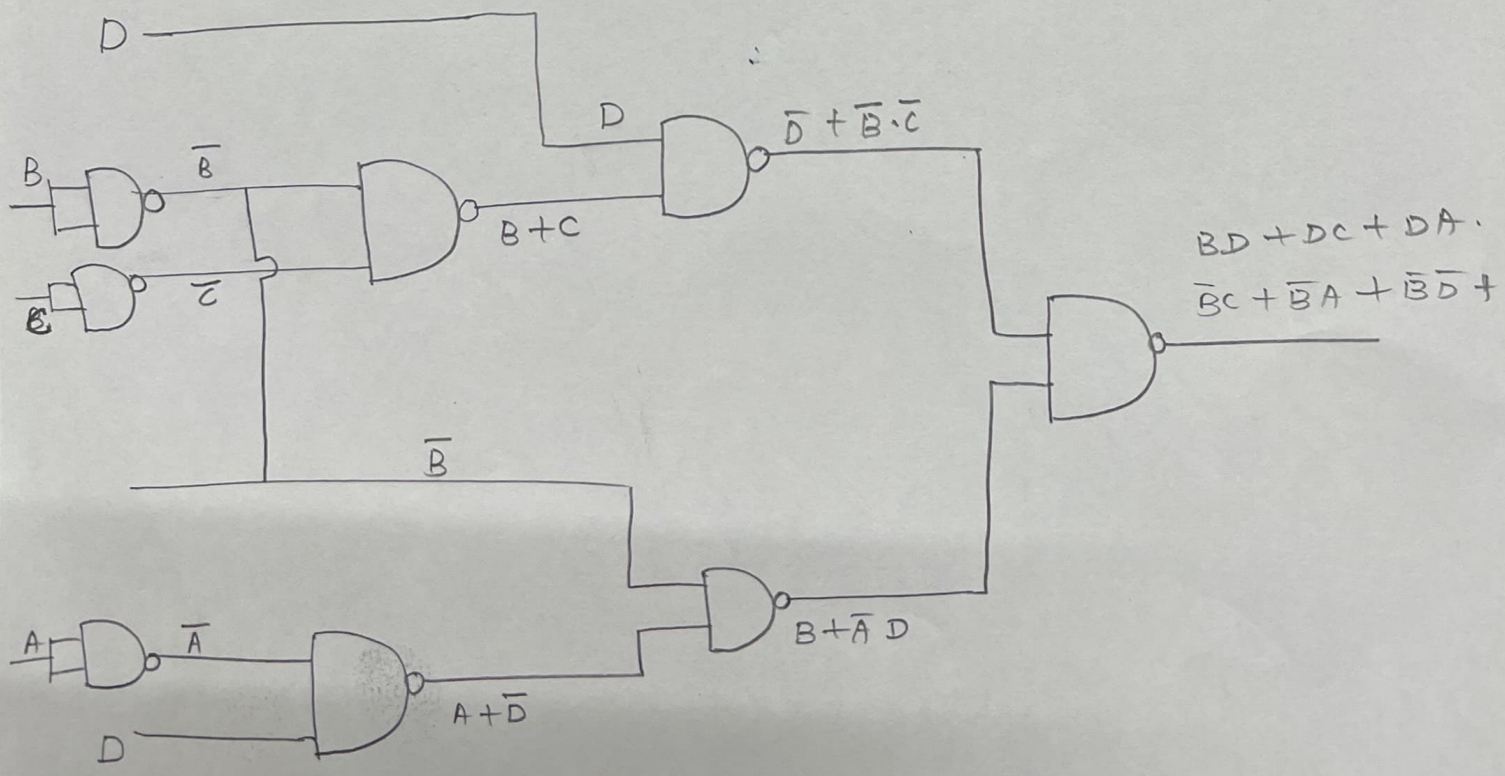
$= NAND(NAND(D, NAND(\bar{B}, \bar{C})), NAND(NAND(\bar{A}, D), \bar{B}))$

$= NAND[NAD(D, NAND(NADD(B, B), NAND(C, C))), NAND(NAND(NAND(A, A), D), NAND(B, B))]$

↓

8 NAND Gates

Circuit-Diagram :



FINAL APPROACH : 3