DC-DC BUCK CONVERTER FOR LOW VOLTAGE APPLICATIONS

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***Abstract*—This paper presents a DC-DC buck converter to convert the voltage from 3.3V to 2.1V, widely used in low-voltage applications. The buck converter works on the principle of PWM(Pulse Width Modulation). The transistor acts as a switch that connects and disconnects alternatively to the inductor with a duty cycle of 0.63. The current flow path and the time decide the capacitor charging, in turn, the output voltage. To stabilize the output, feedback is applied with an error amplifier, comparator, and driver circuits. Performance parameters are calculated for the proposed design which includes a Line transient of 160mV, a Constant load transient as ideal, and a step response in a few milliseconds. The DC-DC Buck Converter design and layout are implemented in 180nm CMOS technology.**

***Index Terms*—PWM,CMOS,Duty cycle**

I. Introduction

All electrical devices operate on a specific supply voltage, which is taken to be constant. A voltage regulator is an electrical circuit designed to provide a constant output. Various voltage regulator types and control methodologies are employed to regulate the output. Unregulated DC is fed into the DC-DC converter to produce regulated DC. There are several different types of conversion processes, including linear, switched mode, magnetic, electronic, and capacitive. The use of switching regulators is expanding as a result of their increased design flexibility and increased power conversion efficiency. Buck converters are switching regulators that have an efficiency of about 90 percent when converting high voltage to low voltage [9]. The main goal of using charge-storing elements is to achieve continuous output. They are used in devices like chargers, DRAM, CPUs and even in automotive field [5].

II. System Design

A step-down DC-to-DC buck converter is the proposed design. Conversion from high voltage to lower voltage is needed, which is achieved with the feedback circuit. The output voltage is the voltage across the capacitor and the charging of the capacitor depends on the time for which the current flows through the inductor. The MOSFET acts as a switch to alternatively connect and disconnect to the inductor. The duty cycle is provided by the feedback circuit which consists of an error amplifier, comparator [2] , and the driver circuit [13][14]. The output voltage is resistor divided and compared with the reference voltage and the error is amplified. The output of the error amplifier is then compared with the ramp signal to give the required duty cycle. The driver circuit drives the output of the comparator to the MOSFET input. Thus, the required output from the input voltage is obtained with stability. The block diagram of the buck converter is shown in Figure 1.

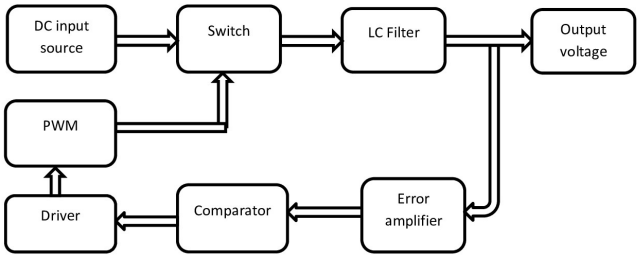

Fig. 1: Functional block diagram

To ensure the stability of the designed buck converter, stability analysis can be carried out and the closed loop [6] ensures this with a compensator. Based on the number of poles added in the converter design, the buck converter can be type1, type2, and type3 and the reliability of the buck converter increases from former to latter. This can be given with the following equations:

The transfer function for the open loop buck converter is given by:

$$V_{\text{out}} = D \cdot V_{\text{in}} \tag{1}$$

where D is the duty cycle.

Closed loop buck converter has the following transfer function as given in equation (2).

$$H_{LG}(s) = \frac{1}{LC} \cdot \frac{1}{s^2 + s\left(\frac{R_{LOSS}}{L} + \frac{1}{R \cdot C}\right) + \frac{1}{LC} \cdot \left(1 + \frac{R_{LOSS}}{R_{LOAD}}\right)} \quad (2)$$

Closed loop buck converter with compensator: (given in equation 3)

$$H_{LG}(s) = \beta \cdot \left(\frac{V_{dd}}{V_m}\right) \cdot \frac{1}{LC} \cdot \frac{1}{s^2 + \left(\frac{R_L}{L} + \frac{1}{R \cdot C}\right) s + \frac{1}{LC}} \quad (3)$$

where

β - Feedback Factor

and R, L, and C are the corresponding resistors, inductors, and capacitors used in the design.

A. Switch

Switch is the most essential part of the buck converter and it is shown in Figure 2.2. The MOSFET acts as a switch in the designed buck converter. The transistor is chosen as a switch because it dissipates almost no power [11]. It takes the duty cycle of the PWM signal [8] as its input to connect and disconnect to the inductor alternatively. The period the switch is turned on is referred to as the duty cycle. The path of the current and the time duration of its flowing through the inductor decide the voltage across the capacitor or the output voltage. Thus switch in the buck converter circuit plays a crucial role.

B. Error Amplifier

Error amplifiers compare two inputs and amplify the error [12][15] . In the designed buck converter circuit 7-pack opamp with 80db gain is used as an error amplifier. Figure 2. depicts the circuit of the same. As the output voltage is resistor divided and it may have variations, it is compared with the reference voltage taken which generates an error signal and is amplified. The output is fed to the comparator as input at the next stage. This part of the circuit comes in the feedback path of the buck converter and helps in stabilizing the circuit with minimum output voltage fluctuations. The choice of an error amplifier with good gain and bandwidth is important as it affects the transient response and stability.

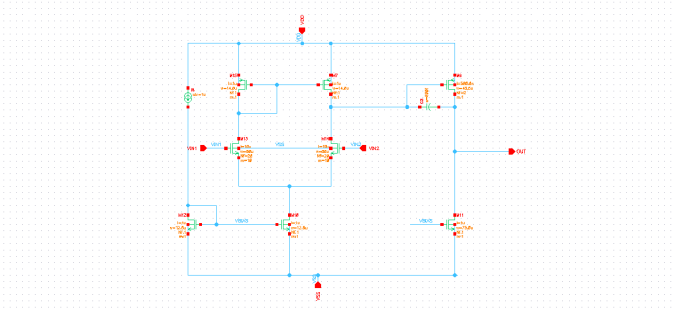

Fig. 2: Error Amplifier

C. Dynamic Comparator

Clocked comparators are often called dynamic comparators. They provide faster operation and lesser power dissipation the circuit of which is shown in Figure 3. The function of a comparator is to compare the given input with the reference value and give output high or low accordingly. In the designed buck converter, the comparator compares the output of the error amplifier with the reference ramp signal. For the input greater than the reference value, the output will be high(maximum supply given to the comparator circuit) and it follows the clock if the input signal is lesser than the reference ramp signal. The output of this circuit in the buck converter is the pwm signal upon which the the output value is decided.

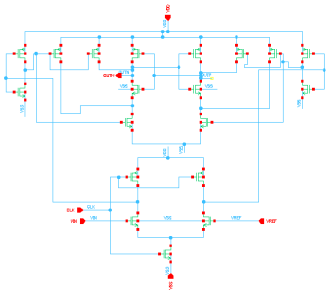

Fig. 3: Dynamic Comparator

D. Driver

They are usually used to regulate current flowing through a circuit or they control other devices in the circuit. The chain of inverters is used to drive the MOSFET which acts as a switch as shown in figure 4. It ensures that the switch turns on and off at the right time to regulate the output voltage. Minimizing the switching losses ensures that the efficiency is maximized. Ensuring smooth transition during switching and preventing voltage spikes contributes to the stability of the buck converter. Also, it ensures controlled power conversion.

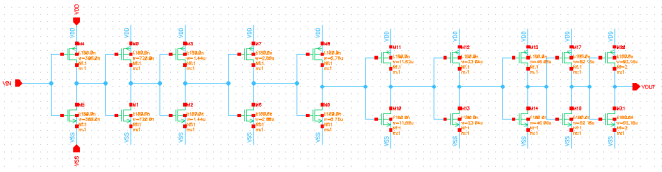

Fig. 4: Driver Circuit

III. Implementation of the System

The design specifications of the switch, error amplifier, dynamic comparator, and driver are tabulated below:

• Switch: The switch is the most essential part of the buck converter. It takes a duty cycle of PWM signal as its input to connect and disconnect to the inductor alternatively. The path of the current and the time duration of its flowing through the

inductor decide the voltage across the capacitor or the output voltage.

• Error Amplifier: Error amplifiers compare two inputs and amplify the error. As the output voltage is resistor divided and it may have variations, it is compared with the reference voltage taken which generates an error signal and is amplified. The output is fed to the comparator as input at the next stage.

• Comparator: The function of a comparator is to compare the given input with the reference value and give output high or low accordingly. The output of this circuit in the buck converter is the pwm signal upon which the the output value is decided. • Driver: They are usually used to regulate current flowing through a circuit or they control other devices in the circuit. The chain of inverters is used to drive the MOSFET which acts as a switch. It ensures that the switch turns on and off at the right time to regulate the output voltage.

A. *Design Specification*

– Input Voltage - 3.3V
– Output Voltage - 2.1V
– Power Supply - 3.3V

IV. Simulation and Waveforms

The complete system is simulated in the *Virtuoso Cadence* environment. The technology used is the *UMC 180nm*.

A. *Output of Error Amplifier*

The job of error amplification is done by a 7-pack opamp. Part of the output voltage is taken using a resistor divider and fed as one of the inputs to the error amplifier. The other input is the reference signal. Error in the output voltage is thus amplified. The output of this stage is saturated to 1.2V with a 3percent variation. This output as shown in Figure 5 acts as input to the next comparator stage.

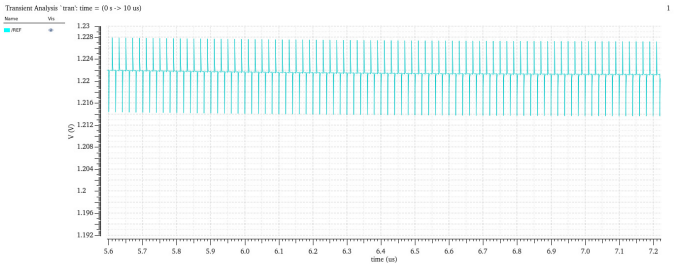

Fig. 5: Error Amplifier Output

B. *Output of Comparator*

The dynamic comparator is used in this system design of the buck converter. The output of the error amplifier and ramp signal of 3.3V with a 5ns period are compared. The ramp signal and the reference are chosen such that the desired duty cycle is obtained. For an input ramp signal greater than the reference, the output of the comparator is 1.2V with some ripples and for the same to be smaller, the output follows the clock of the dynamic comparator. The output of the comparator is shown in Figure 6.

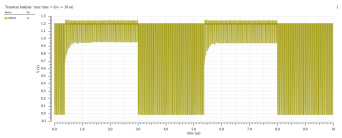

Fig. 6: Comparator Output

C. *Output of Driver*

The driver circuit takes input from the comparator. It minimizes voltage fluctuations and stabilizes the buck converter circuit. The output voltage from the comparator with some fluctuations is stabilized by the driver circuit. Figure 7 depicts the output of the driver circuit

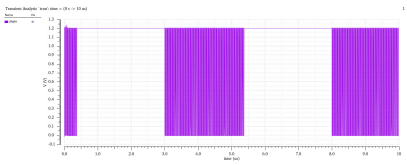

Fig. 7: Driver Output

V. Results

A. *Output of Buck Converter*

From the input voltage of 3.3V, an output of 2.1V was expected from the buck converter design. As per the current flow through the inductor and capacitor, the voltage across the capacitor is the output voltage required. The output of 2.1V is achieved with this buck converter with variations from 2V to 2.2V(0.2V variation) as shown in Figure 8

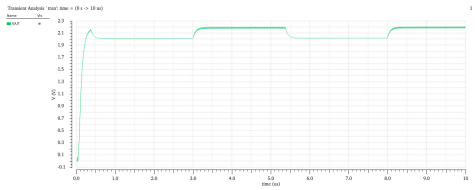

Fig. 8: Buck Converter Output

B. *Stability Analysis*

Stability analysis is the key principle where analytical methods are regularly used to study the properties of dynamic systems. In this work, analysis of stability is done through simulation in Cadence Virtuoso and Matlab [3][7].

Bode Plot: Frequency response of the linear time-invariant system. The designed buck converter is stable with a Phase Margin of 90.3 degrees and Gain Margin of 4.51dB as shown in figure 9.

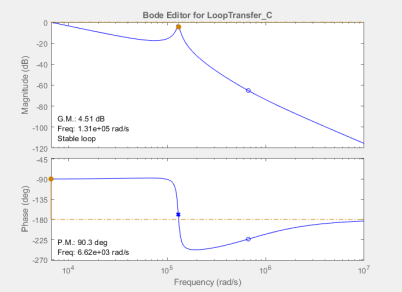

Fig. 9: Bode Plot

C. Parameters of Buck Converter

Buck Converter parameters like line transient, load transient, and line regulations are discussed in this section.

• Step Response: The response of the system is recorded for the step input as it defines how the system behaves when input is suddenly changed and how fast it can settle. The settled graph shows that it takes a few milliseconds to settle.

• Line Transient: It is a step function containing the Fourier components of the step. It injects disturbance at the input. It is 160mV for the design as shown in figure 10.

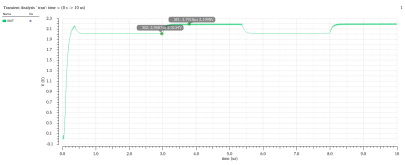

Fig. 10: Line Transient

•Line regulation: The ratio of change in output voltage to change in input current is line transient. Ideally, the plot should be a horizontal line as shown in Figure 11.

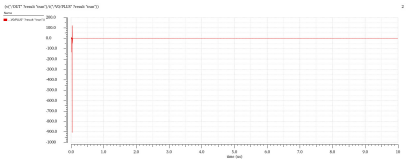

Fig. 11: Line Regulation

• Load transient: This is similar to line transient, the difference is instead of changing input, we change the load, the result of which is shown in figure 12. It is also the sudden changes in load current for which how a particular system can regulate its output voltage.

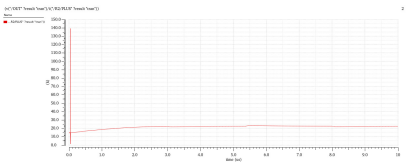

Fig. 12: Load Transient

VI. Layout

This section of the paper discusses about the layout of the switching DC-DC buck converter. It includes layouts of a switch, an error amplifier, a dynamic comparator, and a driver circuit. The layout for the buck converter implemented in 180nm CMOS technology is shown in figure 13.

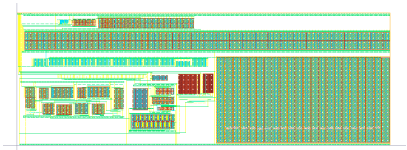

Fig. 13: Layout of dc-dc buck converter

All cells met DRC(Design Rule Check) and LVS (Layout versus Schematic) clean specifications which are shown in figure 14 and figure 15 respectively.

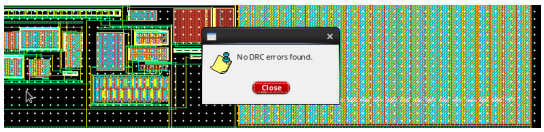

Fig. 14: DRC Clean

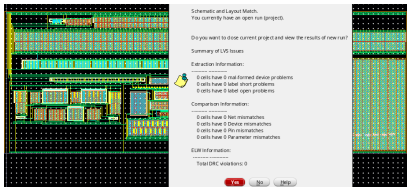

Fig. 15: LVS Clean

VII. Performance Comparison

Table 1 (figure 16) shows the comparison with previously worked papers [1], [4], [10] which are arranged in the sequence as they are referred to in this work. The technology used in this work is more advanced compared to other works which can add to several advantages like smaller feature size, higher performance, low power consumption, etc. Next to simulation, the layout for the design is done for the presented work, whereas papers [1] and [10] have not proposed post-simulation works, the work proposed in paper [4] has been fabricated. The presented work and the paper [10] have the stability analysis results added ensuring reliability, whose data is not available for papers [1] and [10].

VIII. Conclusion

• In this paper, a switching DC-DC Buck converter design and layout is proposed. The design includes a switch, error amplifier, dynamic comparator, and driver circuit, and the layout for the same is implemented in 180nm CMOS technology.

• Dynamic comparator is used in the buck converter design as it is a better candidate when it comes to low power, low offset, and high-speed applications.

Reference	[1]	[4]	[10]	This work
Year	2021	2011	2018	2024
Process	Not specified	0.5 um Bi-CMOS	0.35 um CMOS	180nm CMOS
Vin	20 V	2.7-5.5 V	5 V	3.3 V
Vout	10 V	1.2 V	3.3 V	2.1 V
Duty cycle	0.5	0.44	0.66	0.63
O/P ripple	Not specified	4 mV	Not specified	200 mV
Stability (UGB,PM(in degree))	N/A	540 MHz, 46	N/A	6.829 KHz, 50.39
Further work	Not specified	Fabricated	Not specified	Layout

Fig. 16: Table 1: Comparison Table

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