## **Sprint-1**

## **Introduction**

## In this Sprint, the goal was to develop a working product for floor planning a System-on-Chip (SoC). The following sections document the User Stories and Tasks I worked on in detail.

## **User Story**

## **User Story: SoC and CPU Floor Planning**

## As a SoC Floor Planning Engineer, I want to define and partition functional blocks, integrate standard cell libraries, and ensure design compatibility with SkyWater 0.13um constraints so that I can create an optimized layout that meets performance, power, and manufacturability goals.

## **Conditions of Satisfiability**

## Functional blocks (CPU, memory, I/O) are correctly partitioned.

## Standard cell libraries are integrated following SkyWater 0.13um design rules.

## The floor plan must be DRC/LVS clean with no major violations.

## Macro placement should minimize routing congestion and optimize power distribution.

## **Definition of Done**

## Functional blocks are partitioned and validated.

## Standard cell libraries are correctly placed and verified.

## DRC/LVS checks pass with no major violations.

## The floor plan is optimized for routing feasibility and power distribution.

## The design is ready for further refinement and tape-out.

## **Tasks Worked On**

## **Task 1: Design Partitioning (4 ph) [GitHub Issue #2]**

## Defined functional blocks (CPU, memory, I/O) and allocated areas.

## Created a hierarchical organization for the design.

## Validated partitions against floor planning constraints.

## Ensured functional alignment with SkyWater 0.13um guidelines.

Task:

[Floor.1: Design Partitioning #2](https://github.com/Rivier-Computer-Science/OctoNyte/issues/2)

## **Summary Table of Work**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **GitHub Issue ID** | **User Story** | **Story Points** | **Task** | **Task GitHub Issue ID** | **Task Hours** | **Status** | **Actual Hours** |
| [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | SoC and CPU Floor Planning | 3 | Design Partitioning | [#2](https://github.com/Rivier-Computer-Science/OctoNyte/issues/2) | 6 | Completed | 4 |

## **Summary Table of Commits**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Date | Commit Number | Commit Description | User Story | Task |
| 02/03/2025 | [94ddba4](https://github.com/Rivier-Computer-Science/OctoNyte/commit/94ddba4) | Configure Openlane to run in docker mounted shell | [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | [#2](https://github.com/Rivier-Computer-Science/OctoNyte/issues/2) |

**Conclusion**

Sprint-1 successfully established the foundation for SoC floor planning. The design partitioning task was completed with validation of functional block allocations. The work contributed to an optimized floor plan that aligns with SkyWater 0.13um constraints, ensuring a clean and manufacturable design layout.