**Sprint 2**

**Introduction**

In this Sprint, the goal was to extend the SoC floor planning by completing the design and validation of Library Integration and Macro Placement. The following sections document the User Stories and Tasks I worked on in detail.

**User Story**

User Story: SoC and CPU Floor Planning (Extension for Library Integration & Macro Placement)

As a SoC Floor Planning Engineer, I want to define and partition functional blocks, integrate standard cell libraries, and ensure design compatibility with SkyWater 0.13um constraints so that I can create an optimized layout that meets performance, power, and manufacturability goals.

**Conditions of Satisfiability**

* Library Integration ensures proper standard cell placement and compliance with SkyWater 0.13um rules.
* Macro Placement focuses on positioning large components efficiently for power distribution and routing.
* The design must maintain an optimized hierarchy for performance and manufacturability.
* Macro placement should be optimized to reduce congestion and improve manufacturability.
* The final floor plan must be DRC/LVS clean with no violations.

**Definition of Done**

* Library Integration is completed with validated standard cell placements.
* Macro Placement is finalized with proper alignment and spacing.
* Standard cell libraries are correctly placed and verified.
* DRC/LVS checks pass with no major violations.
* Routing feasibility and signal integrity checks are completed.
* The design is ready for further refinement and tape-out.

**Tasks Worked On**

Task 2: Library Integration (5 ph) [GitHub Issue #33]

* Defined functional blocks and allocated areas.
* Created a hierarchical organization for the design.
* Validated partitions against floor planning constraints.
* Ensured functional alignment with SkyWater 0.13um guidelines.

Task 3: Macro Placement (6 ph) [GitHub Issue #34]

* Extended the floor planning to include additional functional blocks.
* Optimized placement strategies to enhance performance and power distribution.
* Verified alignment with design constraints and manufacturing requirements.
* Conducted routing feasibility analysis.

Tasks:

[Floor.2: Library Integration #33](https://github.com/Rivier-Computer-Science/OctoNyte/issues/33)

[Floor 3: Macro Placement #34](https://github.com/Rivier-Computer-Science/OctoNyte/issues/34)

**Summary Table of Work**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **GitHub Issue ID** | **User Story** | **Story Points** | **Task** | **Task GitHub Issue ID** | **Task Hours** | **Status** | |  |  | | --- | --- | |  | **Actual Hours** | |
| [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | SoC and CPU Floor Planning | 3 | Library Integration | [#33](https://github.com/Rivier-Computer-Science/OctoNyte/issues/33) | 4 | Completed | 5 |
| [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | SoC and CPU Floor Planning | 3 | Macro Placement | [#34](https://github.com/Rivier-Computer-Science/OctoNyte/issues/34) | 6 | Completed | 6 |

**Summary Table of Commits**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Date** | **Commit Number** | **Commit Description** | **User Story** | **Task** |
| 02/19/2025 | [C938d65](https://github.com/Rivier-Computer-Science/OctoNyte/pull/51/commits/c938d65df8cfbfd0a7f7f158d3d02e67e9bf899a) | Updated Time period | [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | [#33](https://github.com/Rivier-Computer-Science/OctoNyte/issues/33), [#34](https://github.com/Rivier-Computer-Science/OctoNyte/issues/34) |
| 02/19/2025 | [7e8dfda](https://github.com/Rivier-Computer-Science/OctoNyte/pull/51/commits/7e8dfdaec1900700073bee9317a5a055764846dc) | Added TetraNyteCore and TetraNyteCore\_Synth | [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | [**#**33](https://github.com/Rivier-Computer-Science/OctoNyte/issues/33)**,** [#34](https://github.com/Rivier-Computer-Science/OctoNyte/issues/34) |

**Conclusion**

Sprint-2 successfully extended the SoC floor planning by finalizing Library Integration and Macro Placement. The design partitioning tasks were completed with validation of functional block allocations. The work contributed to an optimized floor plan that aligns with SkyWater 0.13um constraints, ensuring a clean and manufacturable design layout.