**Sprint 3**

**Introduction**

The focus of Sprint 3 was to integrate configuration scripts required for OpenLane 1.1.1. This involved preparing, organizing, and validating .tcl files used for flow configuration to enable efficient and reproducible digital design implementation using the SkyWater 130nm PDK. The primary objective was to align the design environment with the updated OpenLane version while ensuring compatibility and automation in the workflow.

**User Story**

User Story: SoC and CPU Floor Planning (Extension for Library Integration & Macro Placement)

As a Physical Design Engineer, I want to organize and validate .tcl config files for OpenLane 1.1.1 so that I can ensure a clean, automated, and version-compatible flow for RTL-to-GDSII implementation.

**Conditions of Satisfiability**

* All .tcl configuration files must be properly structured and compatible with OpenLane 1.1.1.
* Config files must comply with the design and process constraints of SkyWater 130nm PDK.
* Script execution should pass without errors in test runs.
* The structure should support reuse and future project integration.

**Definition of Done**

* .tcl config files created and pushed to repository.
* Scripts verified for syntax and execution compatibility.
* Changes merged successfully in GitHub.
* Design passes basic configuration and flow setup steps with OpenLane 1.1.1.

**Tasks Worked On**

**Task 4: Signal Routing & Feasibility (6 ph)** [GitHub Issue #58]

* Created and organized multiple .tcl configuration files.
* Ensured compatibility with OpenLane 1.1.1 flow requirements.
* Validated script structure and syntax via dry runs.
* Merged the changes into the Sprint-3 branch.

Tasks:

[Floor 4: Signal Routing & Feasibility #58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58)

**Summary Table of Work**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **GitHub Issue ID** | **User Story** | **Story Points** | **Task** | **Task GitHub Issue ID** | **Task Hours** | **Status** | **Actual Hours** |
| [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | SoC and CPU Floor Planning | 3 | Signal Routing & Feasibility | [#58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58) | |  |  | | --- | --- | | 6 |  | | Completed | 6 |

**Summary Table of Commits**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Date | Commit Number | |  |  | | --- | --- | | Commit Description |  | | User Story | Task |
| 03/27/2025 | 27b6cea | OpenLane 1.1.1 tcl config files | [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | [#58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58) |

**Conclusion**

Sprint 3 accomplished the setup and integration of .tcl config files needed for OpenLane 1.1.1. These configurations are essential for managing design parameters and automating synthesis, placement, and routing steps. The work has laid a strong foundation for subsequent physical design and tape-out stages by enabling a streamlined and compatible flow within OpenLane.