**Sprint 4**

**Introduction**

The focus of Sprint 4 was to integrate YAML configuration scripts required for **OpenLane2** within a **Nix-shell** environment. This involved preparing, organizing, and validating .yaml files used for flow configuration to enable efficient and reproducible digital design implementation using the SkyWater 130nm PDK. The primary objective was to align the design environment with the updated OpenLane2 flow while ensuring compatibility, automation, and reproducibility of the workflow.

**User Story**

User Story: SoC and CPU Floor Planning (Extension for Library Integration & Macro Placement)

As a Physical Design Engineer, I want to create and validate a custom register file and supporting YAML configuration for OpenLane2 so that I can ensure clean, modular, and reusable configurations for RTL-to-GDSII physical implementation in a reproducible Nix-shell environment.

**Conditions of Satisfiability**

* YAML configuration files must be properly structured and compatible with OpenLane2.
* Config files must comply with the SkyWater 130nm PDK requirements.
* The directory regfile\_2r1w under octonyte/jg-floorplan/designs/ must integrate successfully with OpenLane2 flows.
* All flows must complete without errors during test executions inside Nix-shell.

**Definition of Done**

* YAML files created within octonyte/jg-floorplan/designs/regfile\_2r1w.
* YAML validated for correctness and compatibility within OpenLane2 via Nix-shell.
* Commits merged to the Sprint-4 branch in GitHub.
* The design completes synthesis, floor planning, and routing stages in OpenLane2.

**Tasks Worked On**

**Task 4: Signal Routing & Feasibility (6 ph)** [GitHub Issue #58]

* Created YAML configuration for a register file design under regfile\_2r1w.
* Ensured YAML compatibility with OpenLane2 workflow.
* Executed flow stages using Nix-shell to validate structure and functionality.
* Pushed verified configuration and committed changes to GitHub.

Tasks:

[Floor 4: Signal Routing & Feasibility #58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58)

**Summary Table of Work**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **GitHub Issue ID** | **User Story** | **Story Points** | **Task** | **Task GitHub Issue ID** | **Task Hours** | **Status** | **Actual Hours** |
| [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | SoC and CPU Floor Planning | 3 | Signal Routing & Feasibility | [#58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58) | |  |  | | --- | --- | | 6 |  | | Completed | 6 |

**Summary Table of Commits**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Date | Commit Number | |  |  | | --- | --- | | Commit Description |  | | User Story | Task |
| 04/23/2025 | 0d4df2c | Custom Register File and YAML Configuration | [#1](https://github.com/Rivier-Computer-Science/OctoNyte/issues/1) | [#58](https://github.com/Rivier-Computer-Science/OctoNyte/issues/58) |

**Conclusion**

Sprint 4 accomplished the development and integration of a YAML-based configuration for the regfile\_2r1w design under octonyte/jg-floorplan/designs/ using OpenLane2 in a Nix-shell environment. This effort ensures a modular, reproducible setup aligned with the SkyWater 130nm PDK and establishes a reliable foundation for ongoing layout and physical design tasks.