DMD 101 – Introduction to DMD technology

This document describes basic structure and operation of the DMD array.

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1   Overview

This document covers the basic structure and operation of DMD devices. The DMD is a unique combination of opto-mechanical and electro-mechanical elements. The journey begins with understanding how one pixel works and building on that to encompass the entire array of pixels that comprise a DMD.

2   The Pixel

The DMD Pixel (mirror) is both an opto-mechanical element and an electro-mechanical element.

2.1   Bi-Stable Operation (+12 degrees and -12 degrees)

The DMD Pixel is an electro-mechanical element in that there are two stable mirror states (+12 degrees and -12 degrees for current DMDs) which are determined by electrostatics of the pixel during operation.

The DMD Pixel is an opto-mechanical element in that these two positions determine the direction that light is deflected. In particular the DMD is a "spatial light modulator". By convention the "+" state is tilted toward the illumination and is referred to as the "on" state. Similarly the "–" state is tilted away from the illumination and is referred to as the "off" state. Figure 1 shows a pixel in the "on" state and a pixel in the "off" state.
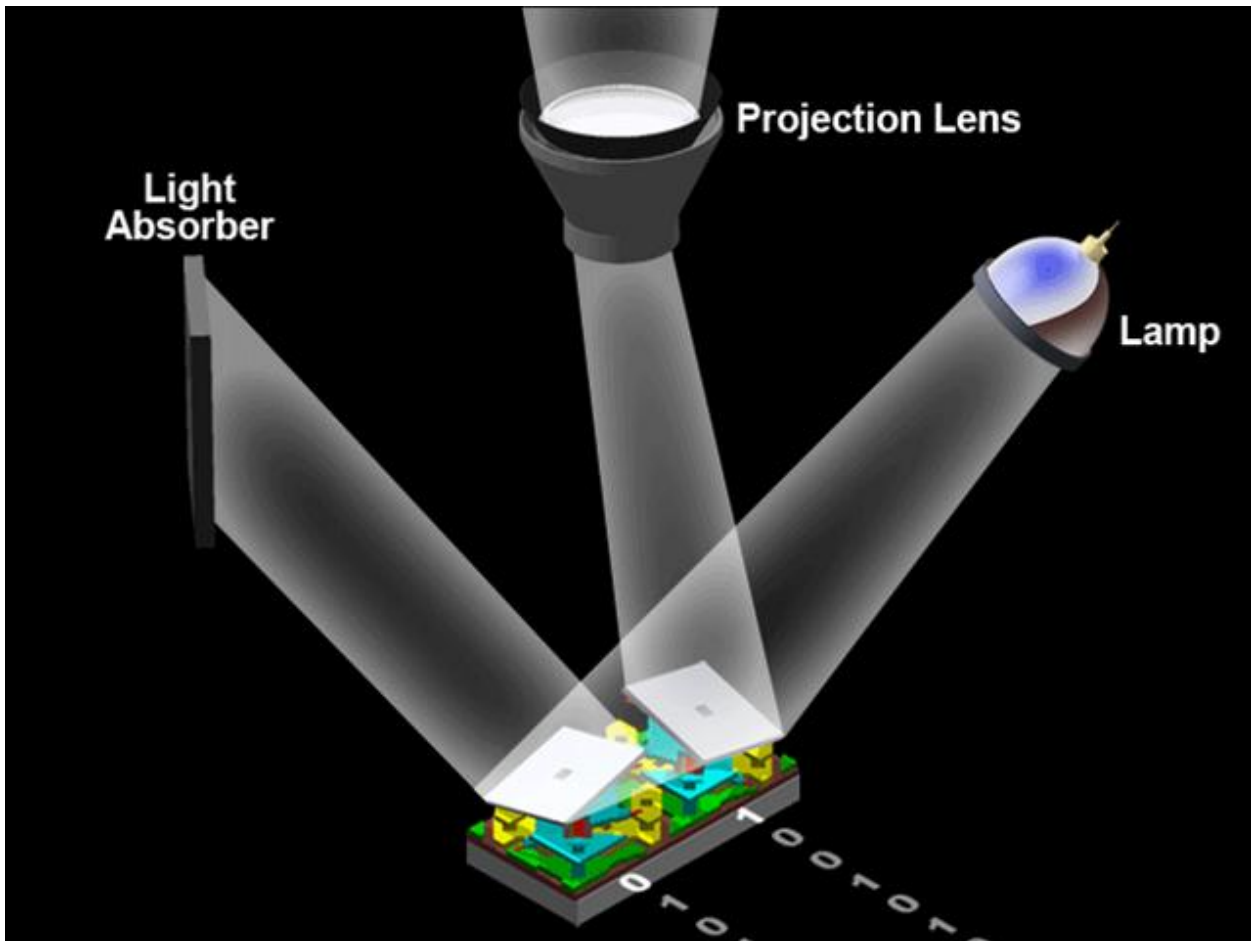

Figure 1 – Pixels in "On" and "Off" State

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2.2 *Mechanical*

Mechanically the pixel is comprised of a mirror attached by means of a via to a hidden yoke and a torsional hinge. The yoke makes contact with the surface below on the spring tips shown in Figure 2. The diagram also shows a mirror in each of the two stable states. The yellow electrodes shown are used in holding the mirror in these positions.
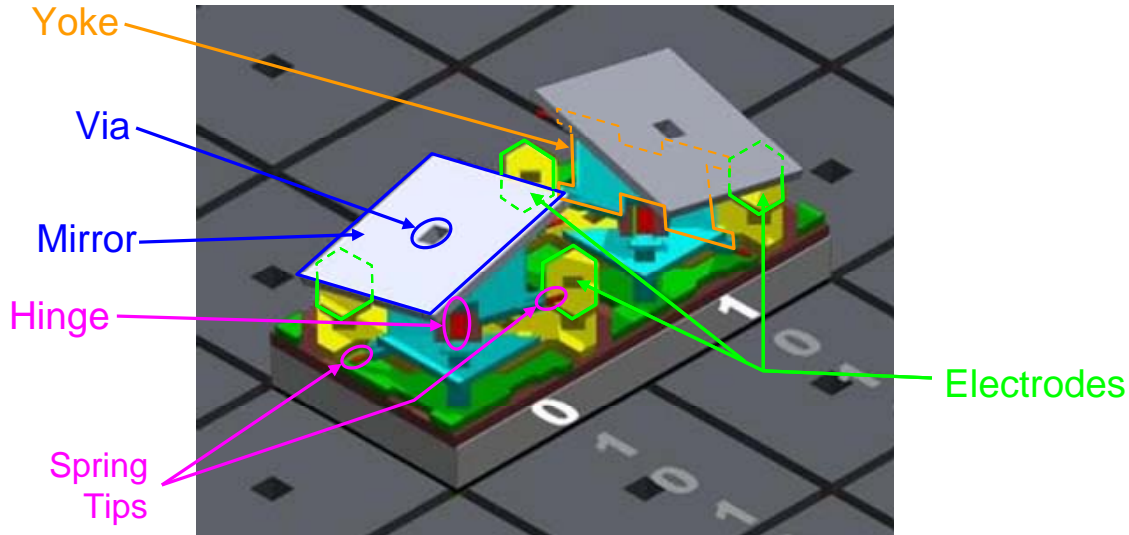

Figure 2 – Pixel showing labeled parts

.

2.3 *Electrical*

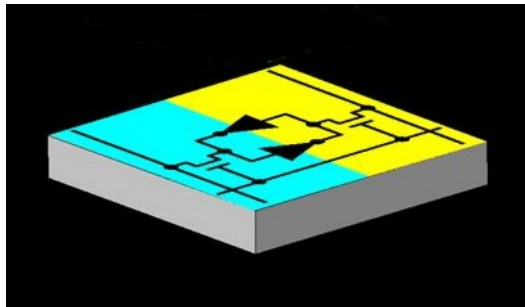### 2.3.1 Dual CMOS Memory

Figure 3 – Dual CMOS Pixel Memory

Below each mirror is a memory cell formed from Dual CMOS memory elements as depicted in Figure 3. The state of the two memory elements are not independent, but are always opposite. If one element is 1 the other element is 0 and visa-versa. The state of the Pixel memory cell plays a part in the mechanical position of the mirror, however, loading the memory cell does not automatically change the mechanical state of the mirror.

2.3.2 Memory State vs Mirror State

Although the state of the dual CMOS cell plays a part in determining the state of the mirror, it is not the sole factor. Once the mirror has landed changing the state of the memory cells will not cause

the mirror to flip to the other state. Therefore, Memory State and Mirror State are not directly linked together.

2.3.3 RESET – Transferring Memory State to Mirror State

In order for the state of the CMOS memory to be transferred to the mechanical position of the mirror, the pixel must undergo a "Reset". This Reset momentarily releases the mirror and then re-lands the mirror based on the state of the CMOS memory below. Therefore it is important that during a Reset operation that the memory cell is not being loaded. Specifically, the various DMD Data Sheets specify the time before a Reset that data cannot be loaded and the period of time after a Reset has occurred before new data can be loaded.

A Reset allows groups of pixels to be pre-loaded and then change their mechanical position simultaneously.

2.3.4 Power Up and Power Down

When a DMD is "powered up" or "powered down" there are prescribed operations that are necessary to ensure proper operation of the mirrors. These operations land the mirrors during power up and release the mirrors during power down. Specific details are described in the various DMD Data Sheets.

3   The DMD Array

A DMD is an array of individual pixels, the array dimensions being determined by the resolution of the particular DMD. For the purposes of this paper consider a DMD with XGA resolution; 1024 columns by 768 rows.
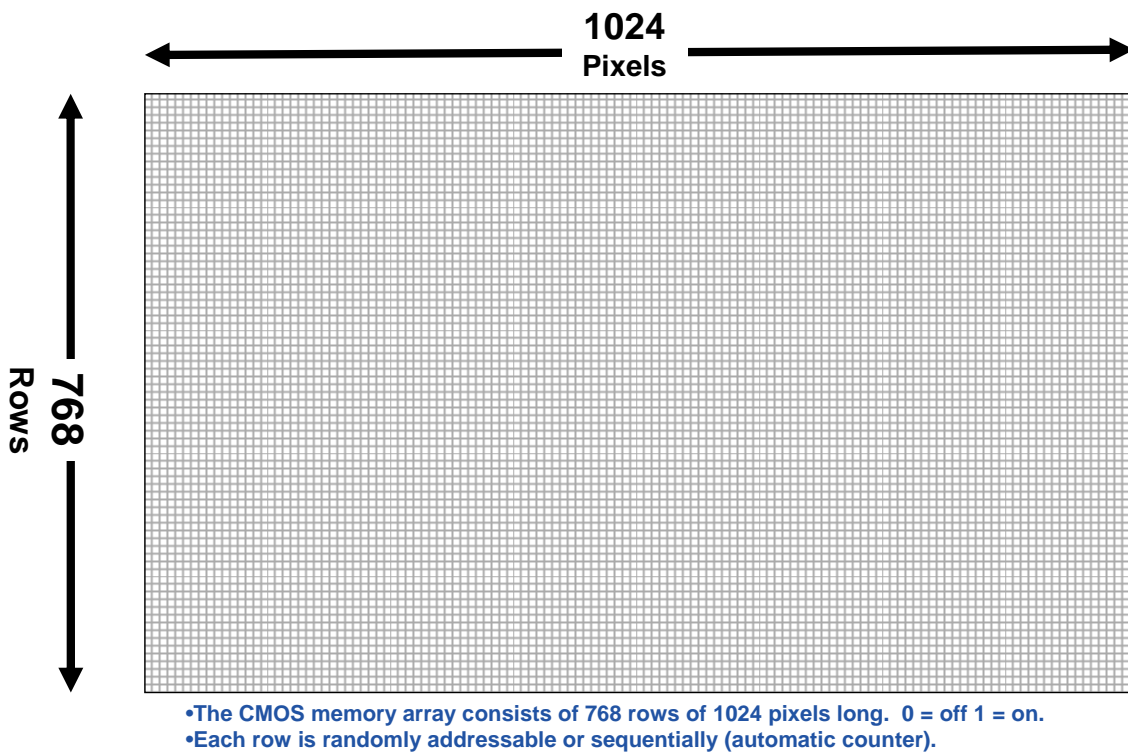

•The CMOS memory array consists of 768 rows of 1024 pixels long. 0 = off 1 = on.
•Each row is randomly addressable or sequentially (automatic counter).

Figure 4 – DMD Array

DMD memory is loaded by row. An entire row must be loaded even if only one pixel in the row needs to be changed

3.1   Row Load

Loading a row is accomplished via a parallel bus of 16 or 32 bits. Current 2xLVDS XGA devices use a 32 bit wide bus. This data is loaded on both rising and falling edges of the data clock (known as Dual Data Rate – DDR). For the XGA device a 32 bit wide bus over 32 clock edges are needed to load a full 1024 bits to complete a Row Load. Figure 4 shows graphically a Row Load.
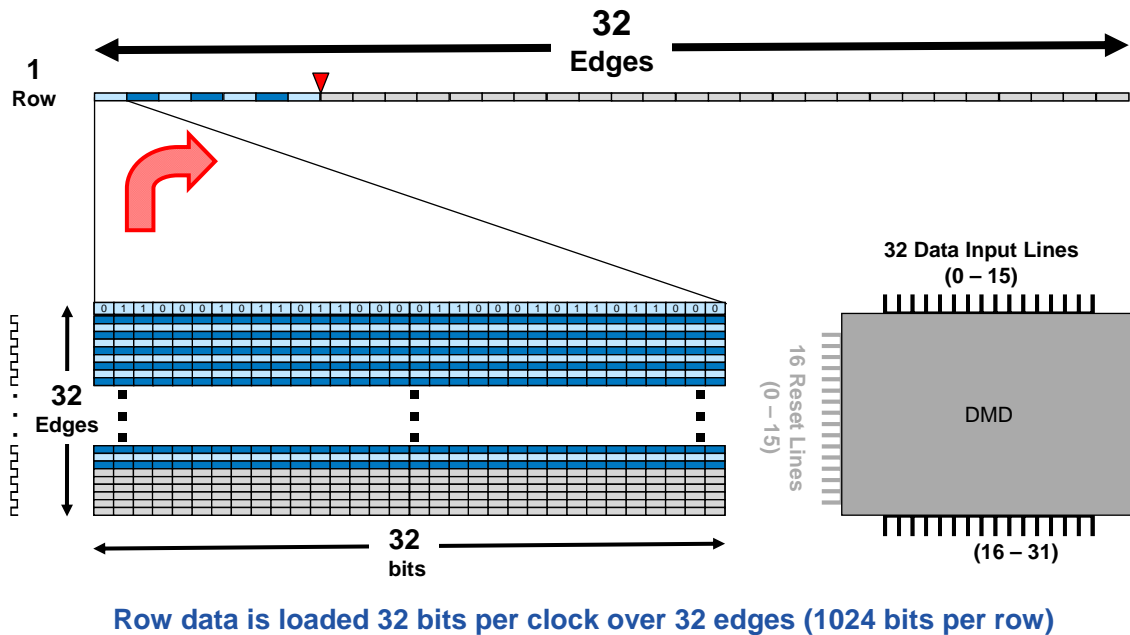
Row data is loaded 32 bits per clock over 32 edges (1024 bits per row)

Figure 5 – Row Load

3.2   Row Addressing

Rows can be addressed sequentially by way of an automatic counter or randomly by row address.

3.2.1   Sequential Mode (Automatic Counter)

Sequential addressing means that when row (n) is loaded, the DMD internally increments the row address pointer to (n + 1). NOTE: However the pointer does not automatically reset to 0 when the last row is load. An explicit command to set the pointer to zero must be issued.

This mode is useful when it is expected that most of the data in the image will change each time the device is loaded. It also does not require the user to keep track of the row address pointer.

3.2.2   Random Mode

Random addressing means that as row data is supplied a row address (n) must also be supplied. The DMD will then load the row data to row (n) specified by the row address.

This mode is useful when it is expected that the data in the image will only change in a subset of rows. However it does requires the user to keep track of row address pointer and supply during each row load.

4   Block Operations

For the purpose of Resetting and Block Clearing the DMD is divided into "Blocks". XGA devices are divided into 16 blocks of 48 rows each. Figure 5 illustrates the Blocks.
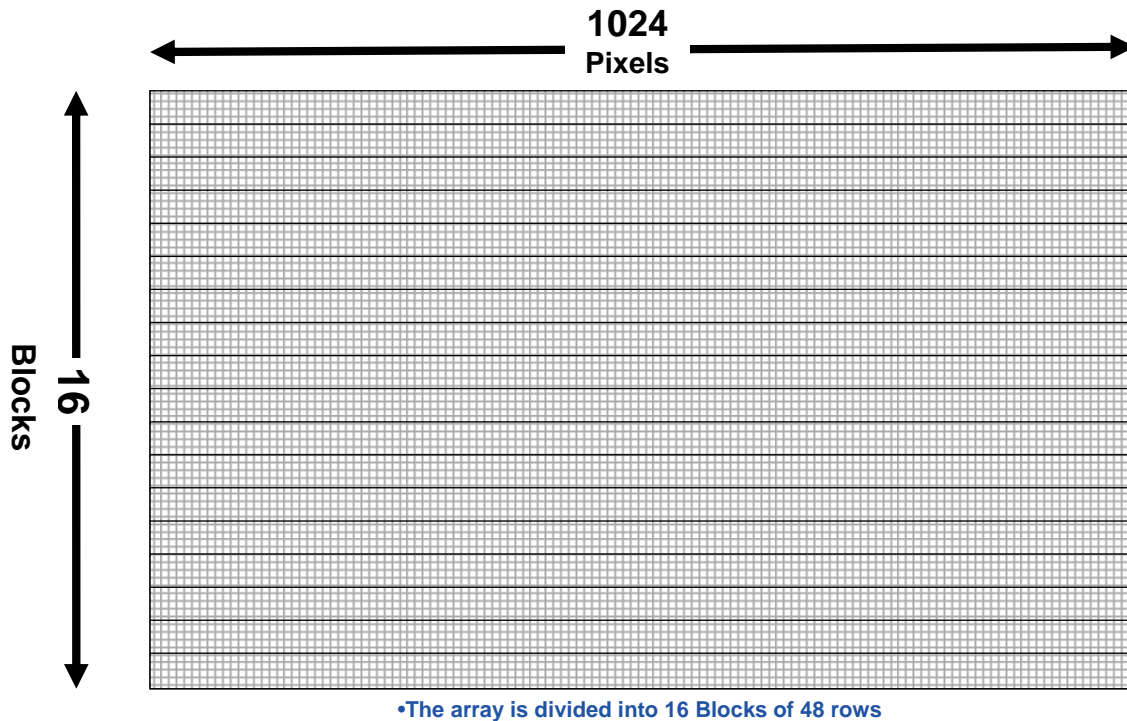
1024
Pixels

16
Blocks

•**The array is divided into 16 Blocks of 48 rows**

.

Figure 6 – DMD Blocks

4.1   Resets

Previously it was noted that loading the CMOS memory does not cause the mirrors to change their mechanical state and that in order for the loaded memory to change the mechanical position of the mirrors a "Reset" must be issued.

When a Reset is issued to a Block the pixels in that block whose data has changed will move to the opposite mechanical position and those whose data did not change will remain in the same mechanical position. These operations are referred to as "cross-over" transitions and "same-side" transitions respectively.

NOTE: Although memory cannot be loaded in a block that is being reset, memory can be loaded in different block while another block is being reset. However, there is a minimum time that must transpire after a block is reset before new data can be loaded to that block. This wait time is referred to as the "Mirror Settle Time".

The DMD has 16 Reset input lines; one for each block as illustrated in Figure 6.
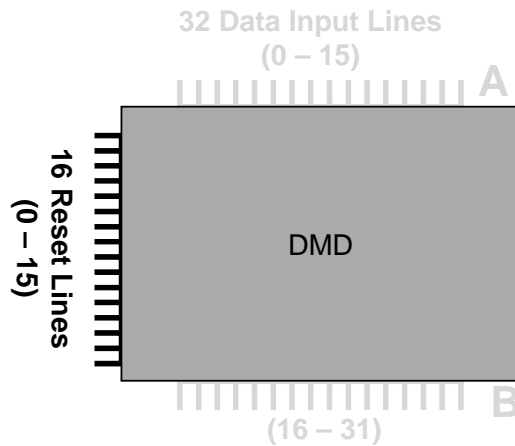
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Figure 7 – DMD Reset Lines

There are four Reset Modes that determine which blocks are reset when a Reset is issued:

- Single Block Mode

- Dual Block Mode

- Quad Block Mode

- Global Mode

4.1.1 Single Block Mode

In Single Block Mode a single blocks can loaded and reset in any order. After a block is loaded it can be reset to transfer the information to the mechanical state of the mirrors.

Figure 8 – Single Block Reset

4.1.2 Dual Block Mode

In Dual Block Mode reset blocks are paired together as follows (0-1), (2-3), (4-5) . . . (14-15). These pairs can be reset in any order. After data is loaded a pair can be reset to transfer the information to the mechanical state of the mirrors.
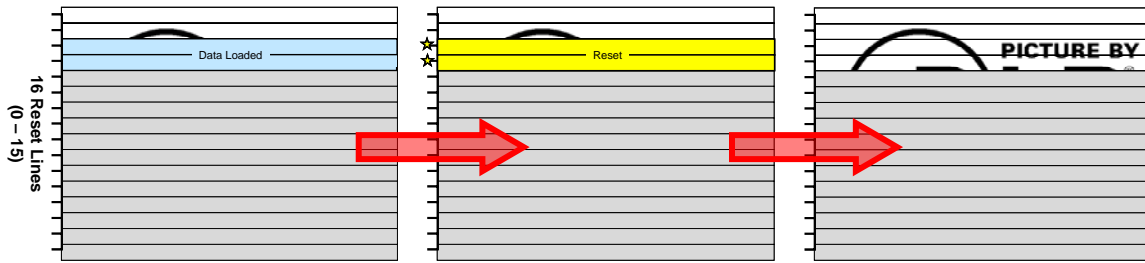
Figure 9 – Dual Block Reset

4.1.3 Quad Block Mode

In Quad Block Mode reset blocks are grouped together in fours as follows (0-3), (4-7), (8-11) and (12-15). However each quad group can be randomly addressed and reset. After a quad group is loaded it can be reset to transfer the information to the mechanical state of the mirrors.
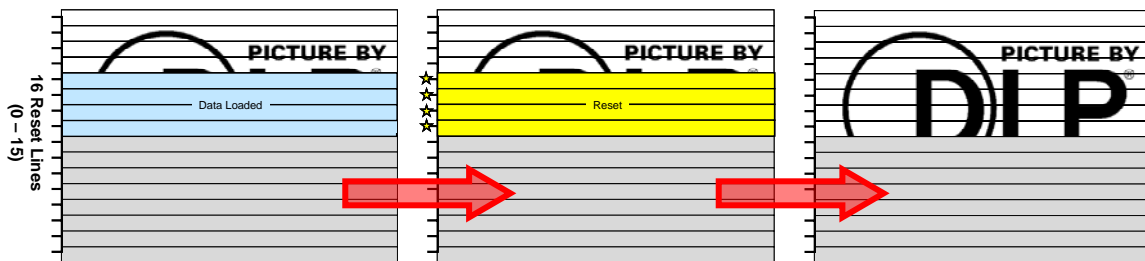

Figure 10 – Quad Block Reset

4.1.4 Global Mode

In Global Mode all reset blocks are grouped into a single group and reset together. Therefore the entire DMD must be load with the desired data before issuing a Global Reset to transfer the information to the mechanical state of the mirrors.

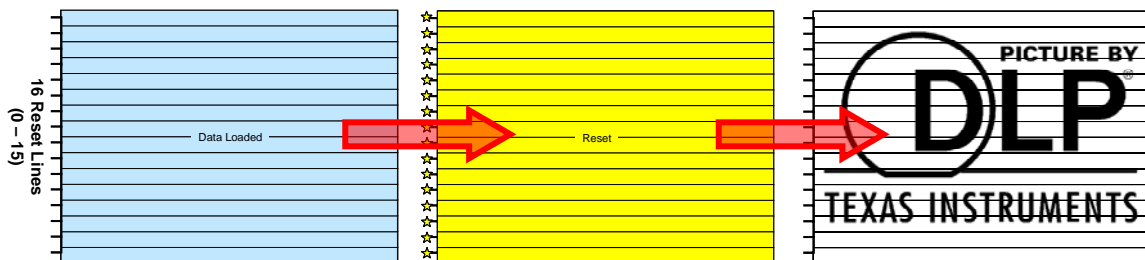*Figure 11 – Global Reset*

4.2 Block Clear

Although memory can be "cleared" by loading all zeros into a block a special block function known as a "Block Clear" can be issued. Loading 48 rows would require 48x32 (1536) clock edges, but a Block Clear causes the DMD to load all zero's into the specified block. For a 2xLVDS DMD a Block clear command takes the same amount of time as three Row Load operations. In other words, in the time

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that it would take to load 3 rows of data (144 clock edges) an entire block can be loaded with zeros. Therefore it is possible to clear the entire DMD memory in the time it would take to load a single block (16 times faster than loading zeros using row loads). This function is useful when short display times are desired.

NOTE: A Block Clear and a Row Load operation cannot be executed simultaneously, even if the row is not in the block to be cleared.

4.3 Phased Operation

4.3.1 Motivation

For some applications it is desirable to display a given image (binary frame) for a very short period of time.

If a Global Reset is used the array cannot begin loading data, even using a Block Clear command, until the Mirror Settle Time is satisfied.

A shorter effective display time can be achieved by loading a a subset of blocks during the Mirror Settle Time of another subset of blocks. This can be done in a cascading fashion down the surface of the DMD until the entire image has been briefly displayed. The result is that the Mirror Settle Time is allowed to occur or while other blocks are loading. This in effect removes the Mirror Settle time from time it takes to display one binary frame.

This operation is analogous to the way a focal plane shutter works in a modern SLR camera to achieve very high shutter speeds.

NOTE: In 2xLVDS parts the load time of one block is shorter than the required Mirror Settle time. Therefore in practice, two consecutive blocks are loaded before returning to clear the initial block.

4.3.2 How it is Done

A phased operation uses both block operations (Reset and Block Clear) to achieve very short effective display times.

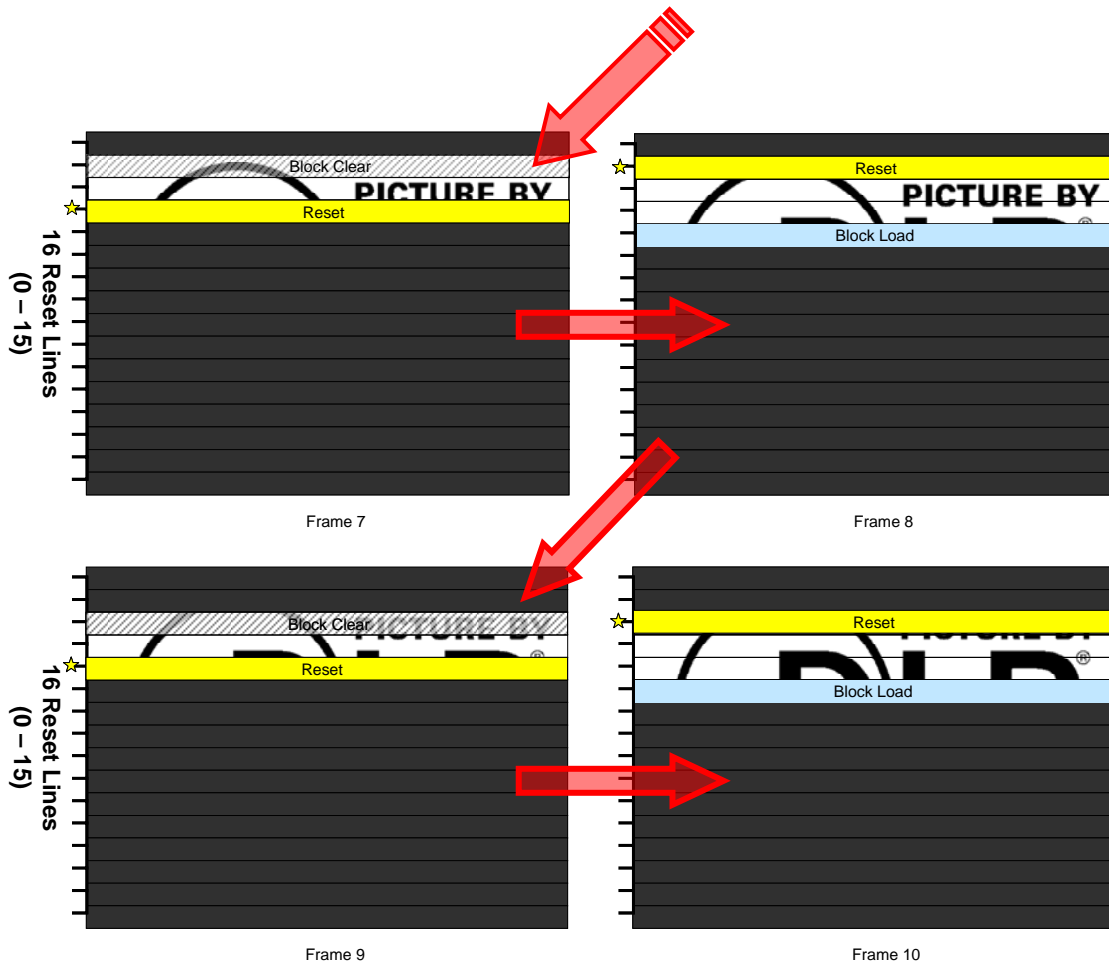Several steps of a phased reset operation for a 2xLVDS part are illustrated here:

Frame 1

Frame 2

Frame 3

Frame 4

Frame 5

Frame 6
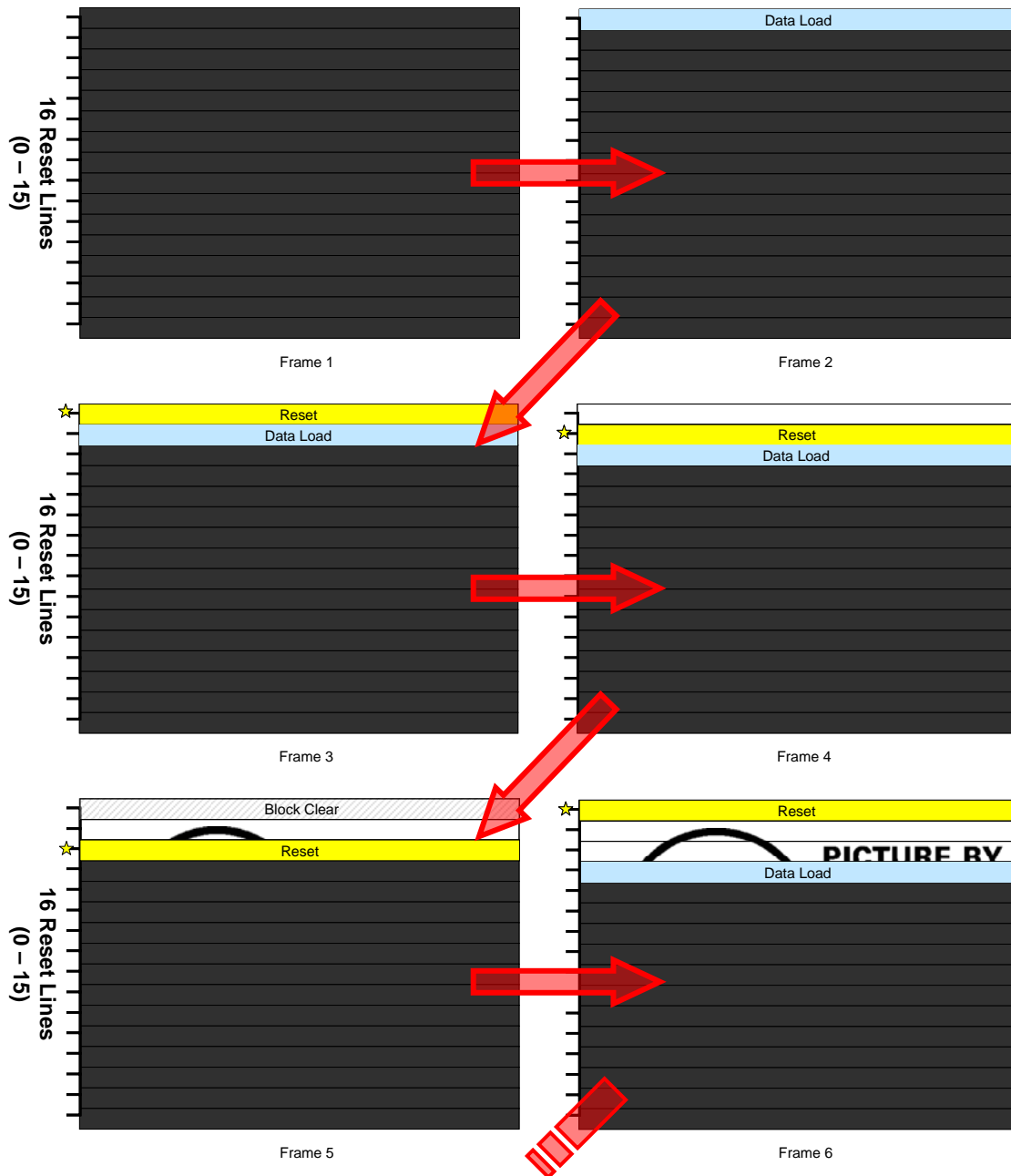
Figure 12 – Phased Reset Sequence

In this sequence a "window" of two displayed blocks will sweep down the surface of the DMD. The image is effectively displayed for the time that it takes to load two blocks. When the bottom of the DMD is reached the next frame of data can begin a sweep immediately since the blocks at the top of the DMD have already satisfied the Mirror Settle Time.