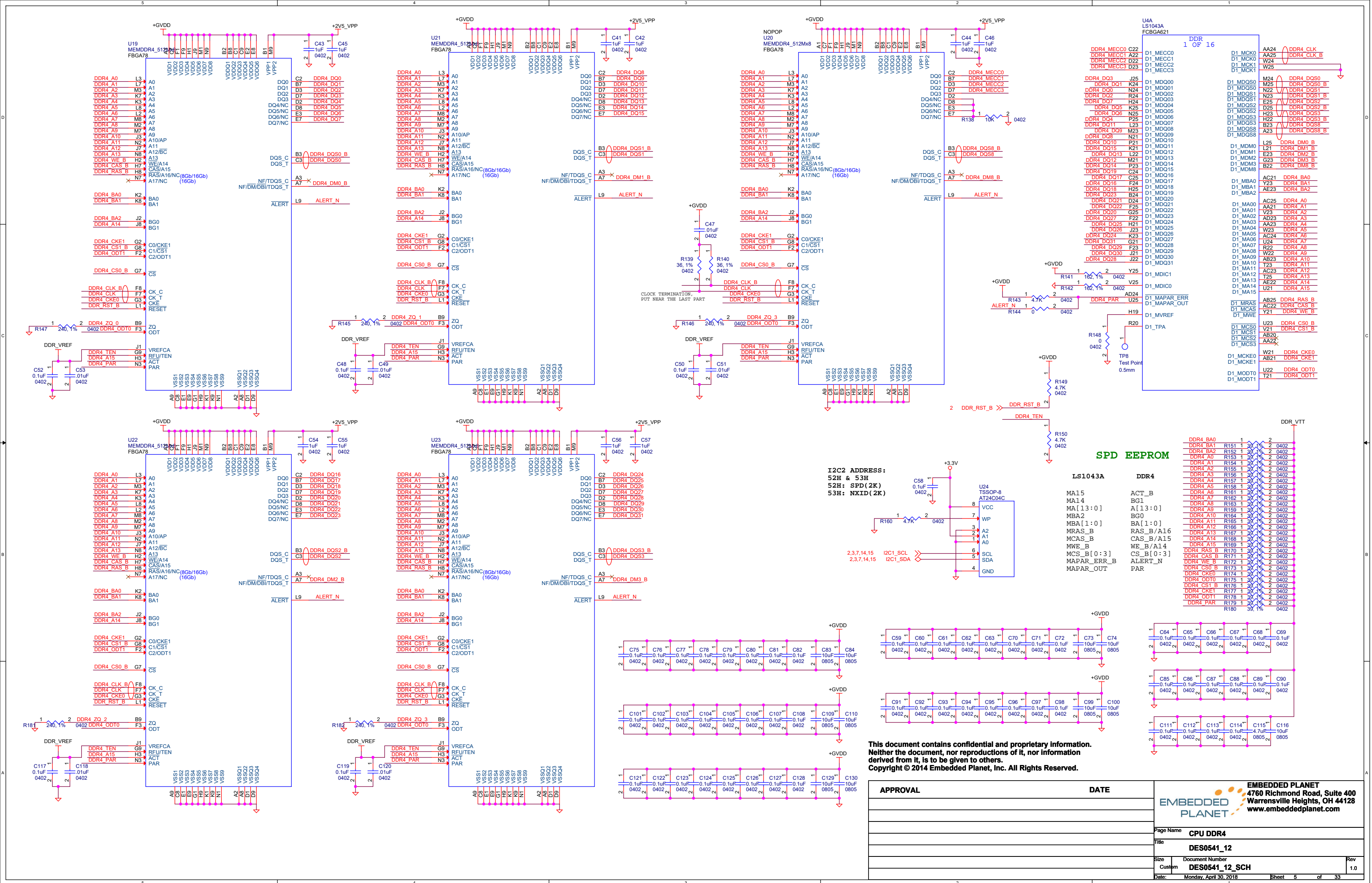
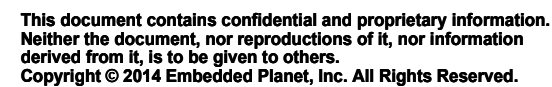



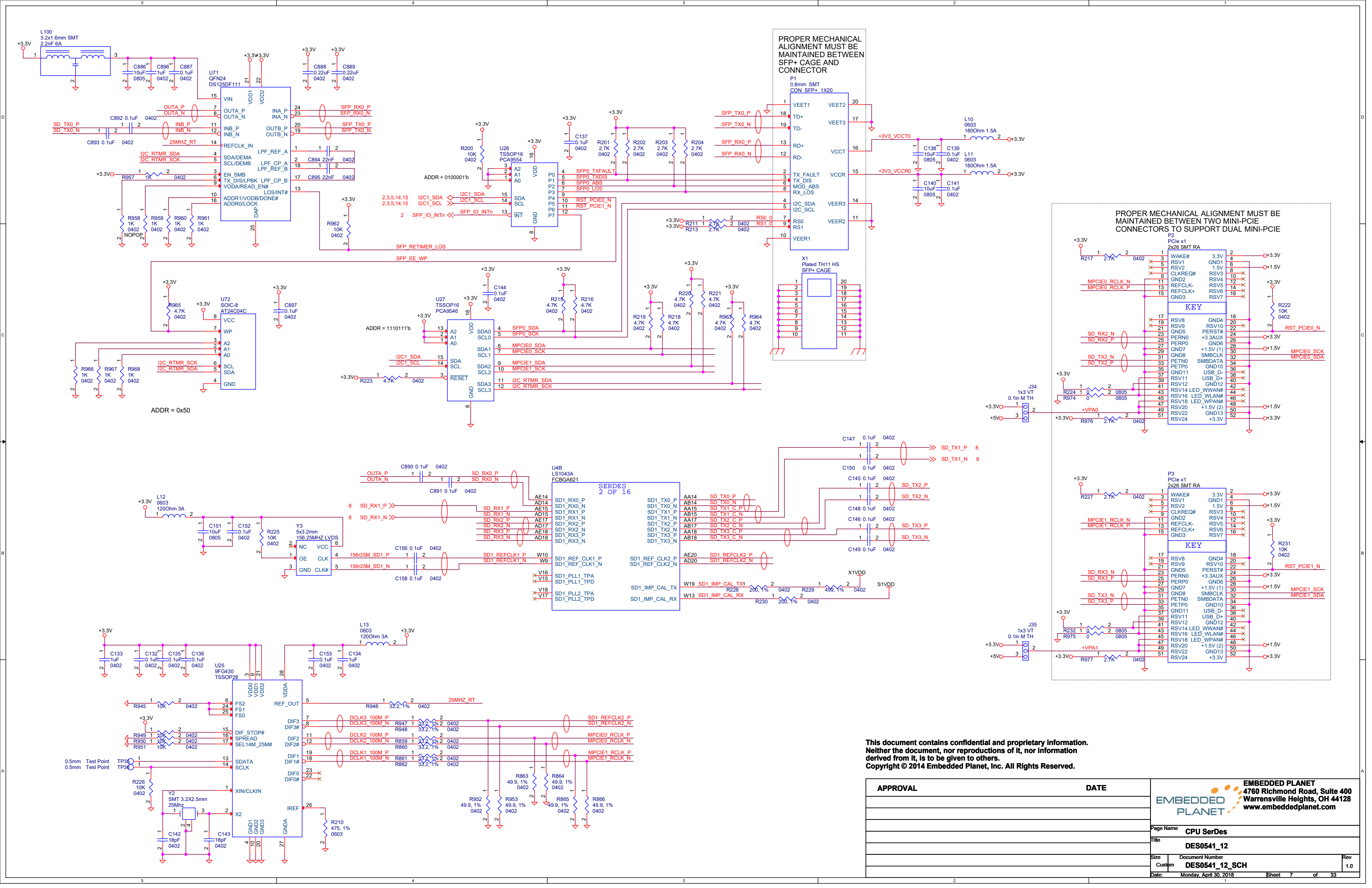


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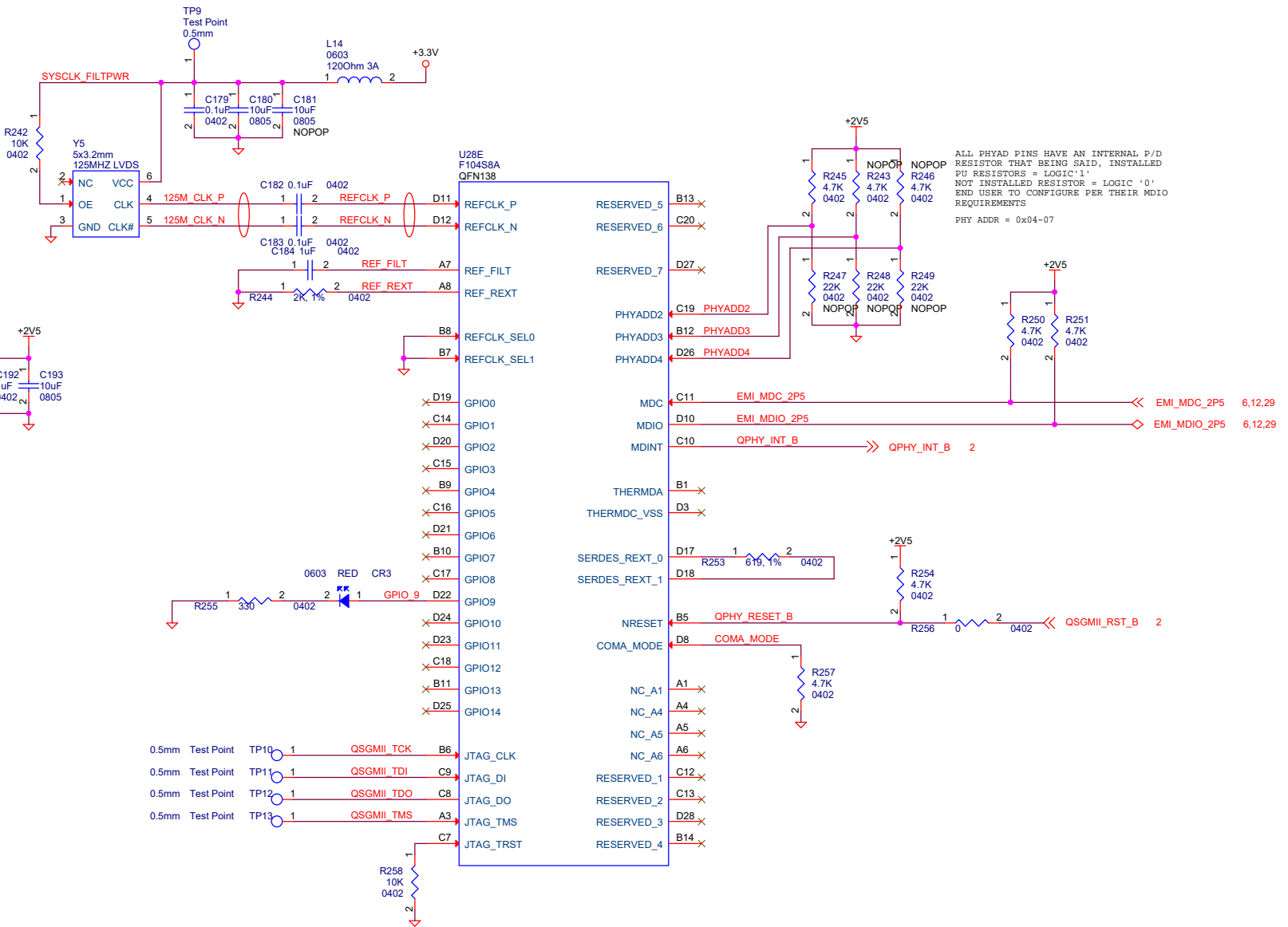
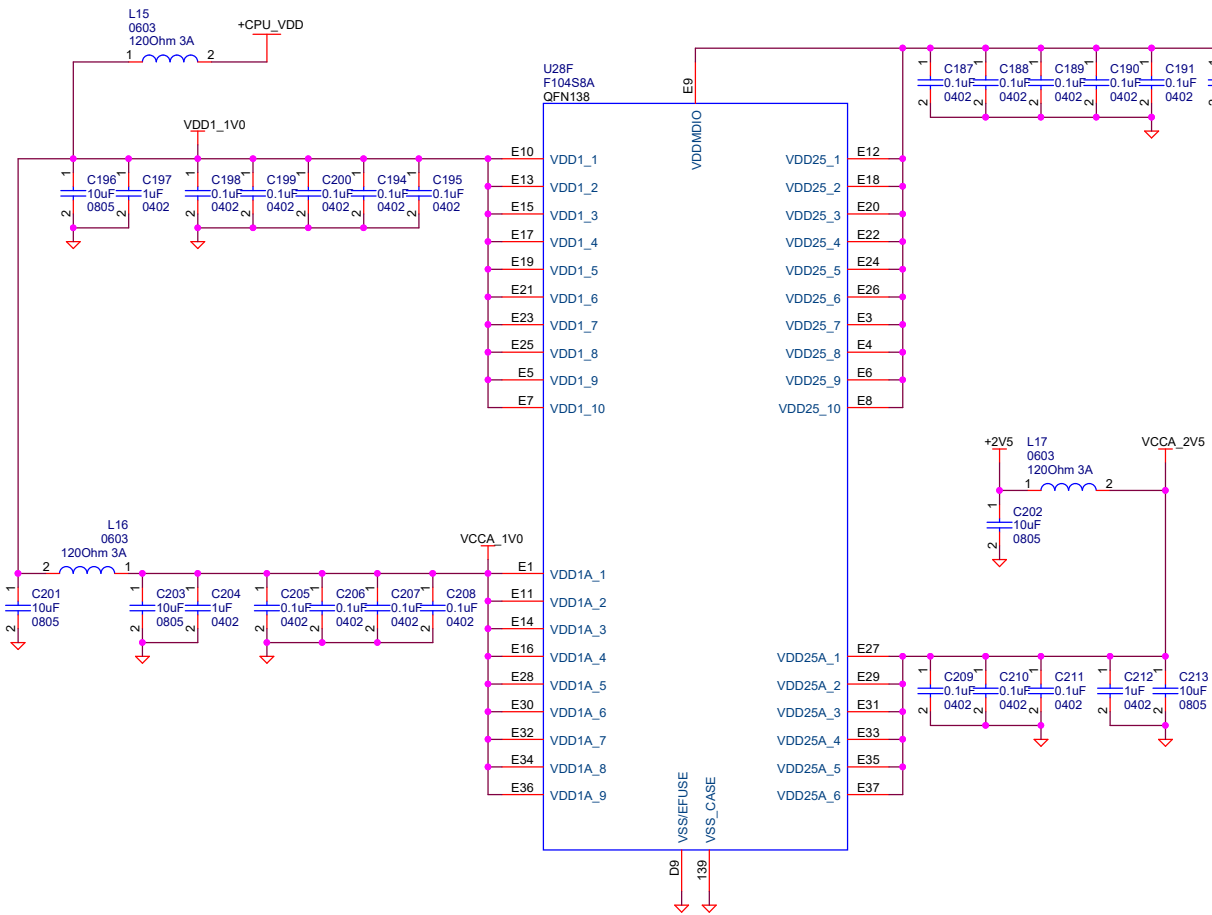




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		Page Name CPU RGMII		
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QSGMII CONFIG & POWER

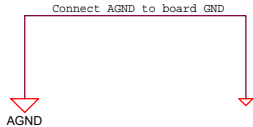
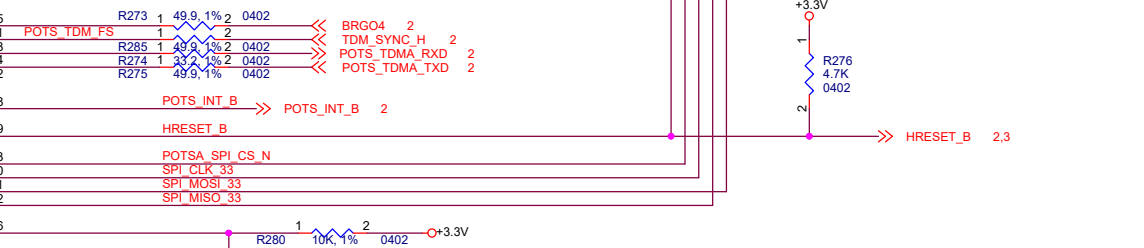
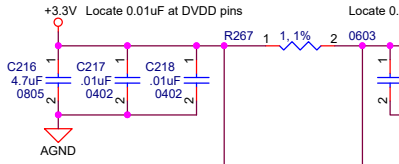
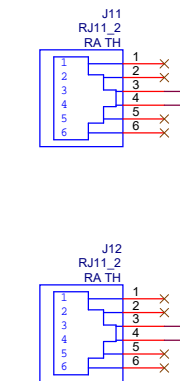



Approx. Power Budget	

Power Supply	Current
VDD1	800 mA
VDD1A	400 mA
VDD25	200 mA
VDD25A	600 mA
VDDMDIO	25 mA

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		Page Name	SLIC I/F	
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CSW1 = 220uF 10V
L1 = 22uH 2A
RC1 = 0ohm

VSW = 12V (10V - 14V)

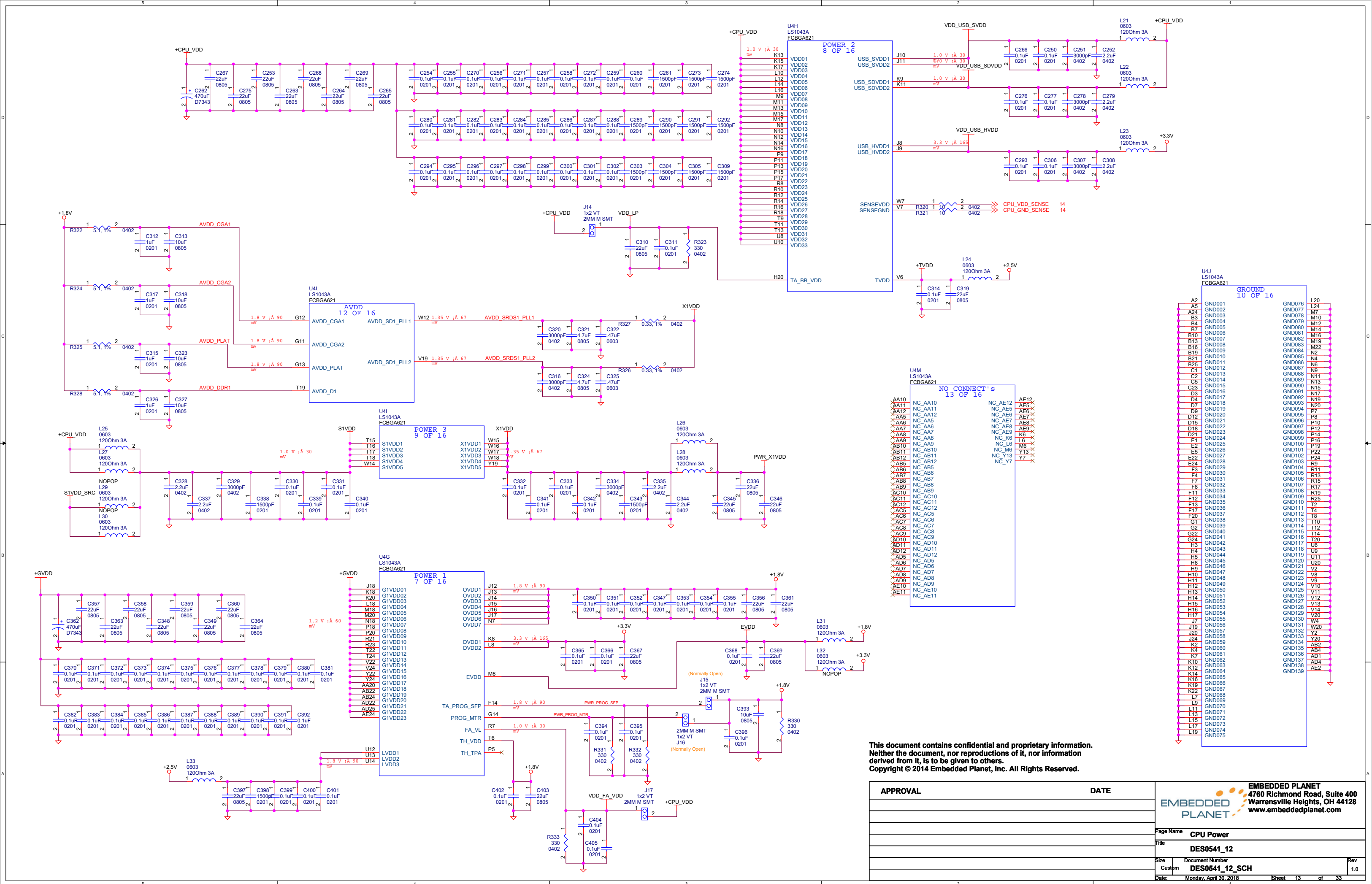


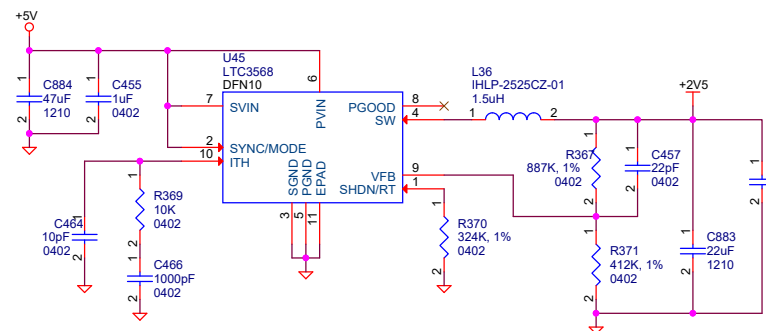
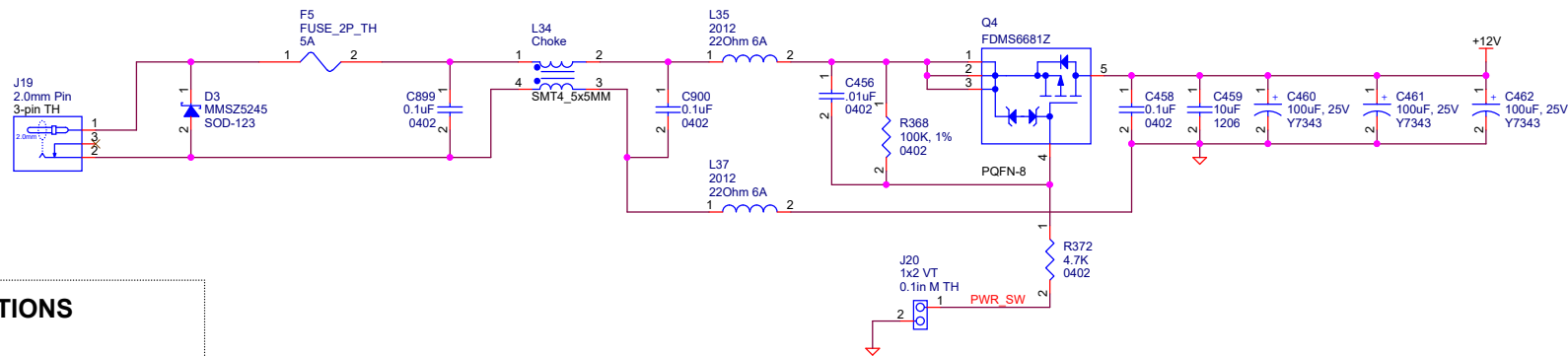
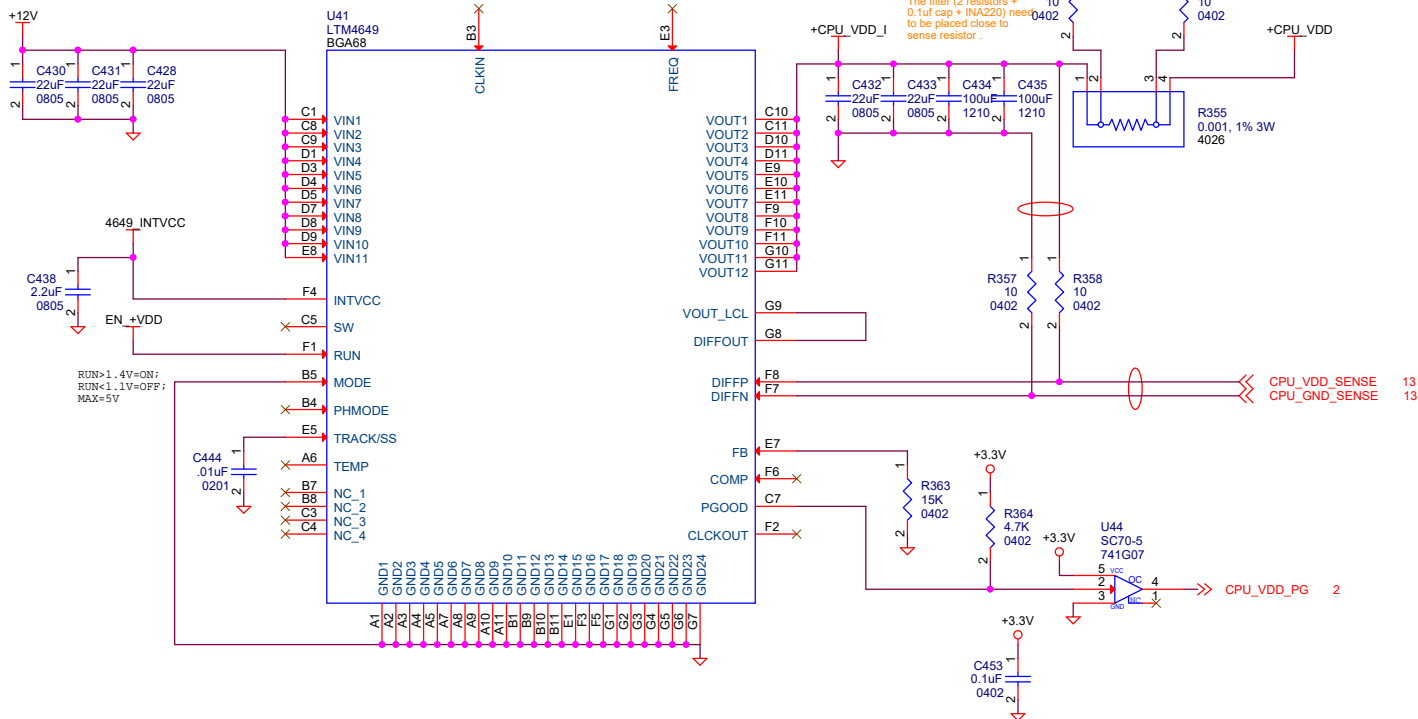
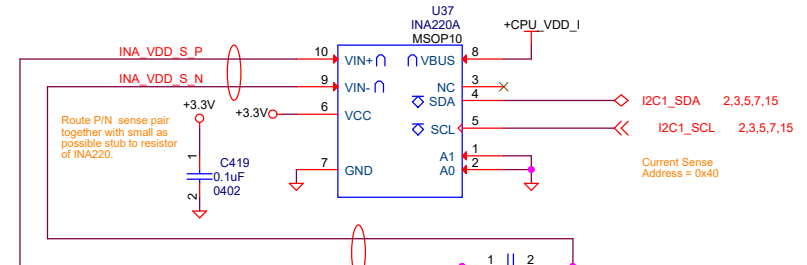
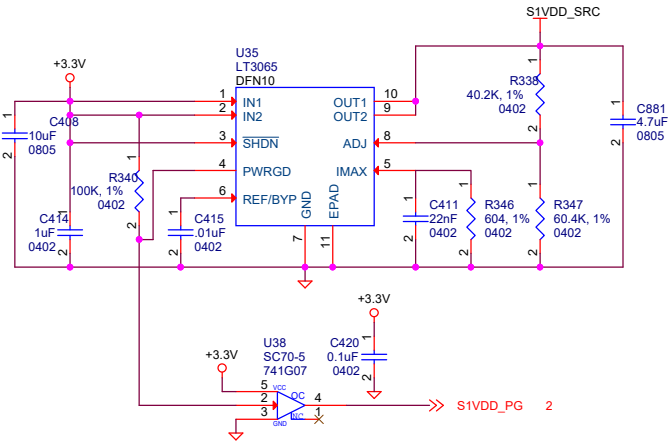
ZTTP2014/ZX5T955/FZT955 Vce=140V SOT223 or SOT89


2) For 60Vrms ringing applications must be 100V Vce rated, ZXTP2013G. C241 should be 63V min.
For 50Vrms ringing Vce can be 60V rated, ZXTP2012G. C241 can be 50V rated.

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The top level schematic shows the board layout with power planes (green for GND, red for +1.8V, blue for +2.5V, and yellow for +12V). It includes two power modules: a +2.5V module (NOPOP L20, 3.2x1.6mm SMT, 2.2nF 6A) and a +1.8V module (NOPOP L19, 3.2x1.6mm SMT, 2.2nF 6A). The board features several connectors and pins: DC_IN, 2_5V_FROM_VX585, 1_8V_LS1043A, RGMII_INT_N, SPI1_CLK_18, SPI1_MOSI_18, SPI1_MISO_18, SPI1_CS1_18, SPI1_SLVCS_18, and RGMII_PHY_CLK_25. The schematic also shows the internal connections between the modules and the board, including the power planes and the various components.






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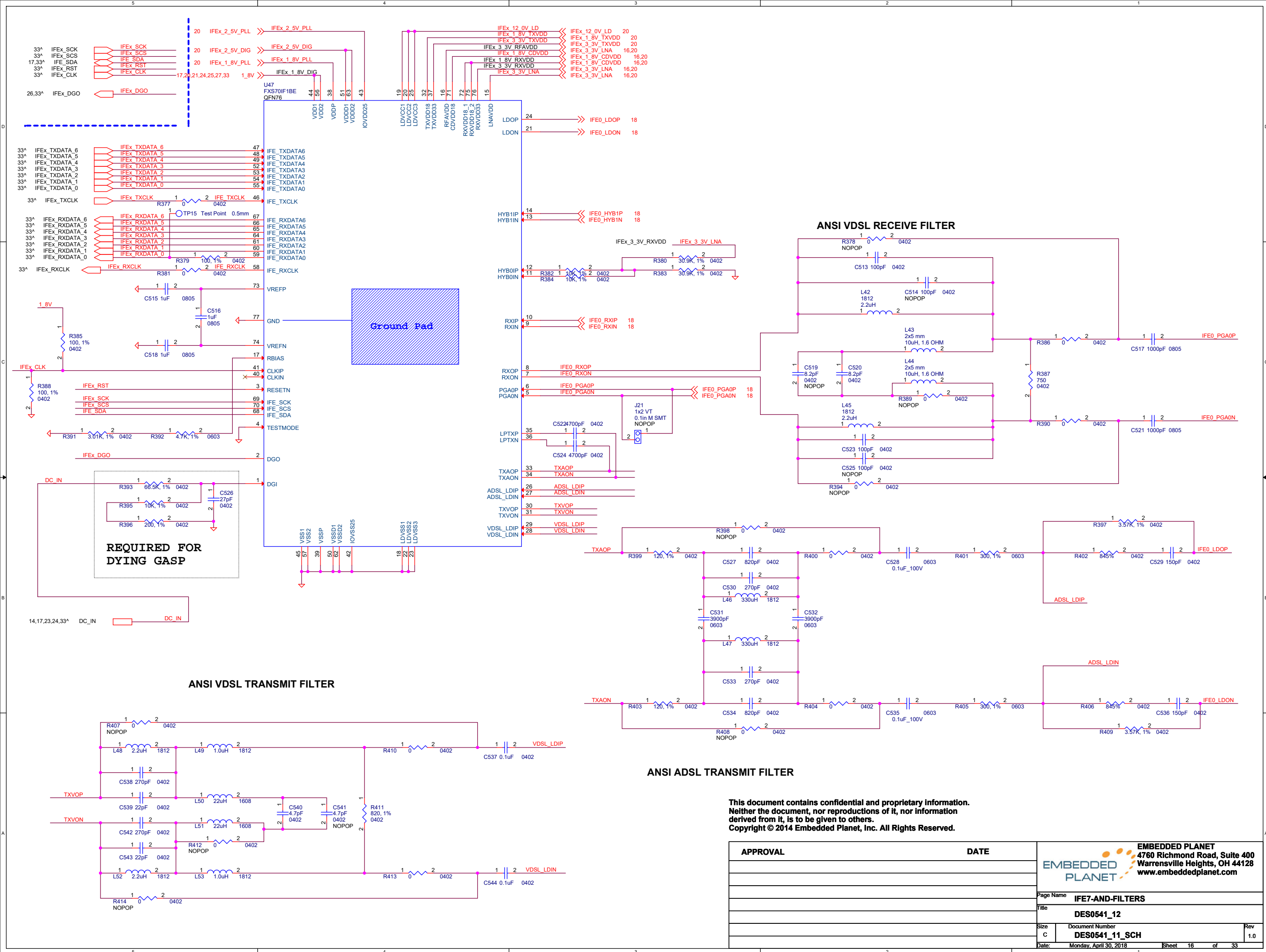
The schematic diagram illustrates the LDO outputs of the MC34VR500V4 QFN56. The internal LDOs (LD01-LD05) are connected to various power rails. The output voltages and currents for each LDO are as follows:

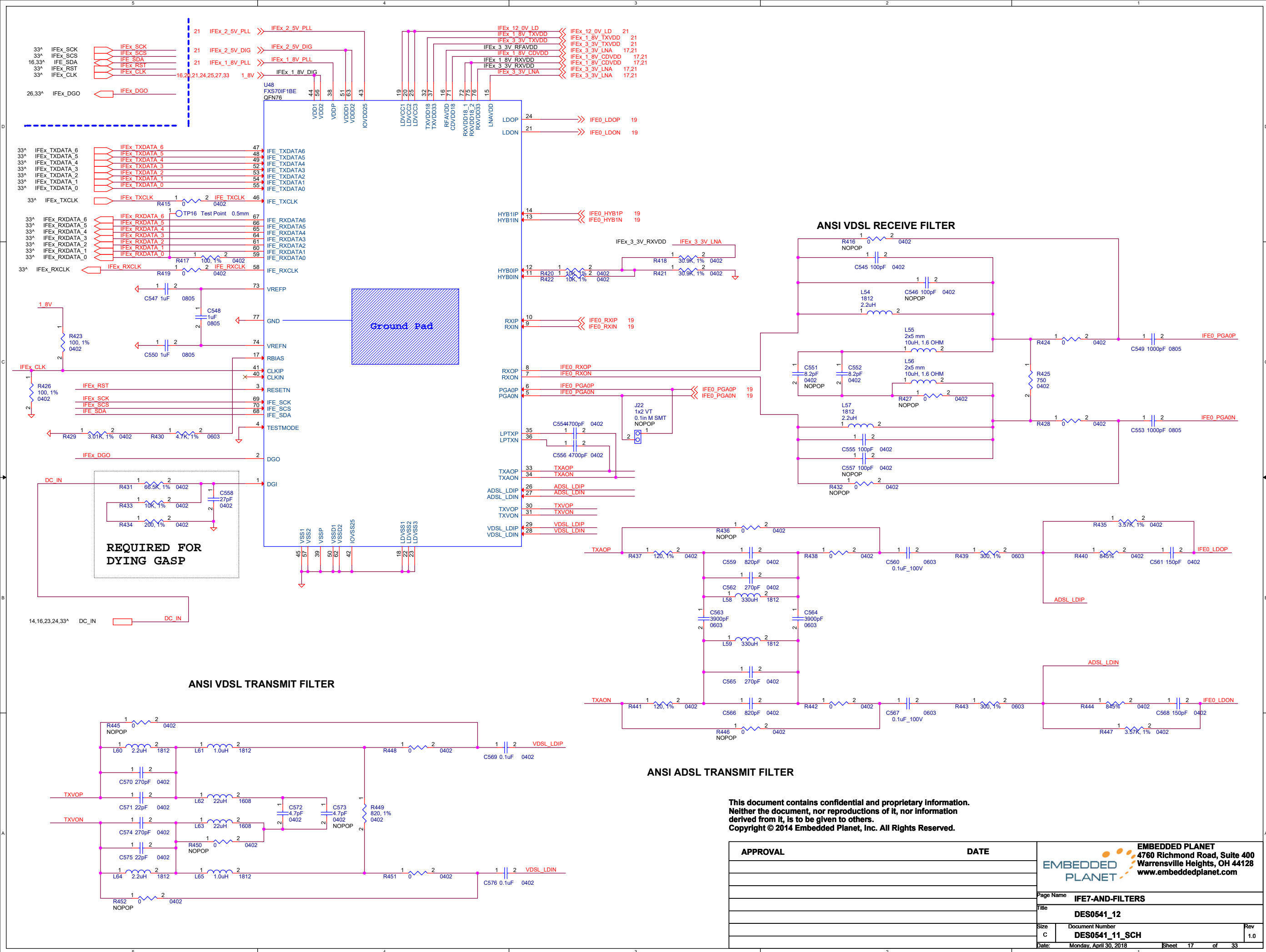
- LD01: 1.35V, 200mA
- LD02: 2.5V, 100mA
- LD03: 2.5V, 350mA
- LD04: 1.8V, 100mA
- LD05: 3.3V, 250mA

The diagram also shows the connections for the VREF, GVDD, and PMIC_VHALF pins. The output of the LDOs is connected to the PWR_X1VDD pin, which is labeled with a current of 250mA. The output of the LDOs is also connected to the EN_VDD pin, which is labeled with a current of 100mA. The output of the LDOs is also connected to the BAKUP1 and BAKUP2 pins, which are labeled with currents of 350mA and 100mA respectively. The output of the LDOs is also connected to the +2V5_VPP pin, which is labeled with a current of 100mA. The output of the LDOs is also connected to the +3.3V pin, which is labeled with a current of 200mA. The output of the LDOs is also connected to the +1.8V pin, which is labeled with a current of 100mA. The output of the LDOs is also connected to the +2.5V pin, which is labeled with a current of 350mA. The output of the LDOs is also connected to the +1.35V pin, which is labeled with a current of 200mA. The output of the LDOs is also connected to the +3.3V pin, which is labeled with a current of 200mA. The output of the LDOs is also connected to the +1.8V pin, which is labeled with a current of 100mA. The output of the LDOs is also connected to the +2.5V pin, which is labeled with a current of 350mA. The output of the LDOs is also connected to the +1.35V pin, which is labeled with a current of 200mA.

[illegible]

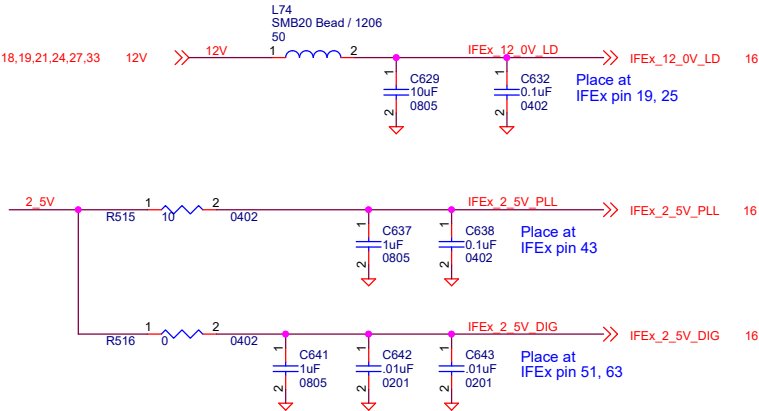
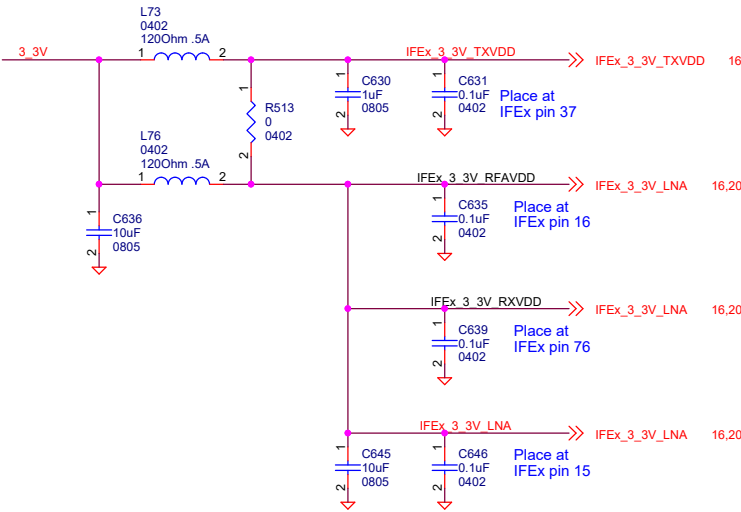
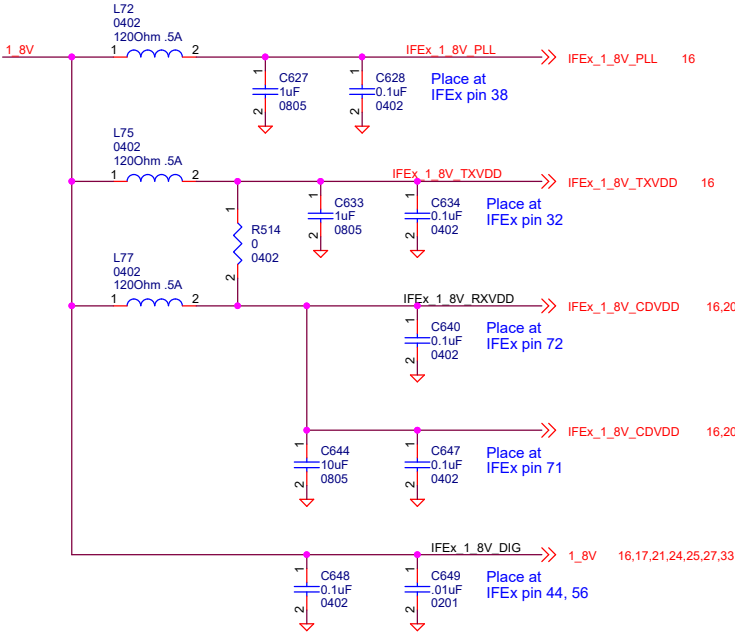
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Power Input

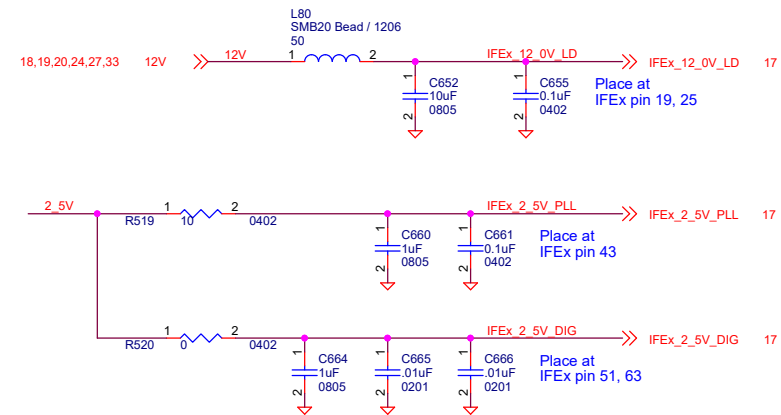
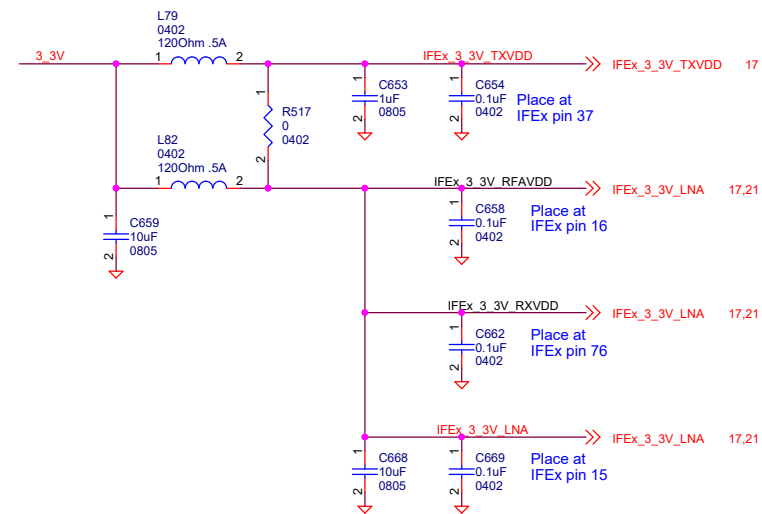
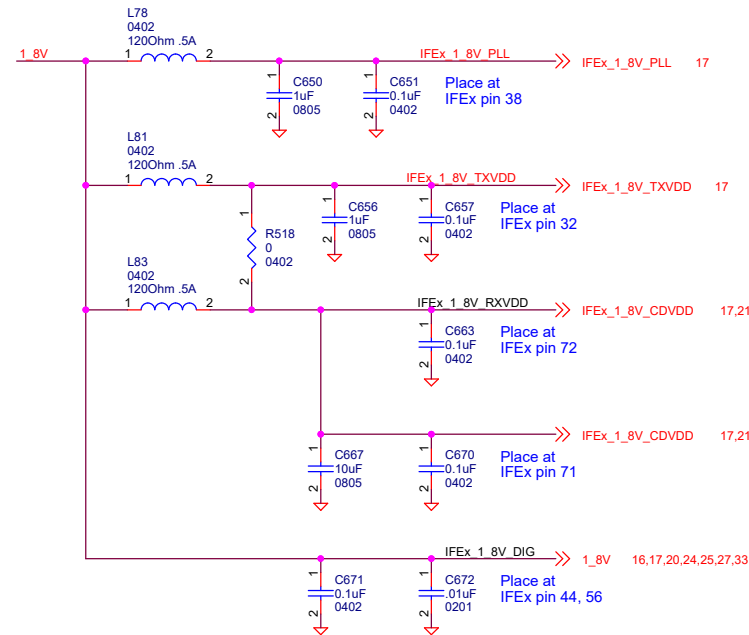
21,23,24,25,26,27,30,31,32,33^	3_3V	<div></div>	3_3V
21,25,26,27,29,31,33^	2_5V	<div></div>	2_5V
16,17,21,24,25,27,33^	1_8V	<div></div>	1_8V




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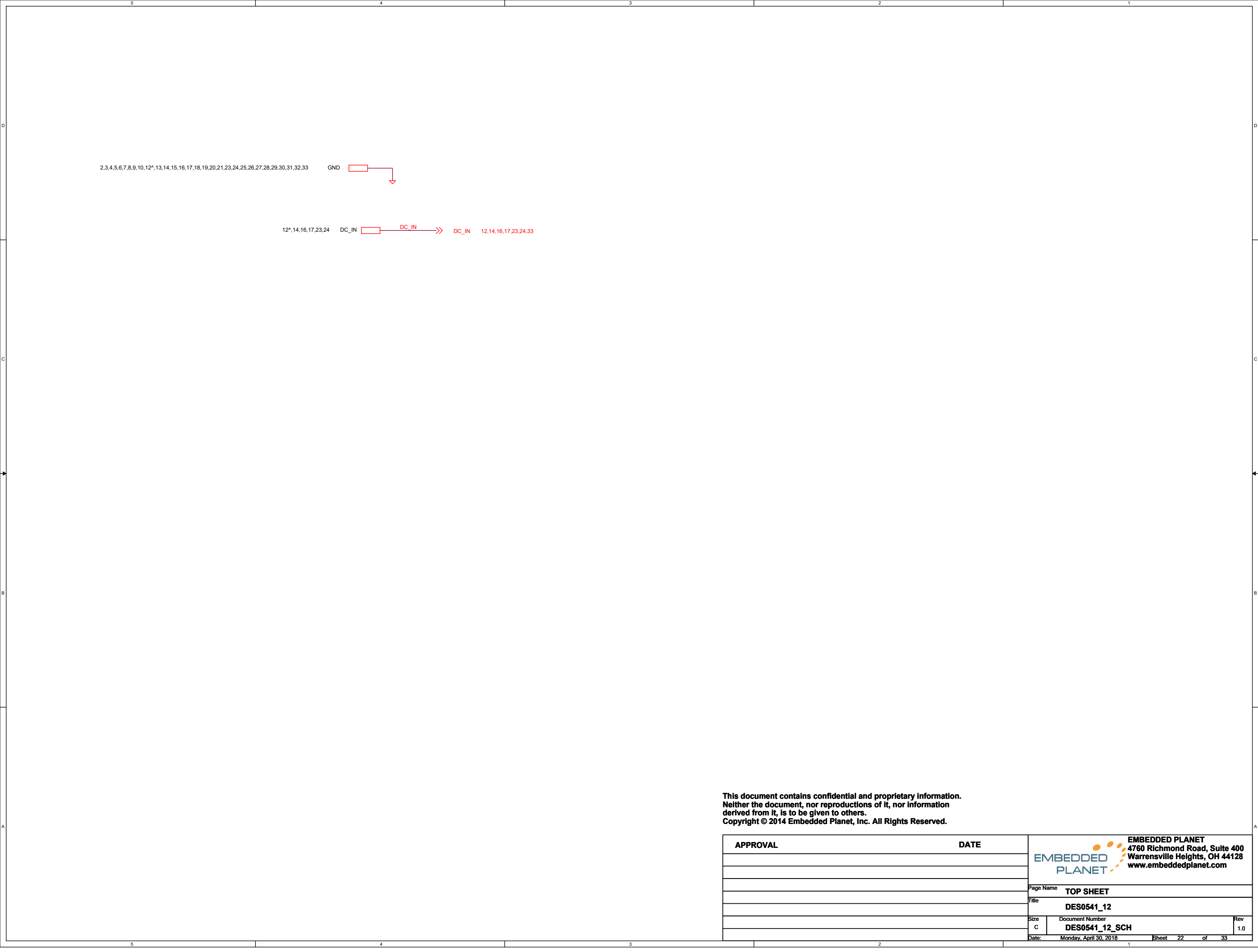
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				Page Name	
				POWER	
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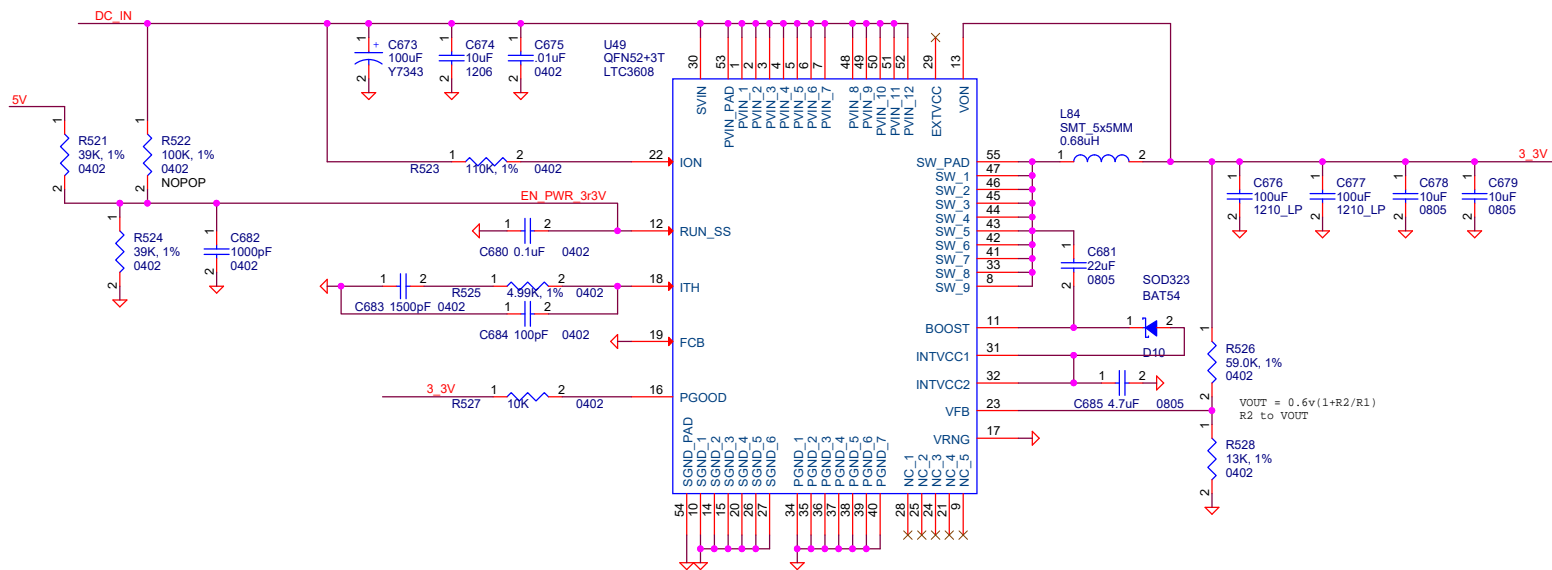
Power Input




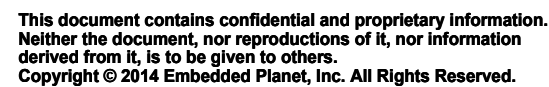
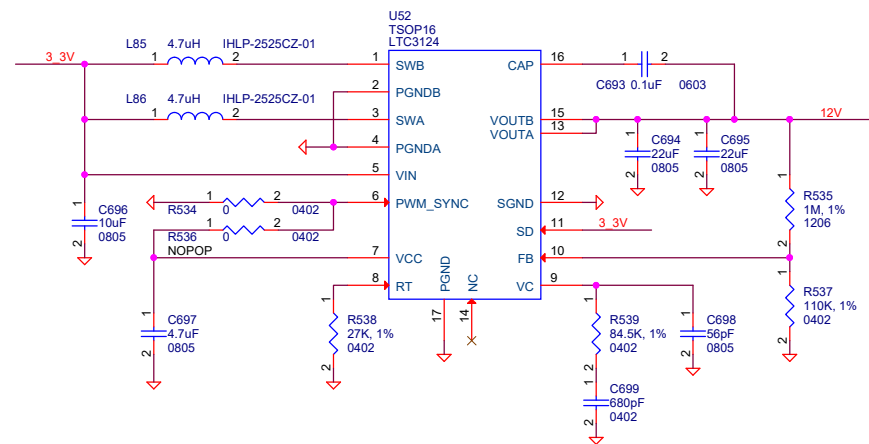
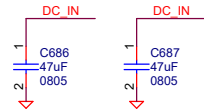
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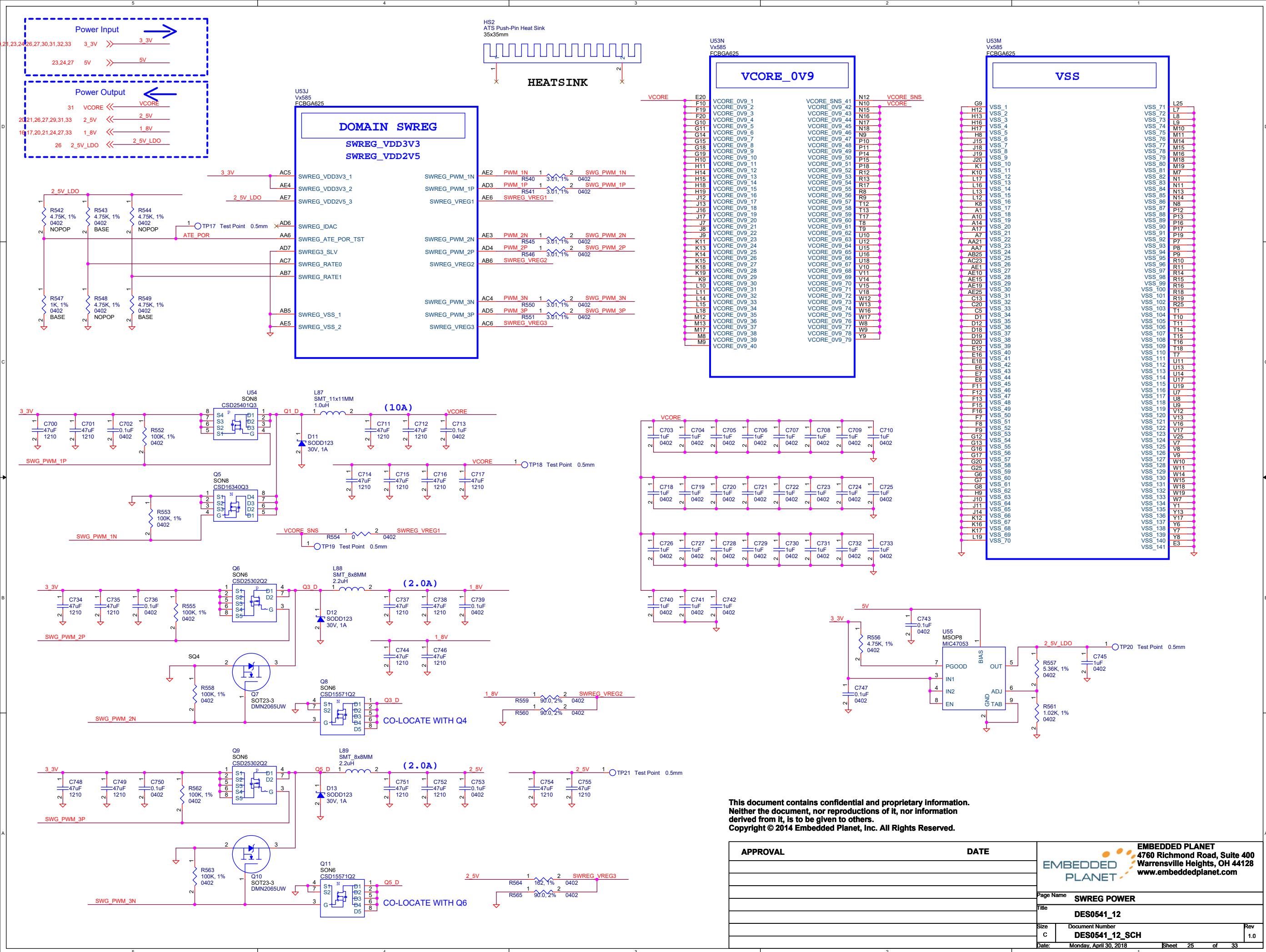




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		Page Name EXTERNAL 3.3V POWER		
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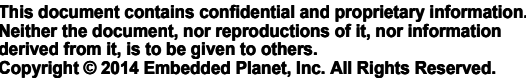
Page Name


GPIO, CLK

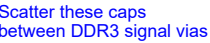
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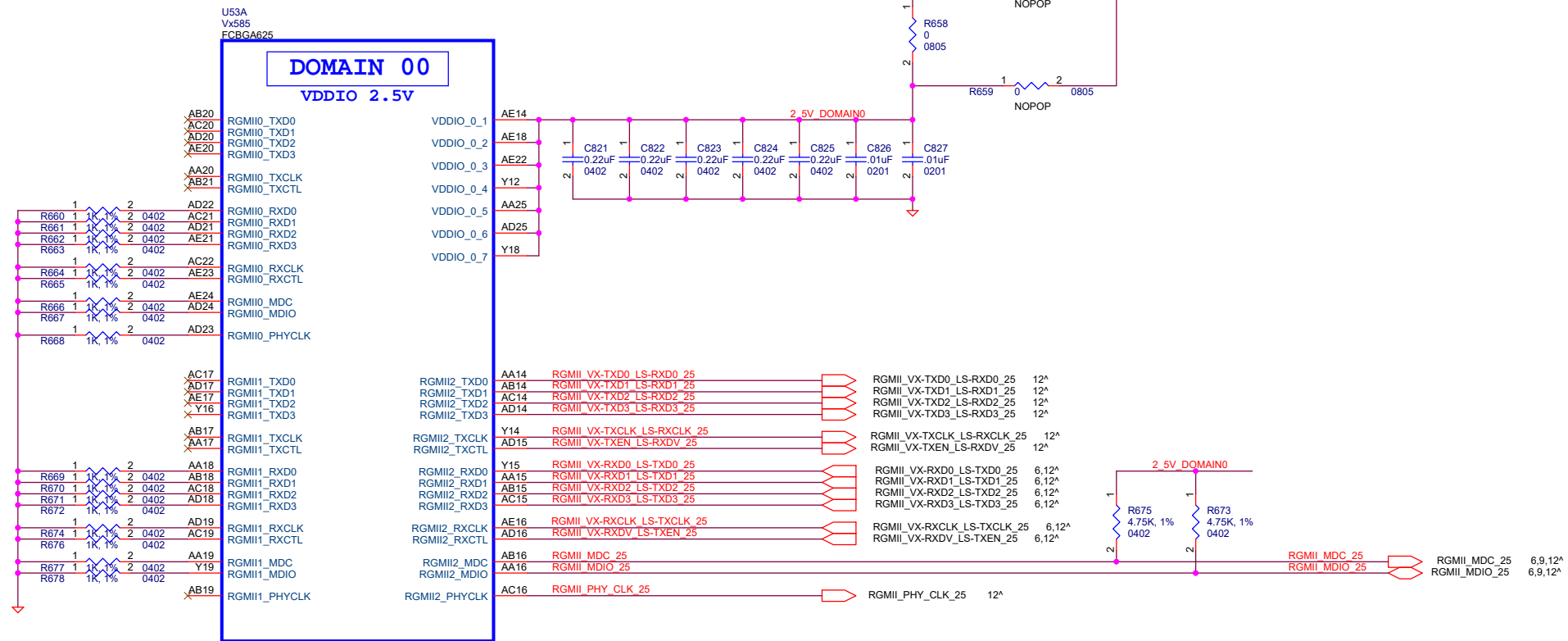
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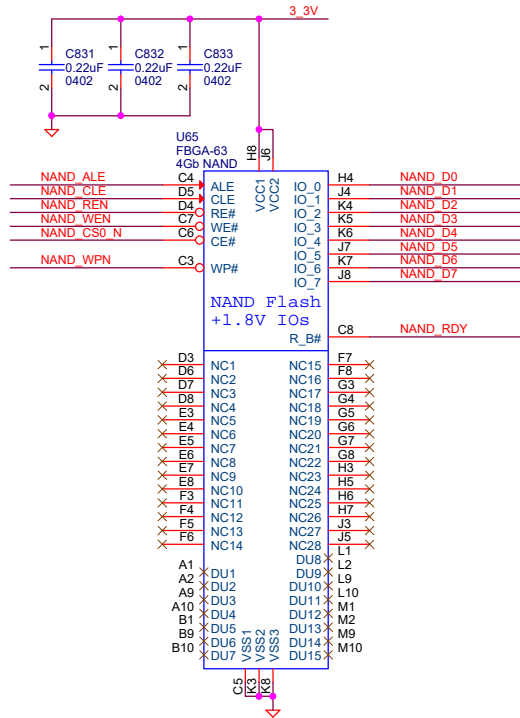
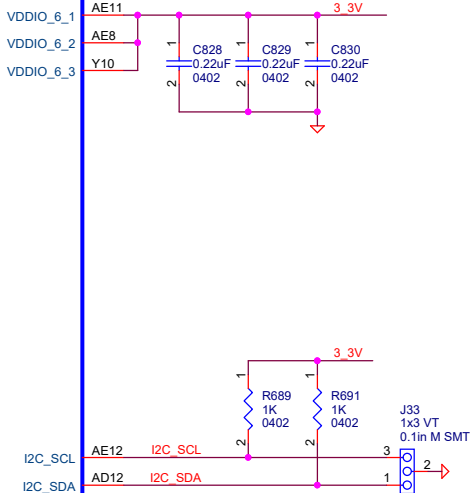
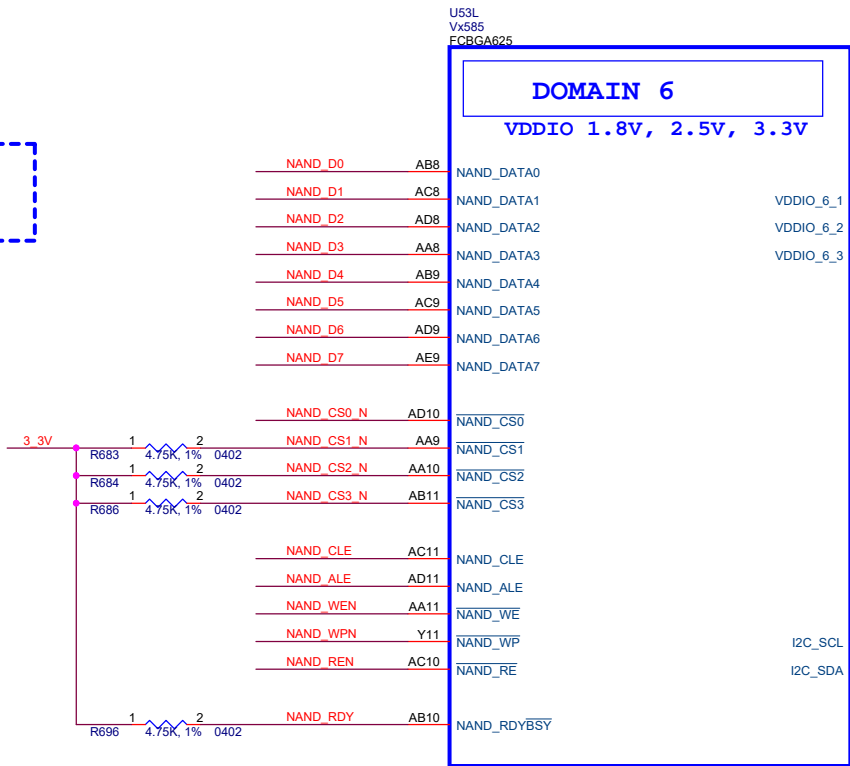
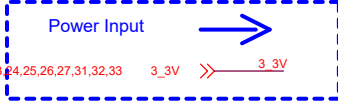
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	Page Name	JTAG,SERIAL			
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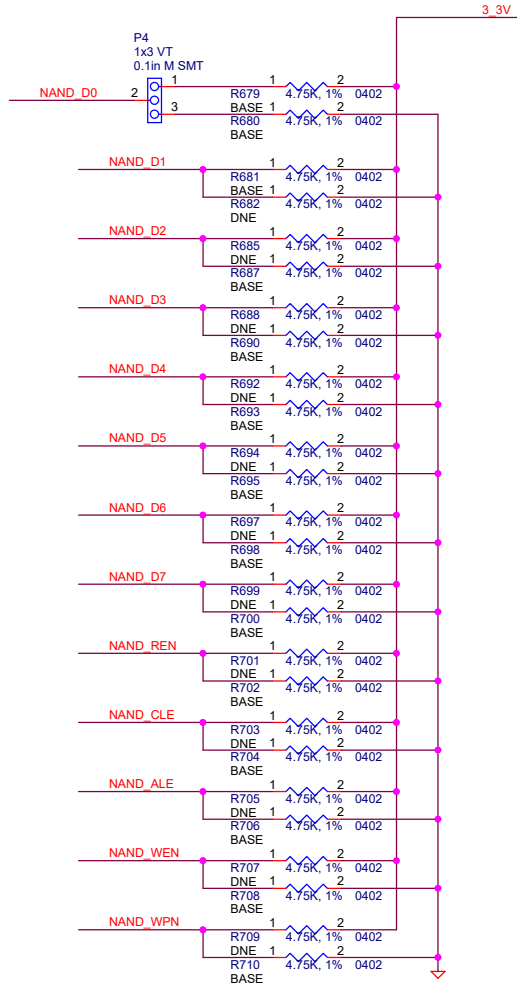
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Page Name	DDR3
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Page Name		ETHERNET INTERFACE	
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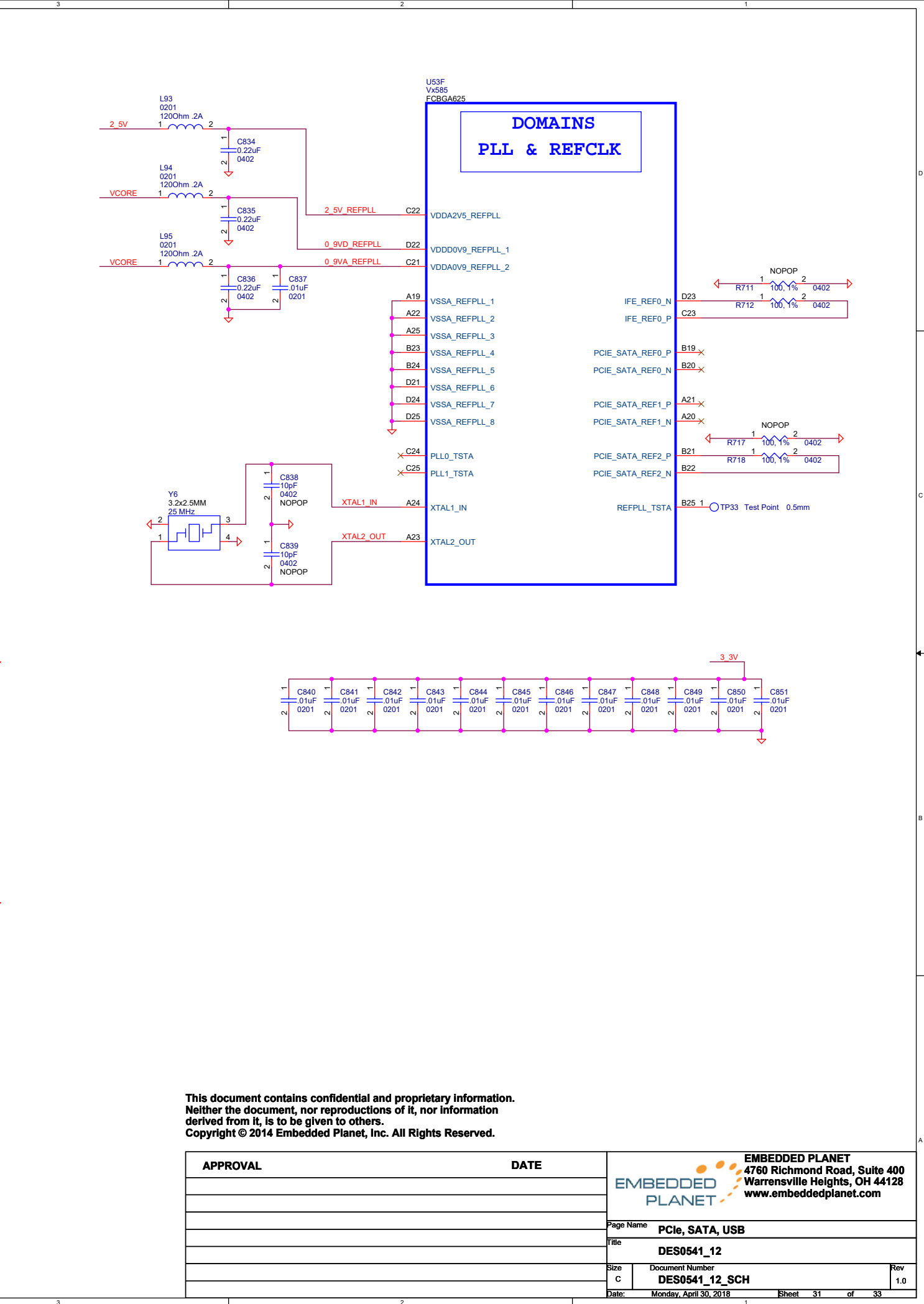
P6 NOTE:
NAND BOOT MODE: JS6 on pins 2 & 3
SERIAL BOOT MODE: JS6 on pins 1 & 2




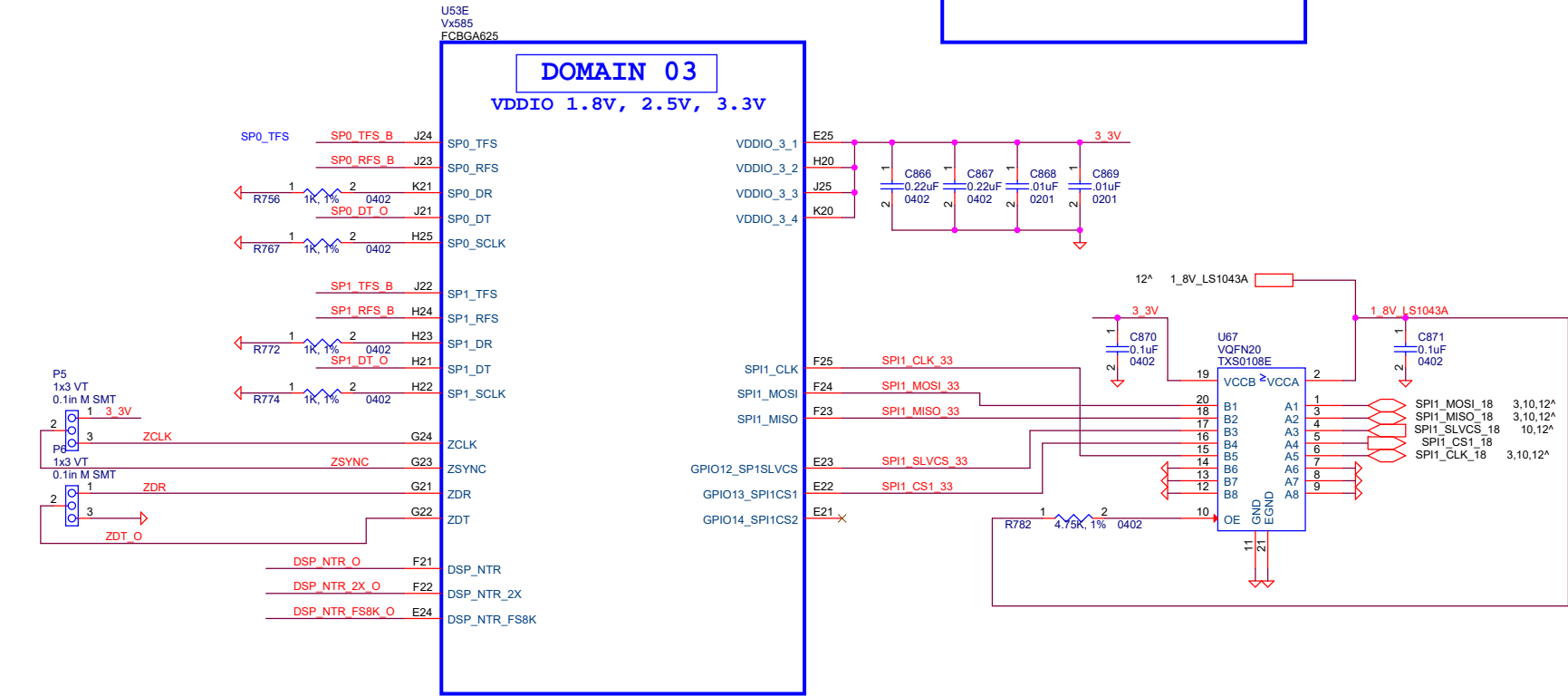
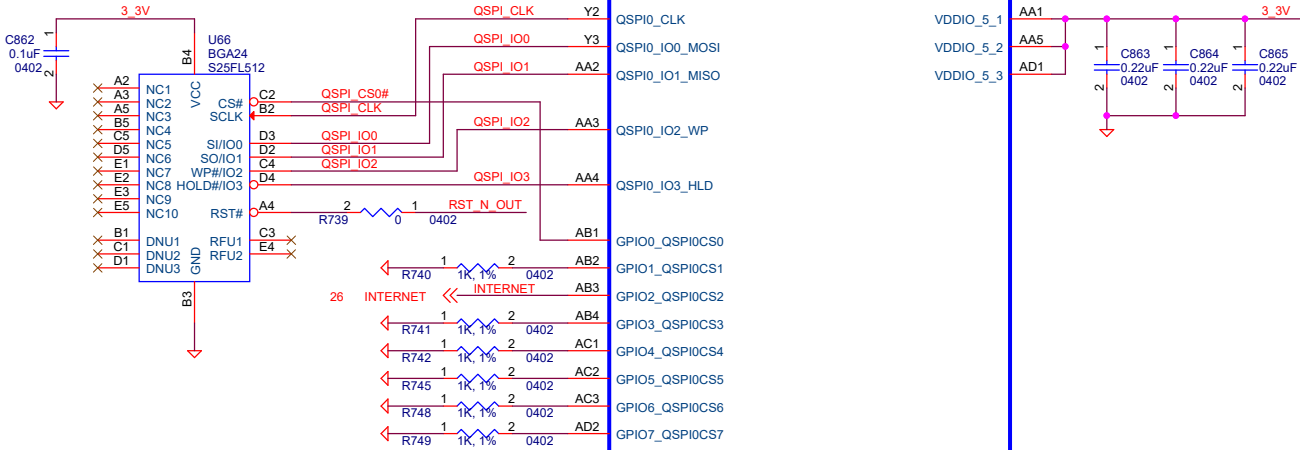
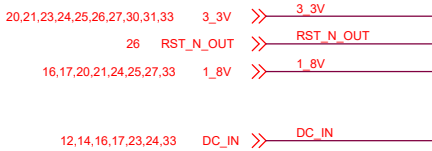
Signal Name	Latch on Reset	Description	Default
NAND_D0	BOOT_MODE[0]	Boot strap pins: 000 Reserved 001 QSPI boot mode 010 NAND boot mode (Default) 011 Serial port (9600 baud) 100 Reserved 101 QSPI boot mode (LSB) 110 Reserved 111 Serial port (38400 baud)	PD
NAND_D1	BOOT_MODE[1]		PU
NAND_D2	BOOT_MODE[2]		PD
NAND_D3	Reserved		
NAND_D4	Reserved	Reserved	
NAND_D5	Reserved		
NAND_D6	Reserved	Reserved	
NAND_D7	Reserved		
NAND_REN	Reserved	Reserved	
NAND_CLE	Reserved	Reserved	
NAND_ALE	Reserved	Reserved	
NAND_WEN	Reserved	Reserved	
NAND_WPN	Reserved	Reserved	

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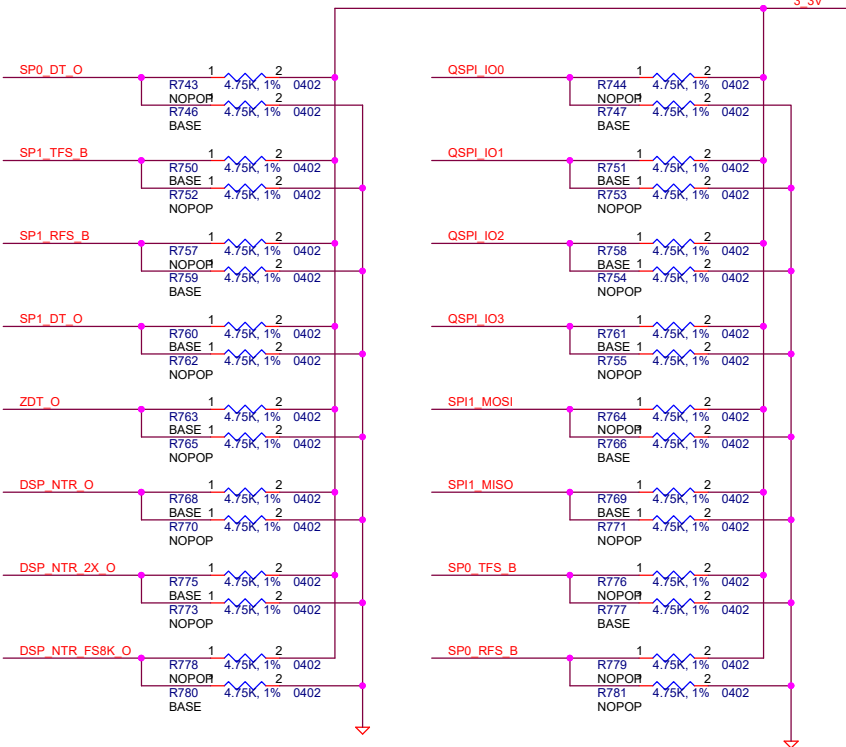
APPROVAL	DATE	 EMBEDDED PLANET 4760 Richmond Road, Suite 400 Warrensville Heights, OH 44128 www.embeddedplanet.com	
		Page Name NAND	
		Title DES0541_12	
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Signal Name	Latch on Reset	Description	PU Domain
QSPI_IO0_MOSI	NAND_CONFIG[0]	Memory Size: 000-64Mb 001-128Mb 010-256Mb 011-512Mb 100-1Gb 101-2Gb 110-4Gb 111-8Gb 110-4Gb (Default)	5
QSPI_IO1_MISO	NAND_CONFIG[1]	Page Size: 00-Reserved[4:3] 01-2Kb, large block (Default) 10-4KB, large block 11-Reserved	5
QSPI_IO2_WP	NAND_CONFIG[2]	Number of row address cycles (Default)	3
QSPI_IO3_HLD	NAND_CONFIG[3]		5
SPI1_MOSI	NAND_CONFIG[4]		3
SPI1_MISO	NAND_CONFIG[5]		3



Pin	Latch on Reset	Description	Power Domain
SP0_TFS	GMAC_CONFIG_0[0]	Set GIGE interface mode for the 3 GIGE ports:	3
SP0_RFS	GMAC_CONFIG_0[1]		
SP0_DT	GMAC_CONFIG_1[0]	00 - RMII 01 - RMII 10 - RGMII (Default) 11 - Reverse RGMII	
SP1_TFS	GMAC_CONFIG_1[1]		
SP1_RFS	GMAC_CONFIG_2[0]		
SP1_DT	GMAC_CONFIG_2[1]		
ZDT	ZARLINK_SILABS_SLIC_SEL	Select between 0 - Zarlink 1 - Silabs (Default) 2 - Bypass	3
DSP_NTR	RTCK_BYPASS	0 - Use RTCK for FS2 1 - Bypass RTCK for FS2 (default)	3
DSP_NTR_2X	EN_EXT_LOR	Enable board level Latch-on-reset pins: 0 - Use OTP 1 - Use Pads (default)	3
DSP_NTR_FS8K	*DEBUG*	0 - Disable (Default)	3

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