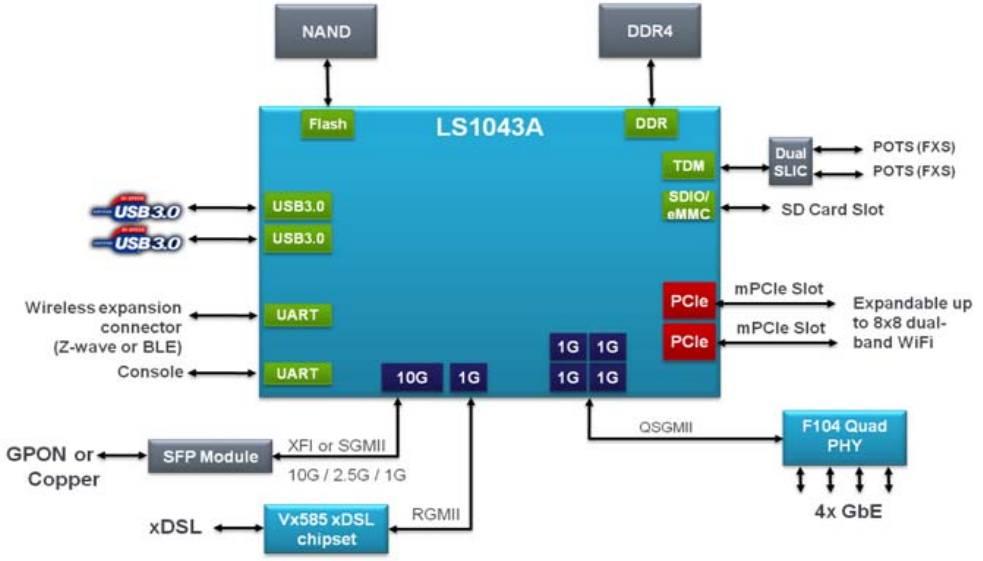

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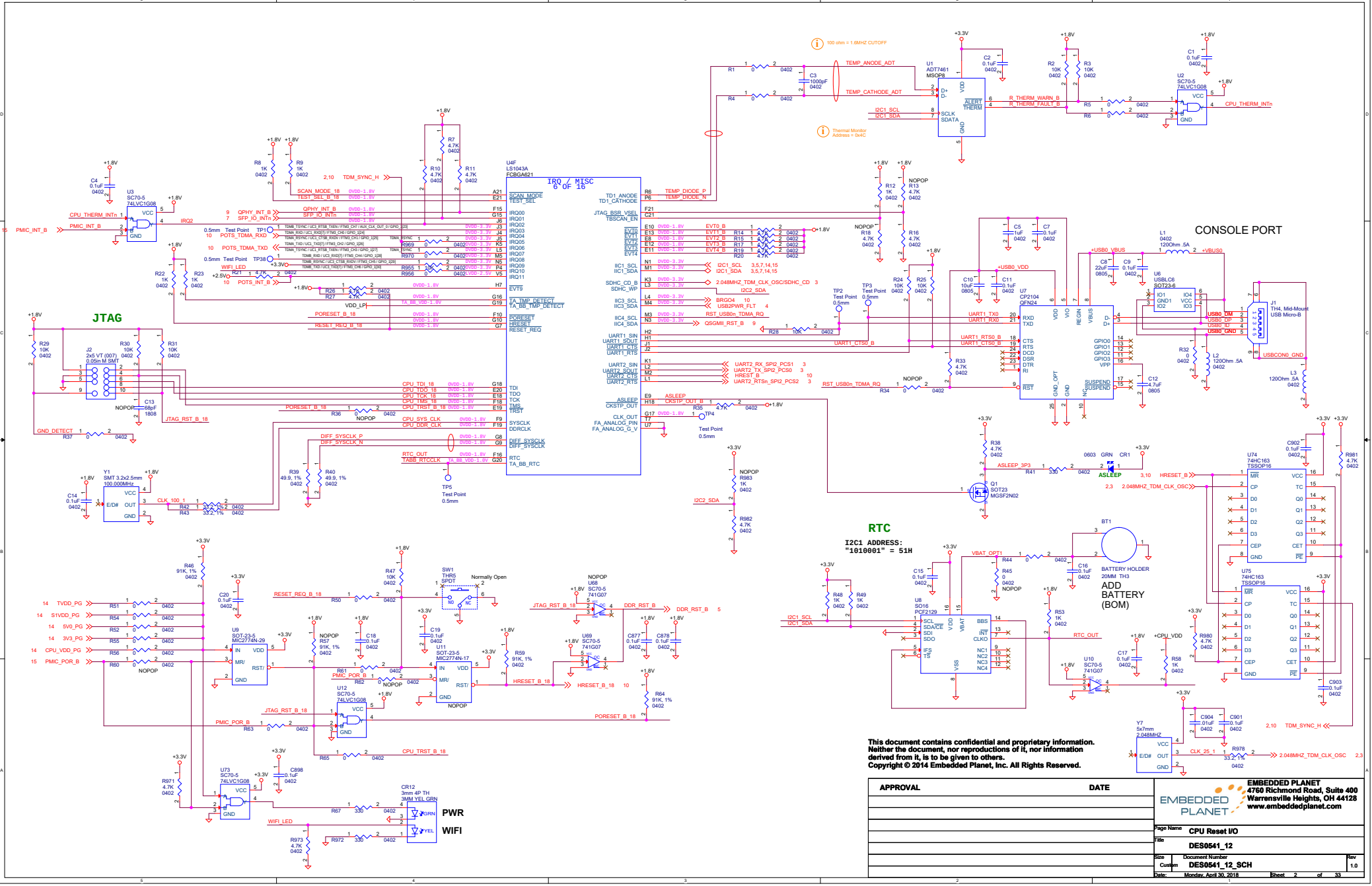
CONSOLE PORT
JTAG
RTC
I2C1 ADDRESS:
"1010001" = 51H
ADD
BATTERY
(BOM)
PWR
WIFI
IRQ / MISC
6 OF 16
U4F
LS1043A
FCBGA621
U1
ADT7461
MSOP8
U2
SC70-5
74LVC1G08
U3
SC70-5
74LVC1G08
U12
SC70-5
74LVC1G08
U73
SC70-5
74LVC1G08
U8
SOT-23-5
MIC2774N-29
U11
SOT-23-5
MIC2774N-17
U68
SC70-5
741G07
U69
SC70-5
741G07
U10
SC70-5
741G07
U6
USBLC6
SOT23-6
U7
CP2104
QFN24
U74
74HC163
TSSOP16
U75
74HC163
TSSOP16
U8
SO16
PCF2129
Q1
SOT23
MGSF2N02
J1
TH4, Mid-Mount
USB Micro-B
J2
2x5 VT (007)
0.05in M SMT
Y1
SMT 3.2x2.5mm
100.000MHz
Y7
5x7mm
2.048MHZ
BT1
BATTERY HOLDER
20MM TH3
SW1
THR5
SPDT
Normally Open
CR1
0603 GRN
CR12
3mm 4P TH
3MM YEL GRN
TEMP_ANODE_ADT
TEMP_CATHODE_ADT
I2C1_SCL
I2C1_SDA
R_THERM_WARN_B
R_THERM_FAULT_B
CPU_THERM_INTn
PMIC_INT_B
QPHY_INT_B
SFP_IO_INTn
POTS_TDMA_RXD
POTS_TDMA_TXD
WIFI_LED
POTS_INT_B
TDM_SYNC_H
SCAN_MODE_18
TEST_SEL_B_18
TEMP_DIODE_P
TEMP_DIODE_N
JTAG_BSR_VSEL
TBSCAN_EN
SDHC_CD_B
SDHC_WP
2.048MHZ_TDM_CLK_OSC/SDHC_CD
USB0_VBUS
USB0_VDD
USB0_DM
USB0_DP
USB0_ID
USB0_GND
UART1_TX0
UART1_RX0
UART1_RTS0_B
UART1_CTS0_B
RST_USB0n_TDMA_RQ
UART2_RX_SPI2_PCS1
UART2_TX_SPI2_PCS0
UART2_RTSn_SPI2_PCS2
HRESET_B
ASLEEP
ASLEEP_3P3
CPU_TDI_18
CPU_TDO_18
CPU_TCK_18
CPU_TMS_18
CPU_TRST_B_18
CPU_SYS_CLK
CPU_DDR_CLK
PORESET_B_18
JTAG_RST_B_18
DIFF_SYSCLK_P
DIFF_SYSCLK_N
RTC_OUT
TABS_RTCCLK
CLK_100_1
GND_DETECT
TVDD_PG
S1VDD_PG
5V0_PG
3V3_PG
CPU_VDD_PG
PMIC_POR_B
RESET_REQ_B_18
DDR_RST_B
HRESET_B_18
PORESET_B_18
CPU_TRST_B_18
VBAT_OPT1
RTC_OUT
+CPU_VDD
CLK_25_1
2.048MHZ_TDM_CLK_OSC
TDM_SYNC_H
I2C2_SDA
USBCON0_GND
100 ohm = 1.6MHZ CUTOFF
Thermal Monitor
Address = 0x4C
Test Point
0.5mm
NOPOP
GND_OPT
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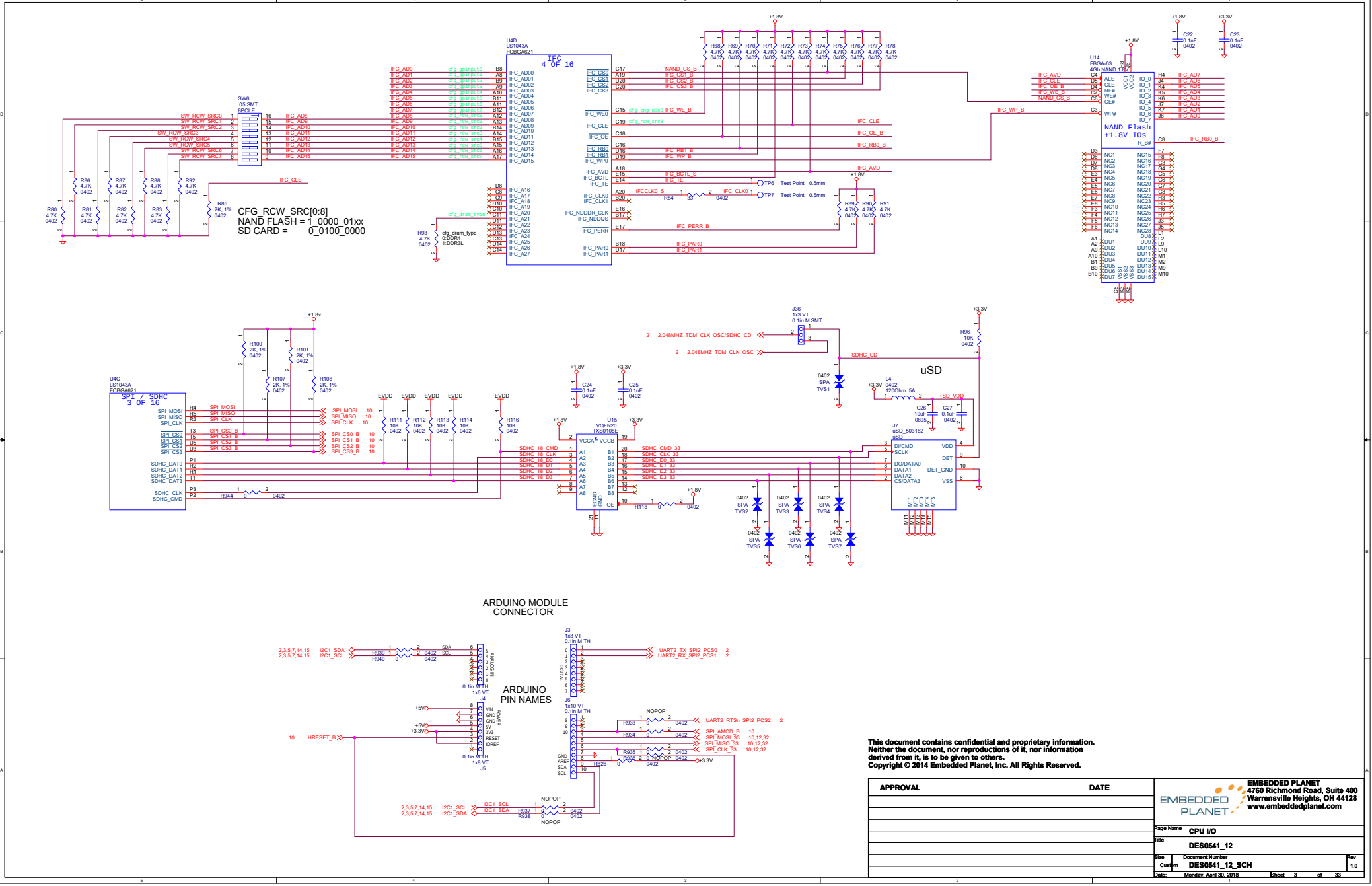

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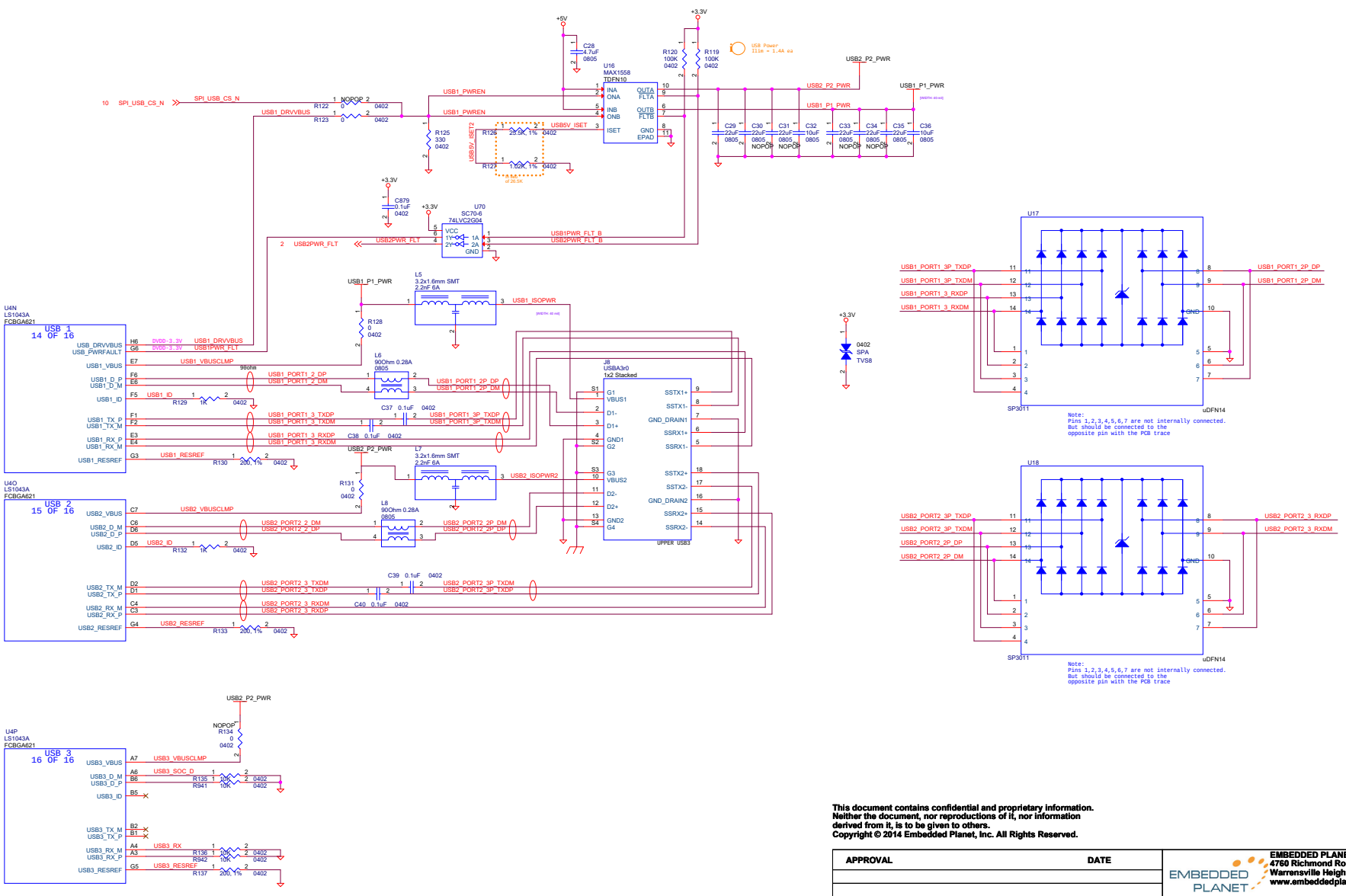

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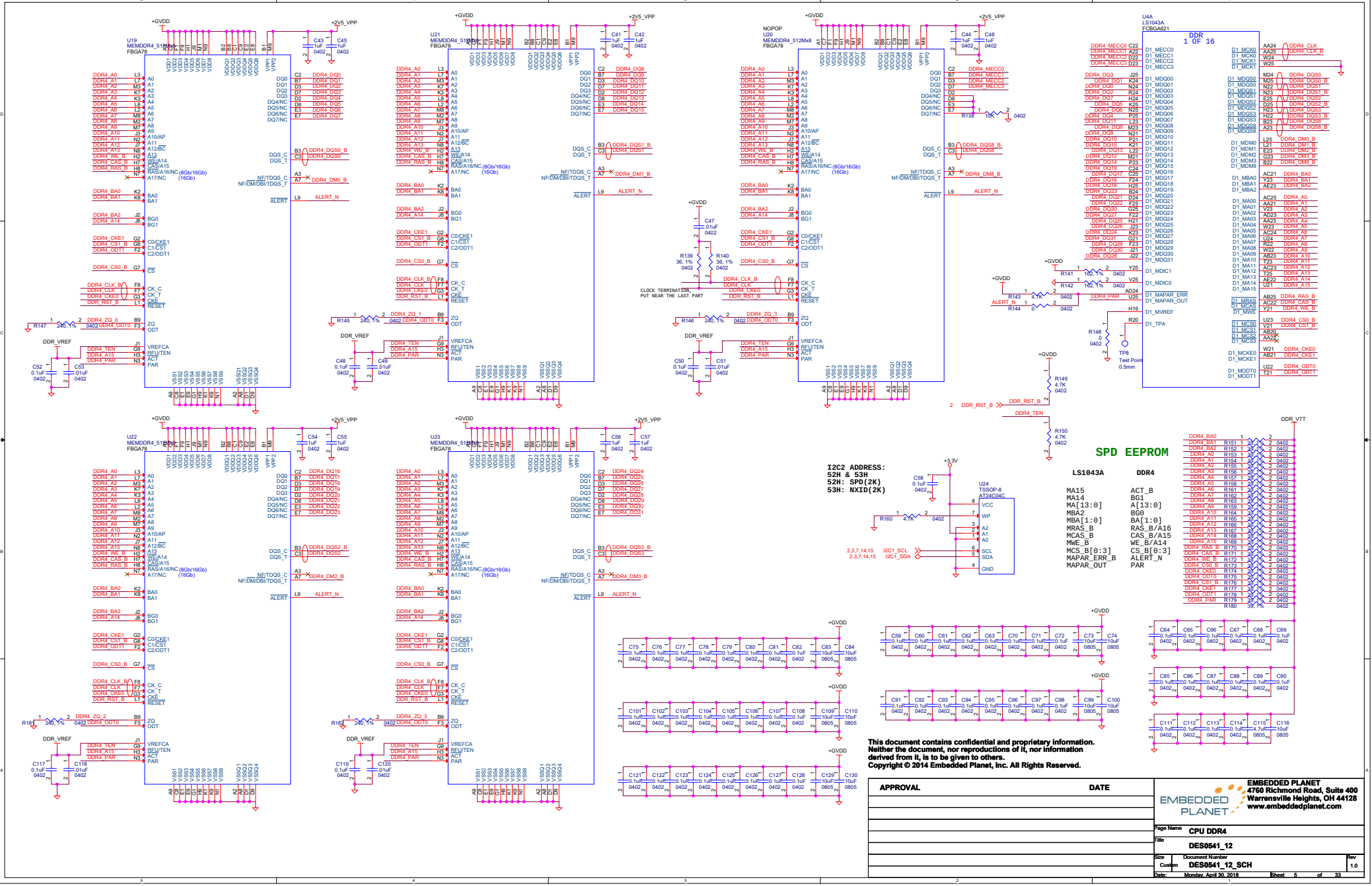
U19
MEMDDR4_512Mx8
FBGA78
U21
MEMDDR4_512Mx8
FBGA78
NOPOP
U20
MEMDDR4_512Mx8
FBGA78
U4A
LS1043A
FCBGA621
DDR
1 OF 16
U22
MEMDDR4_512Mx8
FBGA78
U23
MEMDDR4_512Mx8
FBGA78
+GVDD
+2V5_VPP
DDR_VREF
CLOCK TERMINATION,
PUT NEAR THE LAST PART
I2C2 ADDRESS:
52H & 53H
52H: SPD(2K)
53H: NXID(2K)
SPD EEPROM
LS1043A
DDR4
MA15
MA14
MA[13:0]
MBA2
MBA[1:0]
MRAS_B
MCAS_B
MWE_B
MCS_B[0:3]
MAPAR_ERR_B
MAPAR_OUT
ACT_B
BG1
A[13:0]
BG0
BA[1:0]
RAS_B/A16
CAS_B/A15
WE_B/A14
CS_B[0:3]
ALERT_N
PAR
U24
TSSOP-8
AT24C04C
VCC
WP
A2
A1
A0
SCL
SDA
GND
I2C1_SCL
I2C1_SDA
TP8
Test Point
0.5mm
DDR_VTT
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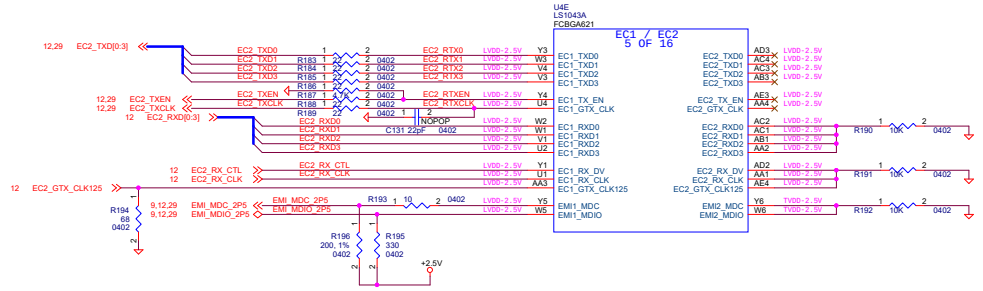

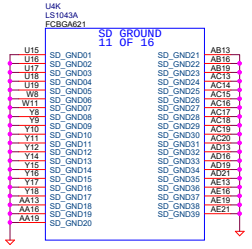

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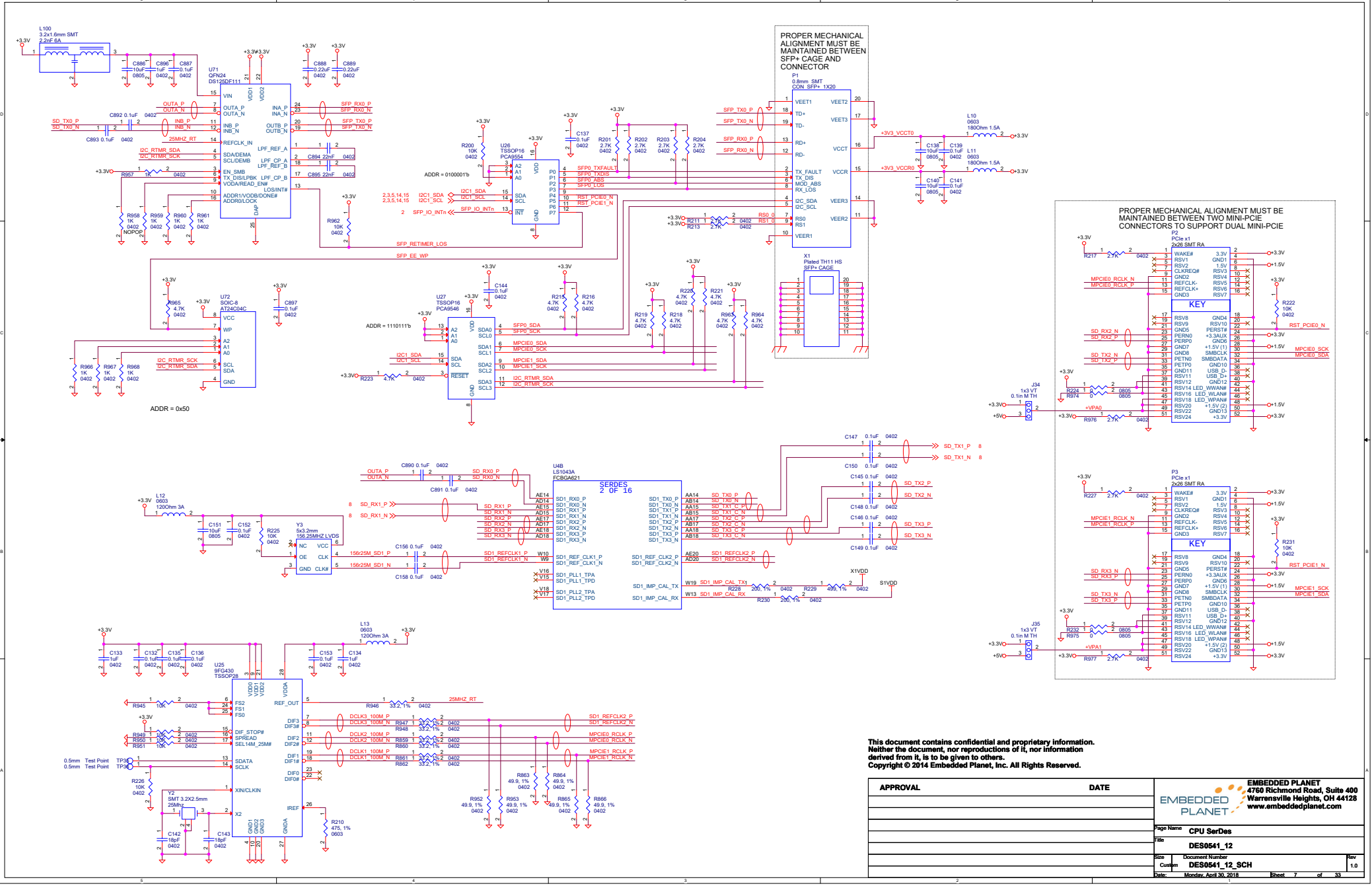
PROPER MECHANICAL ALIGNMENT MUST BE MAINTAINED BETWEEN SFP+ CAGE AND CONNECTOR
PROPER MECHANICAL ALIGNMENT MUST BE MAINTAINED BETWEEN TWO MINI-PCIE CONNECTORS TO SUPPORT DUAL MINI-PCIE
SERDES 2 OF 16
ADDR = 0x50
ADDR = 0100001'b
ADDR = 1110111'b
KEY
KEY
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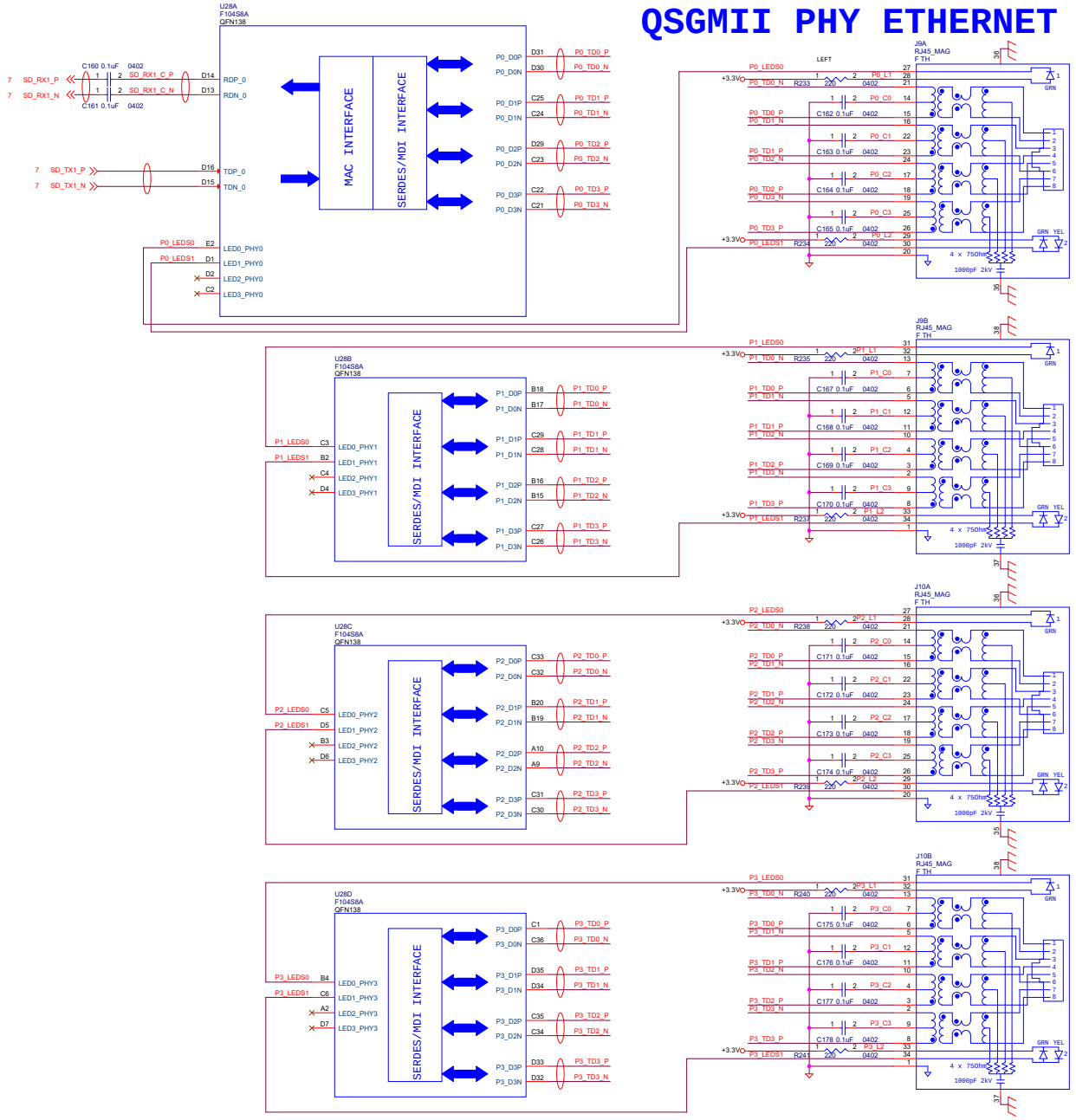
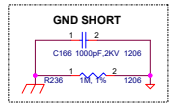
QSGMII PHY ETHERNET PORTS



F104S8A:F104S8A
1.0V 1.425A,max
2.5V 0.57A,max



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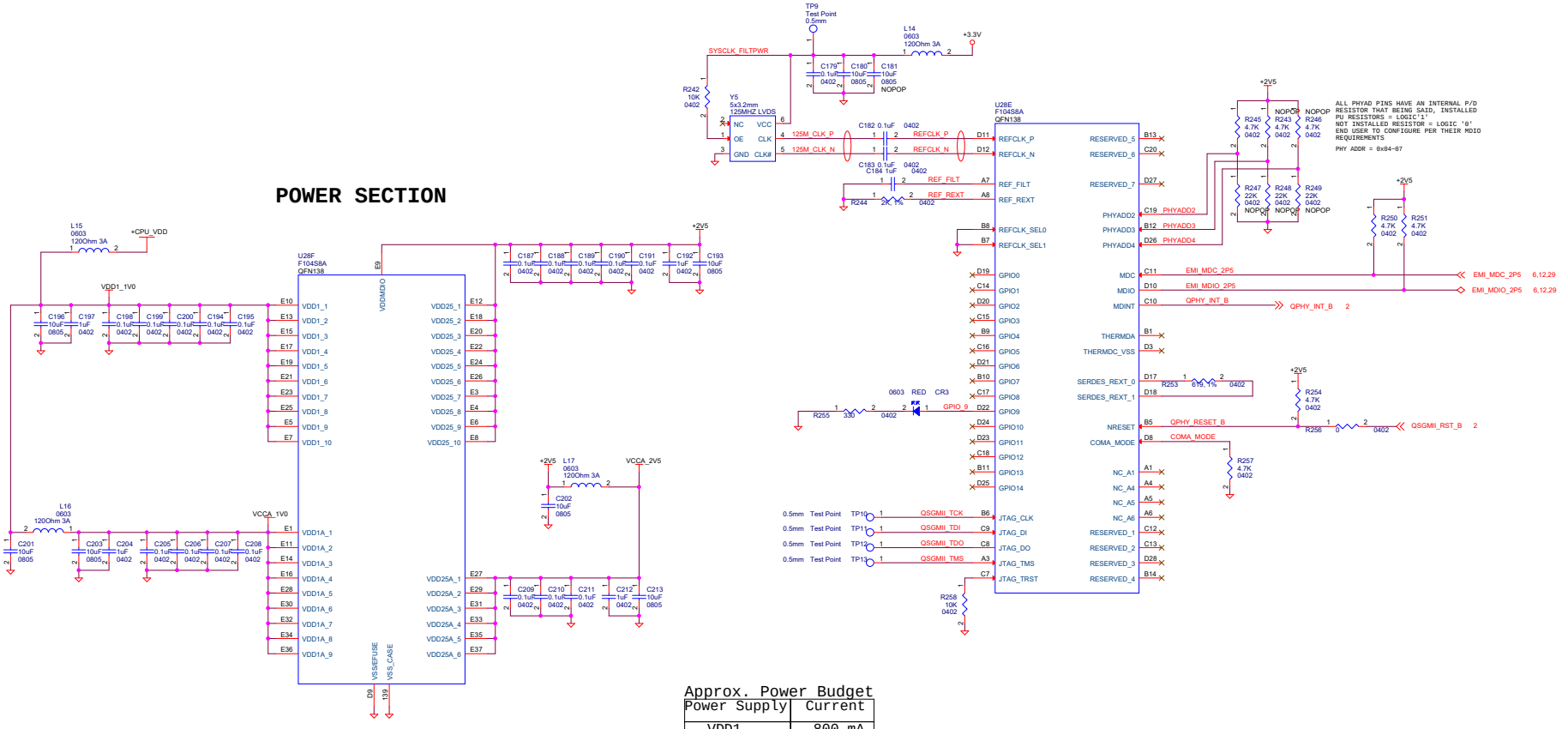
QSGMII CONFIG & POWER

POWER SECTION



Approx. Power Budget

Power Supply	Current
VDD1	800 mA
VDD1A	400 mA
VDD25	200 mA
VDD25A	600 mA
VDDMDIO	25 mA

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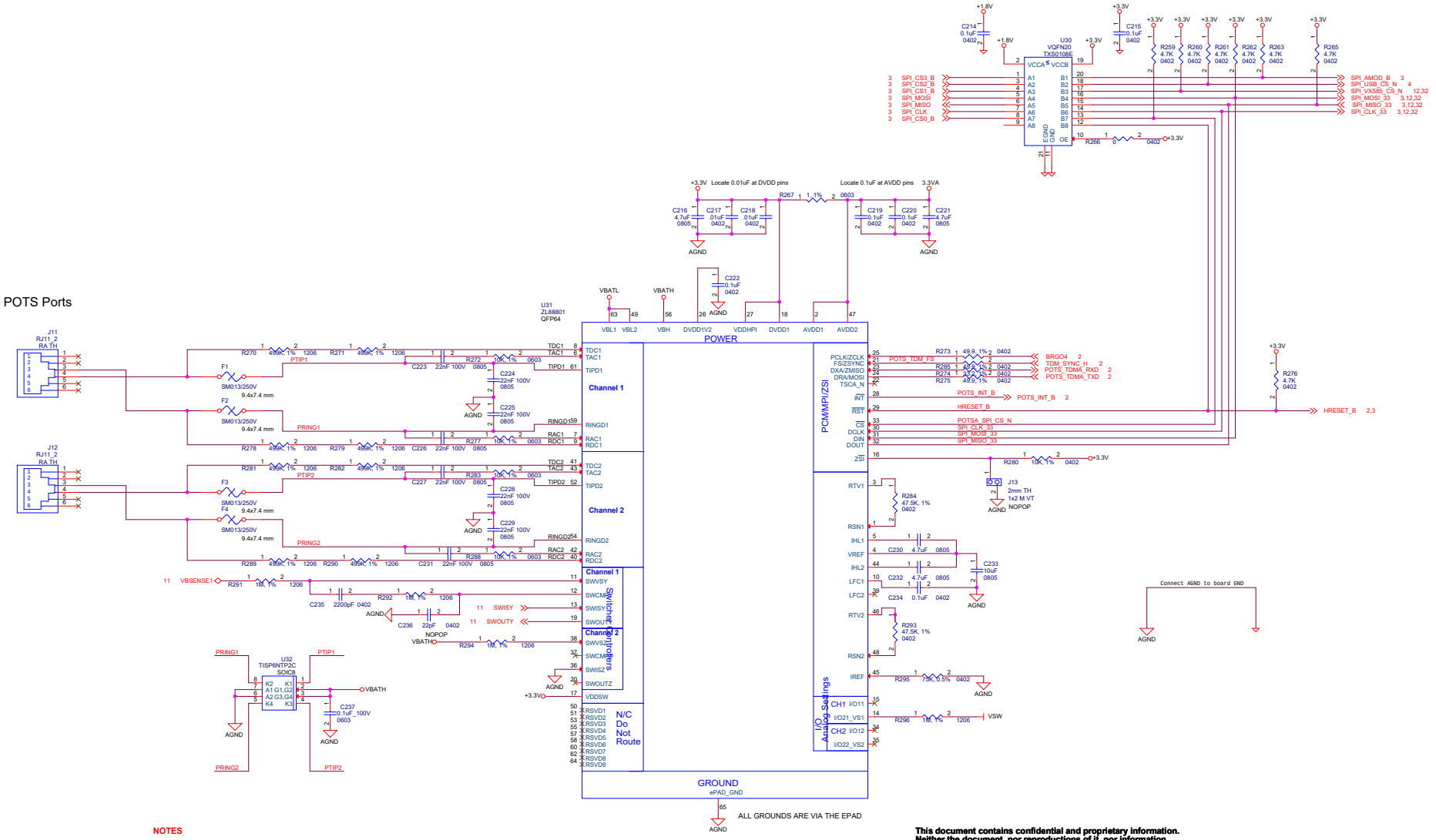

NOTES

- Exposed pad on the ZL88801 must be connected through via holes to both side of top and bottom layer copper and connected to a GND plane.

- Recommended EPAD should be a 292mil square pad with a 9 x 9 array of 13mil/.33mil vias. Vias should be connected to the ground plane with solid connections.

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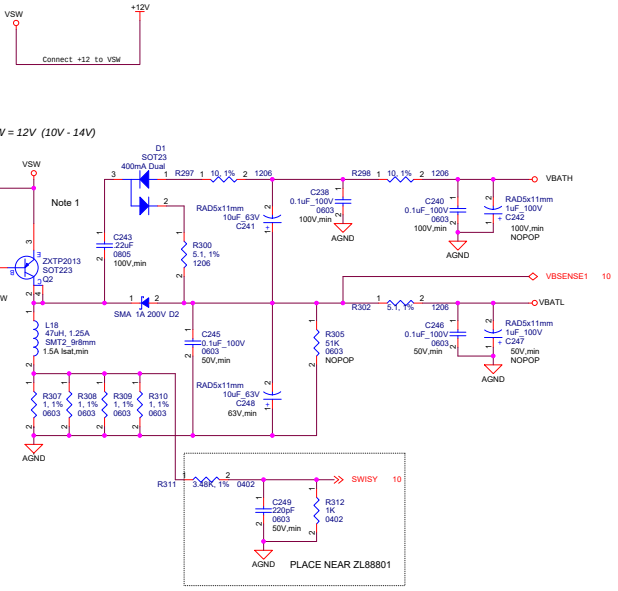
5V VSW INPUT OPERATION
CSW1 = 220uF 10V
L1 = 22uH 2A
RC1 = 0ohm

Ringing capability may be limited
at 5V (4.75V to 6V). 50Vrms 3REN max.



Q1 OPTIONS

For 50Vrms Ringing

ZXTP2012/ZX5T951/FZT951 Vce=60V SOT223 or SOT89

ZXTP2013/ZX5T953/FZT953 Vce=100V SOT223 or SOT89

ZXTP2014/ZX5T955/FZT955 Vce=140V SOT223 or SOT89

For >50Vrms to 60Vrms Ringing

ZXTP2013/ZX5T953/FZT953 Vce=100V SOT223 or SOT89

ZXTP2014/ZX5T955/FZT955 Vce=140V SOT223 or SOT89

NOTES:

1) Q2 should have a collector thermal pad of at least 1cm x 1cm

2) For 60Vrms ringing applications must be 100V Vce rated, ZXTP2013G. C241 should be 63V min.
For 50Vrms ringing Vce can be 60V rated, ZXTP2012G. C241 can be 50V rated.

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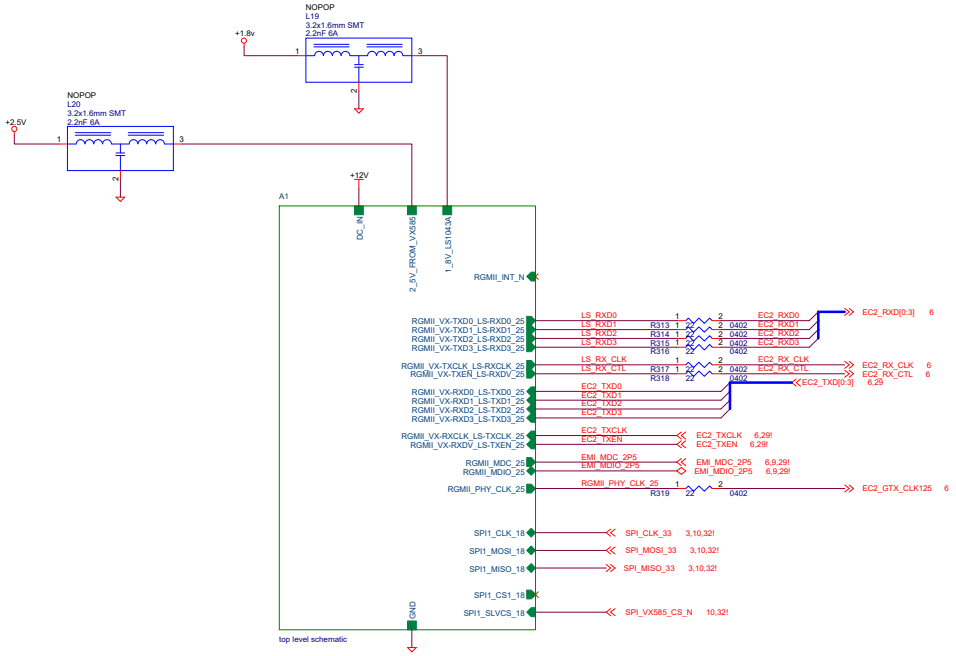
Change L19 and L20 Board Option if DSL circuitry is installed.



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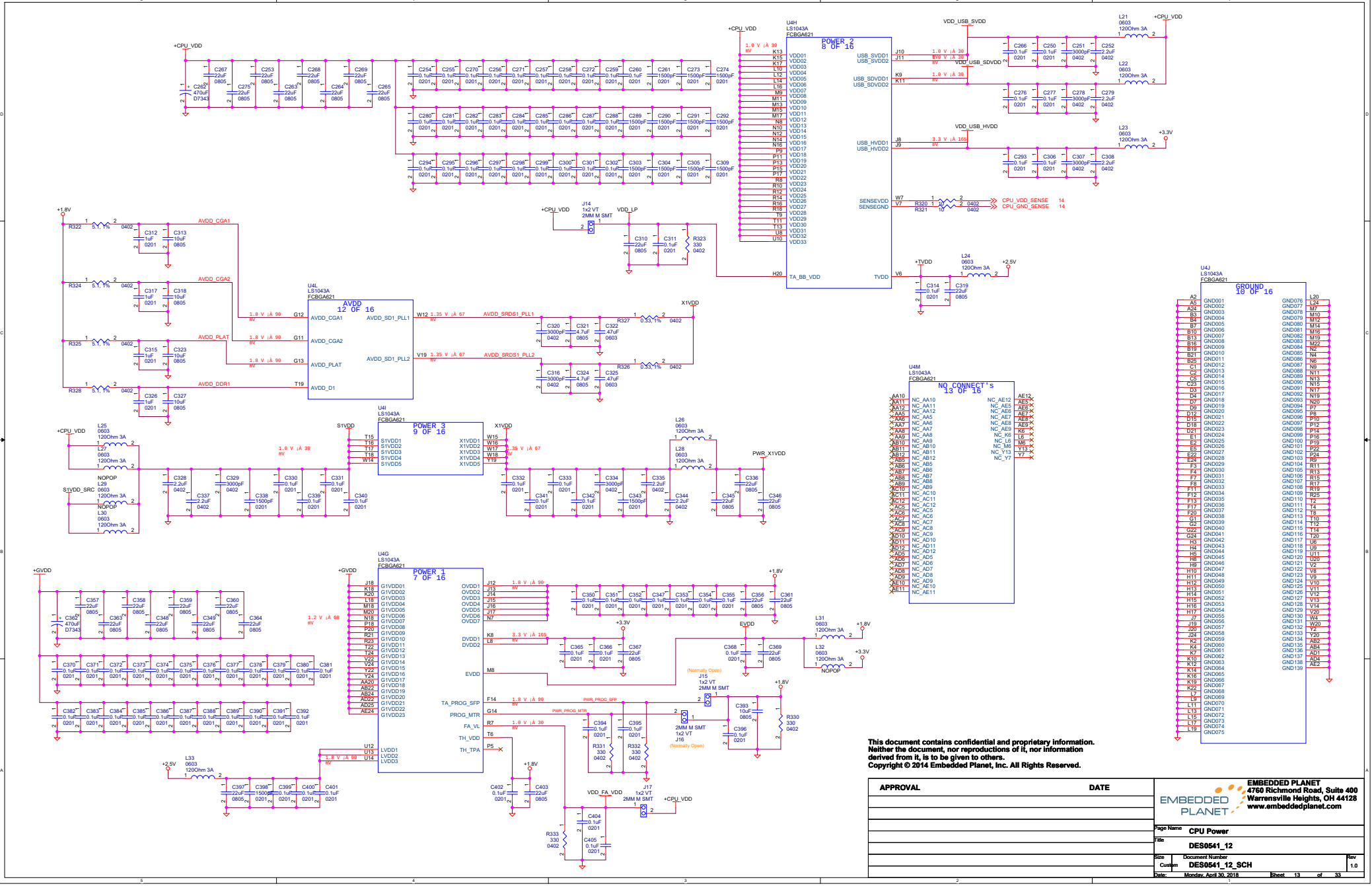

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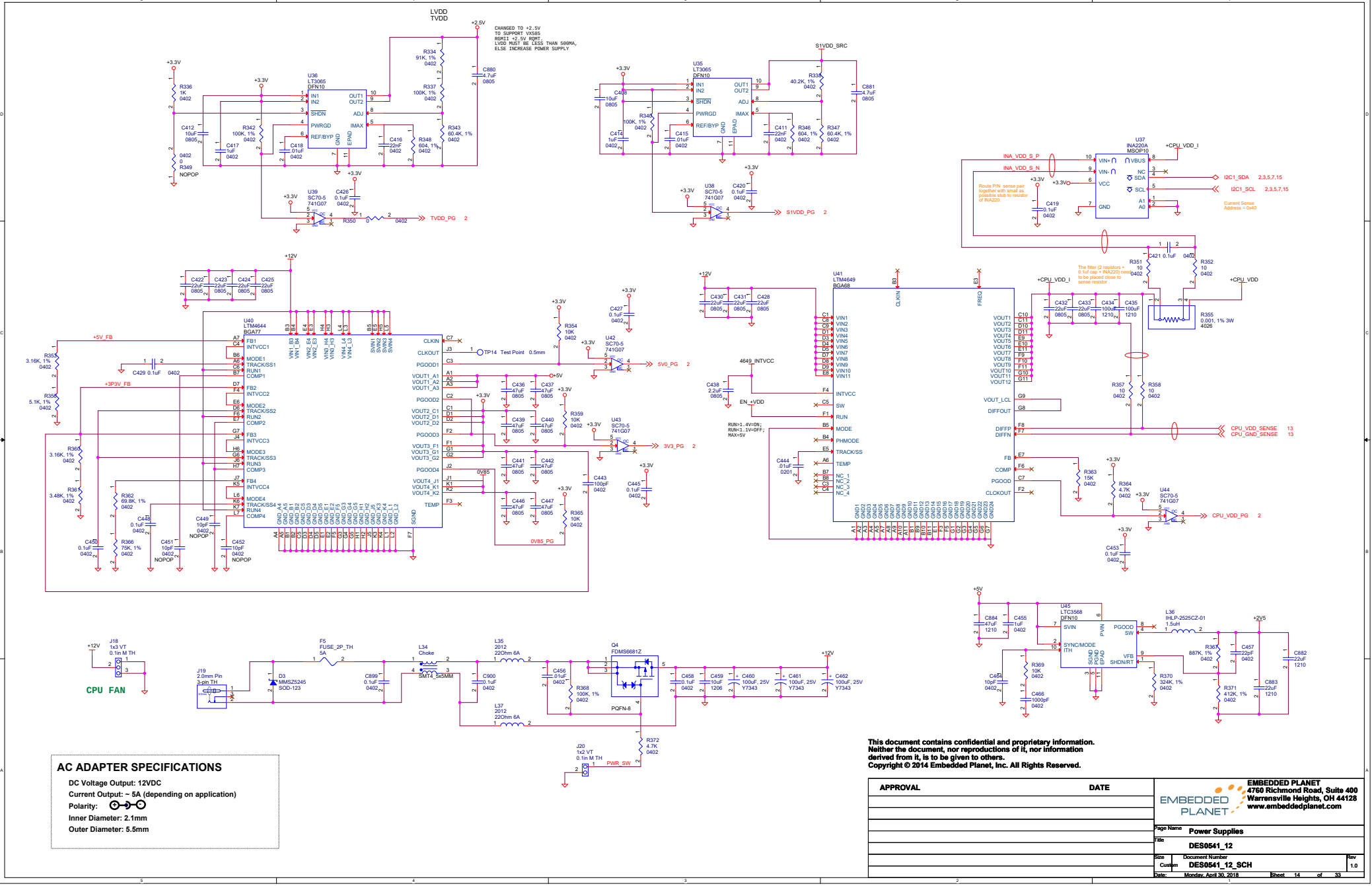

AC ADAPTER SPECIFICATIONS

- DC Voltage Output: 12VDC
- Current Output: ~ 5A (depending on application)
- Polarity:
- Inner Diameter: 2.1mm
- Outer Diameter: 5.5mm

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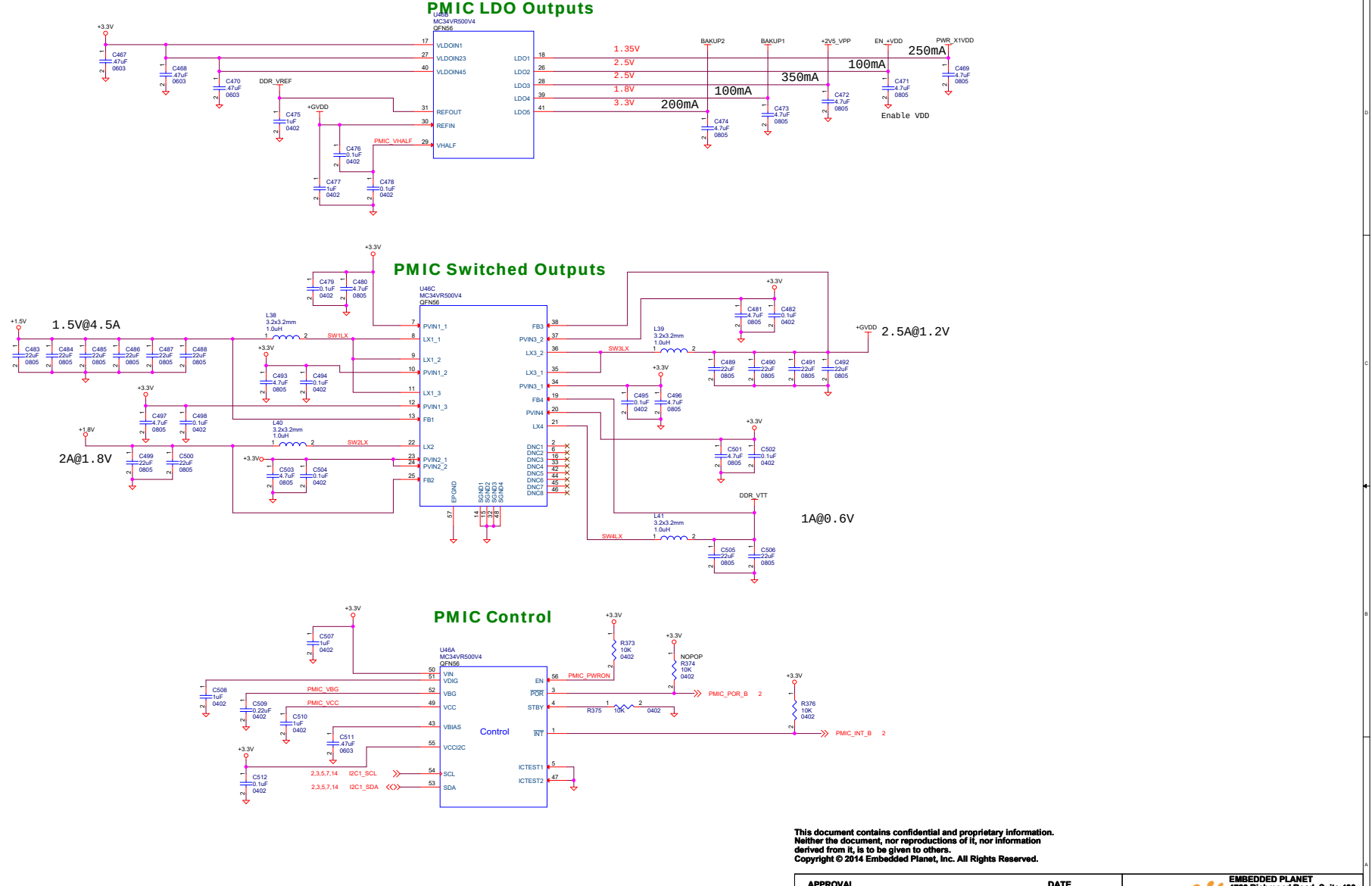

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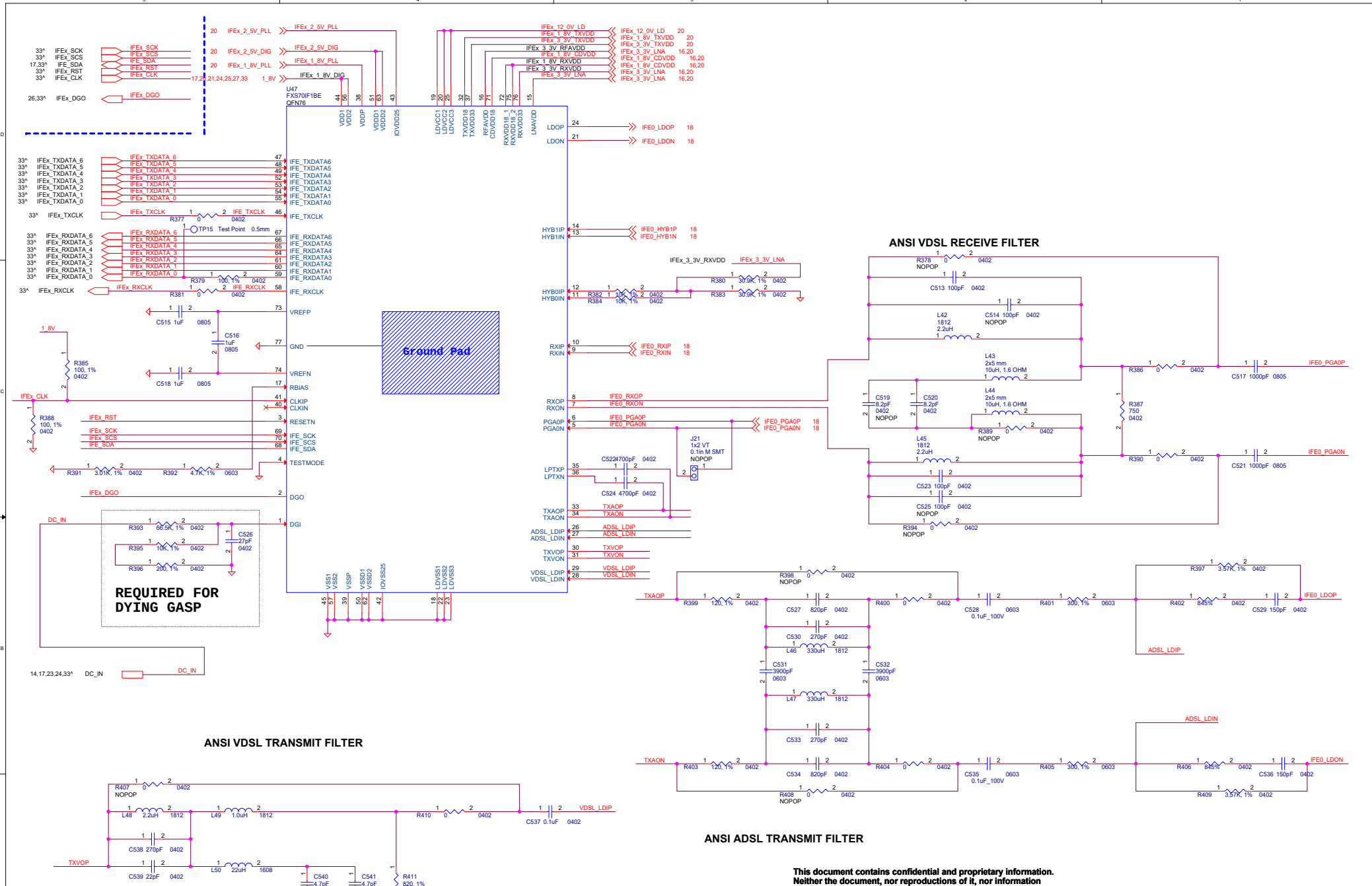
U47
FXS70IF1BE
QFN76
Ground Pad
REQUIRED FOR
DYING GASP
ANSI VDSL RECEIVE FILTER
ANSI VDSL TRANSMIT FILTER
ANSI ADSL TRANSMIT FILTER
IFEx_2_5V_PLL
IFEx_2_5V_DIG
IFEx_1_8V_PLL
IFEx_1_8V_DIG
IFEx_SCK
IFEx_SCS
IFE_SDA
IFEx_RST
IFEx_CLK
IFEx_DGO
IFEx_TXDATA_6
IFEx_TXDATA_5
IFEx_TXDATA_4
IFEx_TXDATA_3
IFEx_TXDATA_2
IFEx_TXDATA_1
IFEx_TXDATA_0
IFEx_TXCLK
IFEx_RXDATA_6
IFEx_RXDATA_5
IFEx_RXDATA_4
IFEx_RXDATA_3
IFEx_RXDATA_2
IFEx_RXDATA_1
IFEx_RXDATA_0
IFEx_RXCLK
IFEx_12_0V_LD
IFEx_1_8V_TXVDD
IFEx_3_3V_TXVDD
IFEx_3_3V_RFAVDD
IFEx_1_8V_CDVDD
IFEx_1_8V_RXVDD
IFEx_3_3V_RXVDD
IFEx_3_3V_LNA
IFE0_LDOP
IFE0_LDON
IFE0_HYB1P
IFE0_HYB1N
IFE0_RXIP
IFE0_RXIN
IFE0_RXOP
IFE0_RXON
IFE0_PGA0P
IFE0_PGA0N
TXAOP
TXAON
ADSL_LDIP
ADSL_LDIN
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DC_IN
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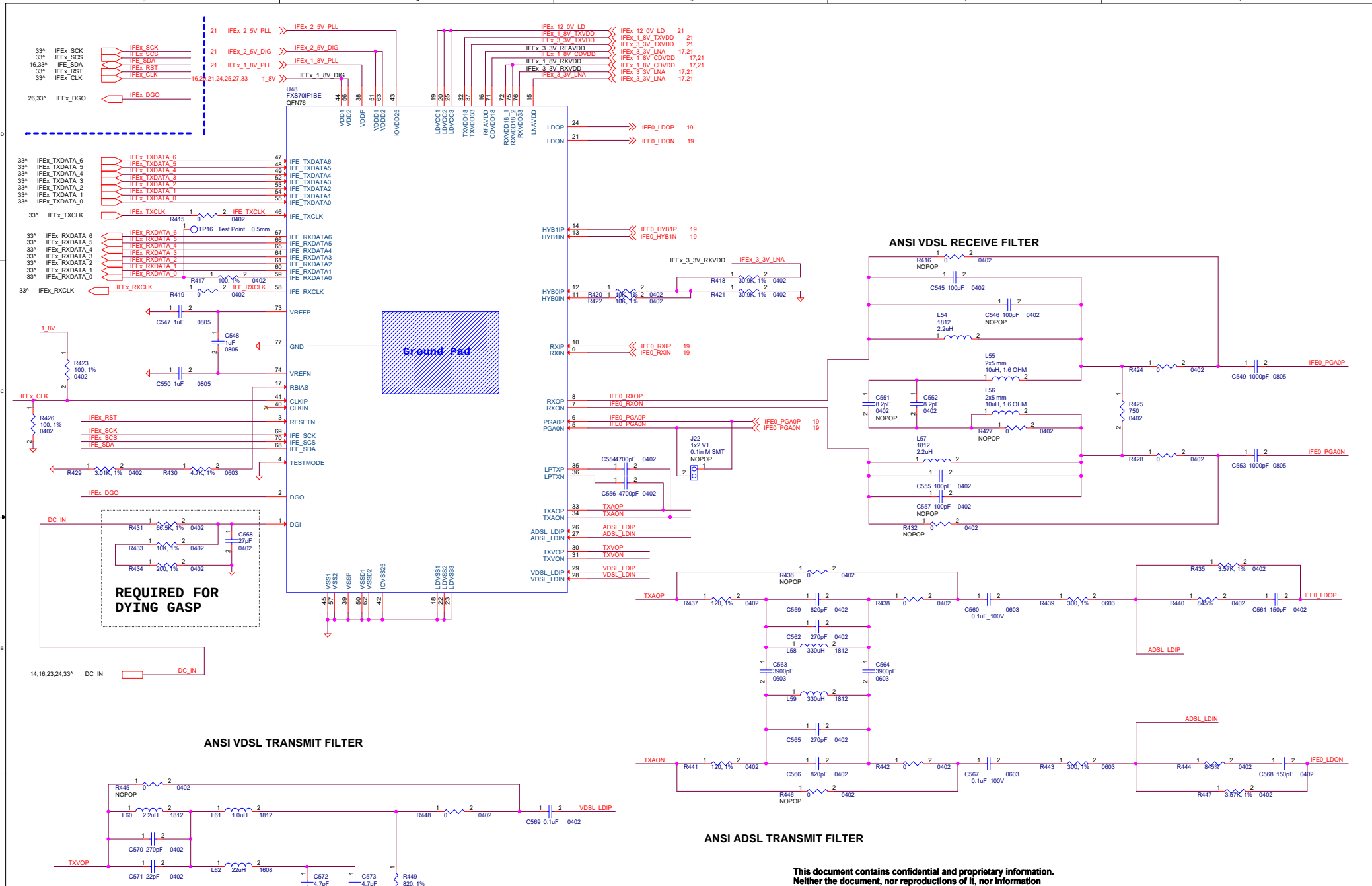
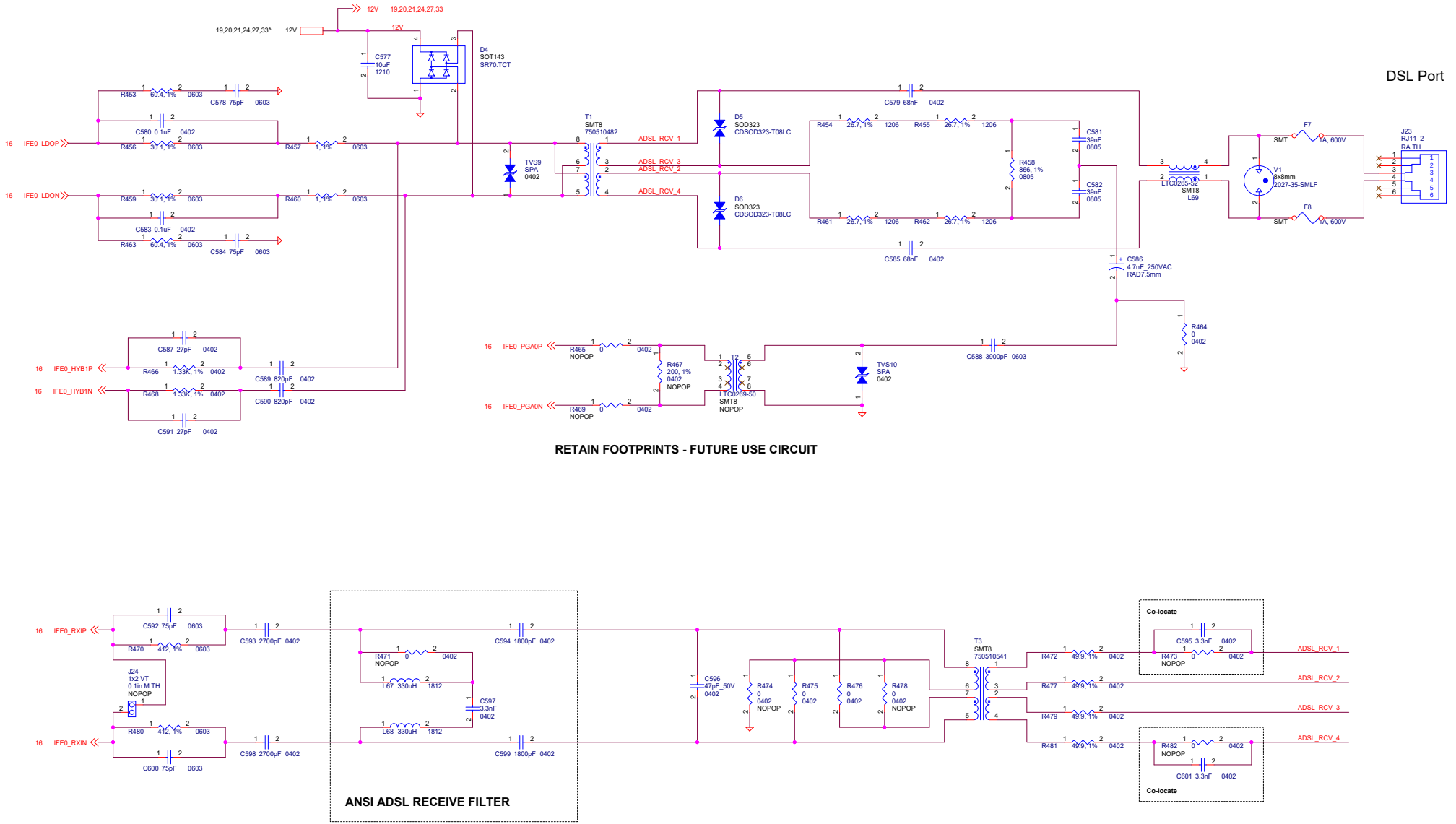
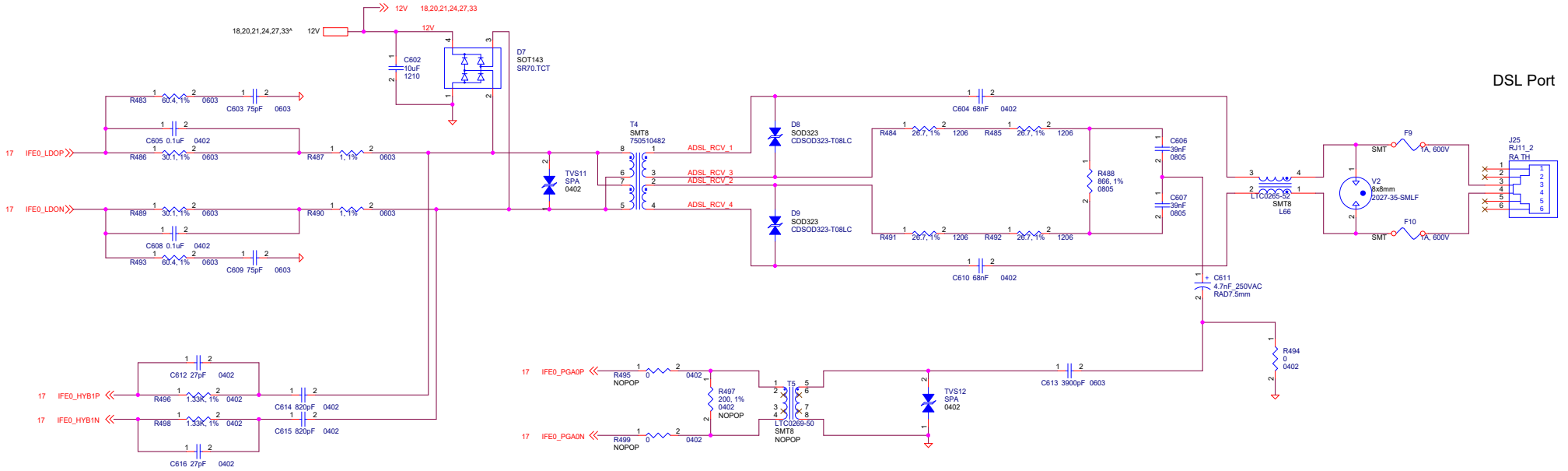
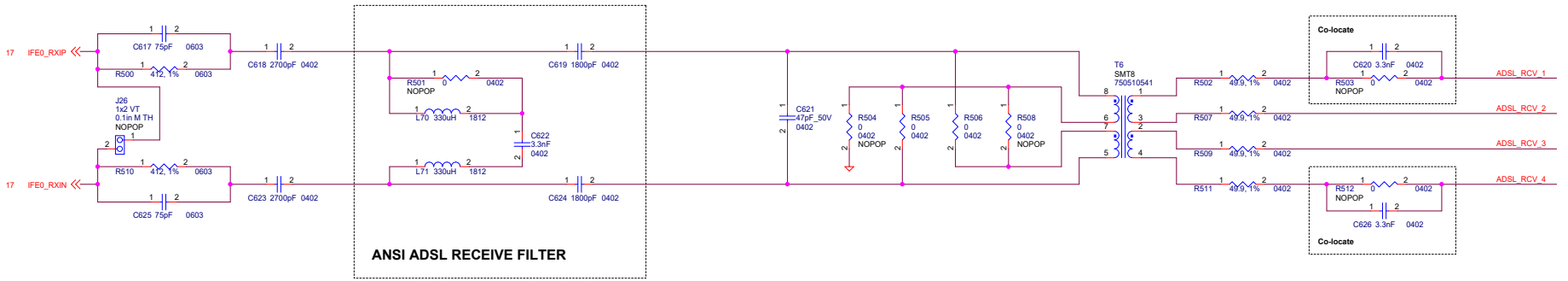




DSL Port

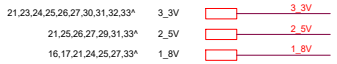


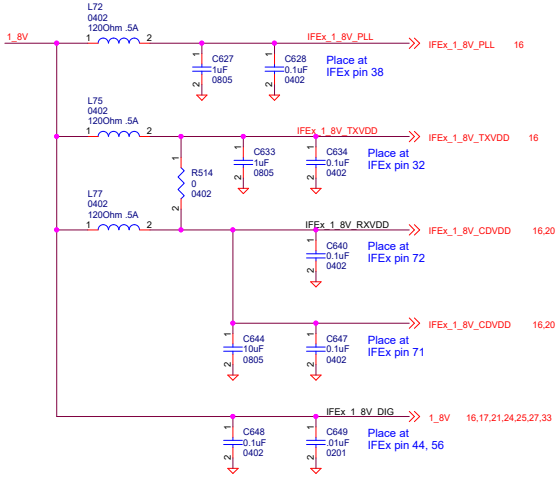
RETAIN FOOTPRINTS - FUTURE USE CIRCUIT

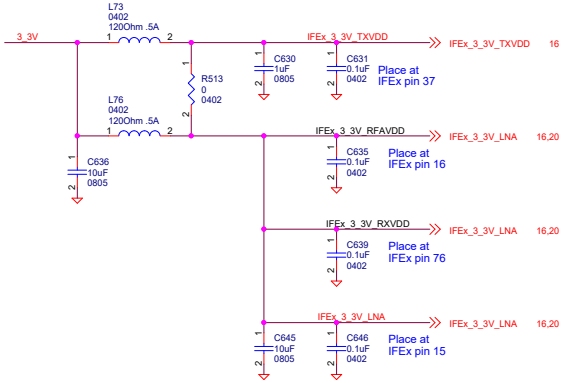


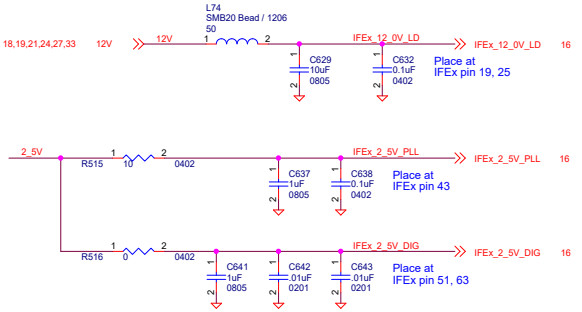
ANSI ADSL RECEIVE FILTER

Power Input

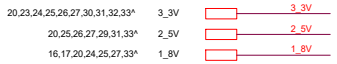


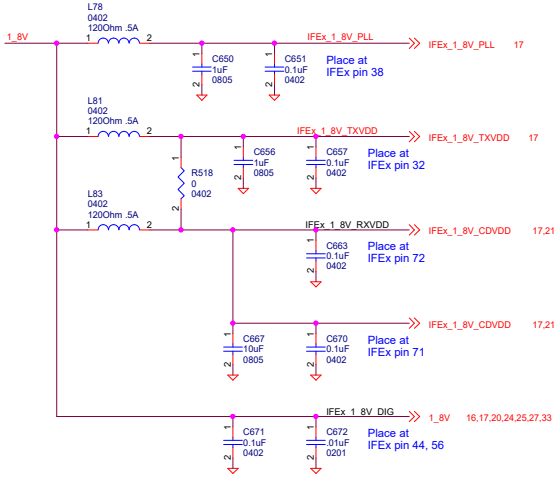


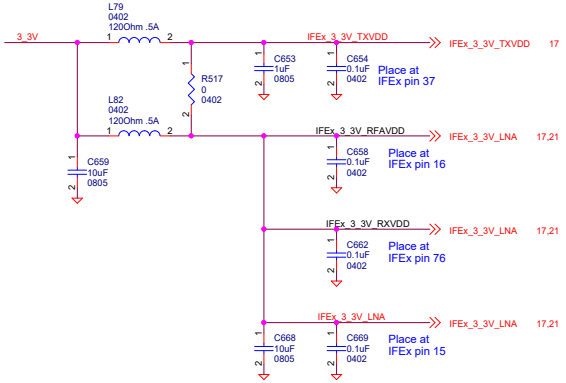


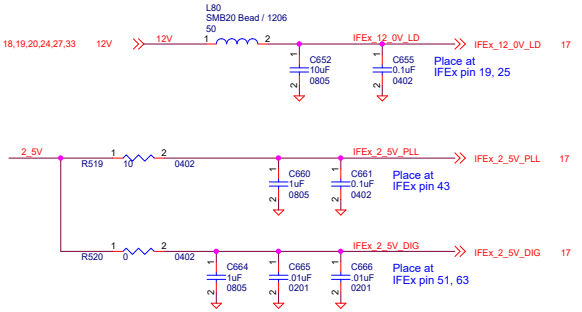


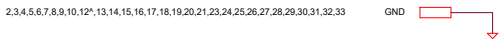
Power Input

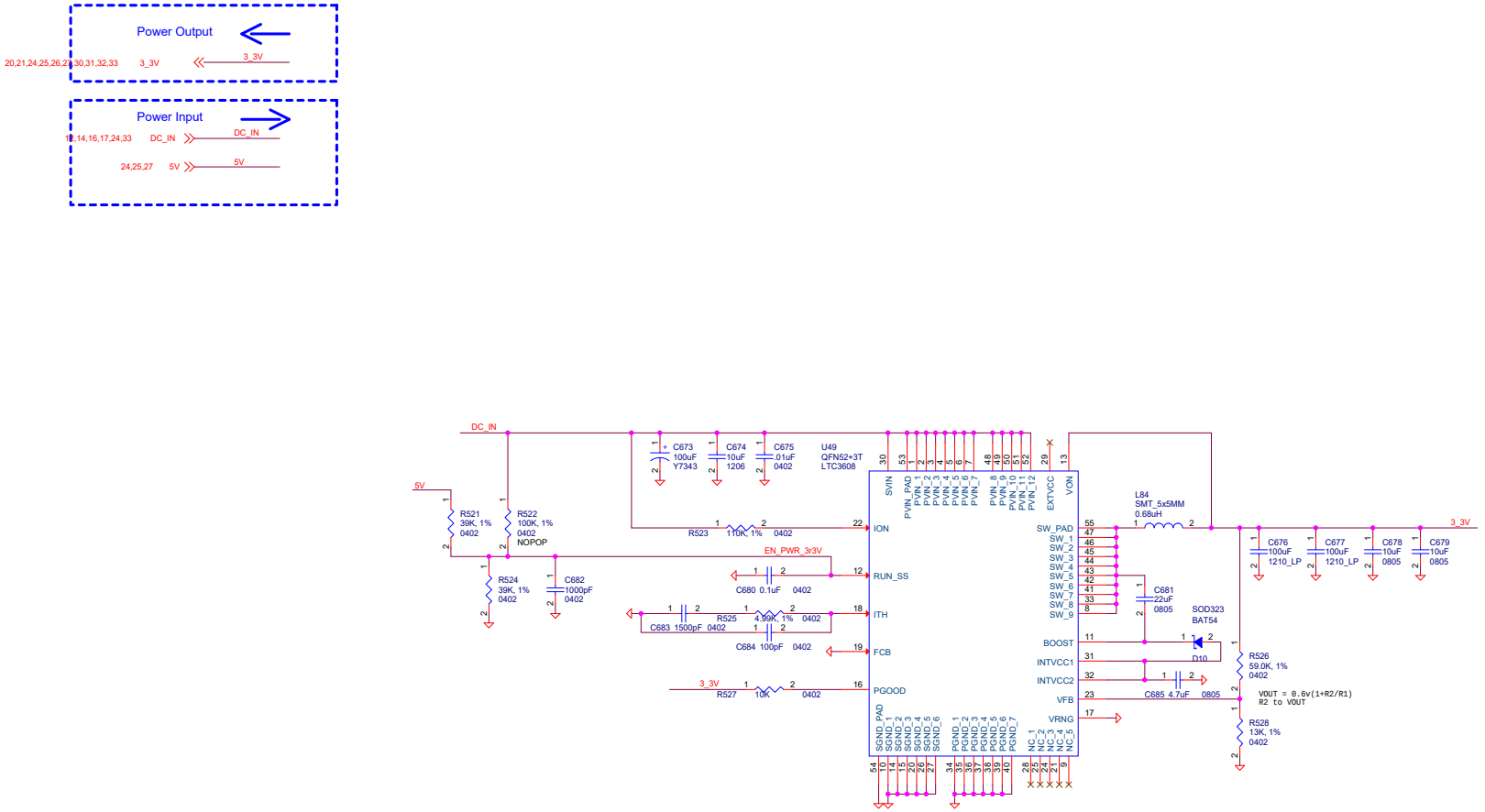


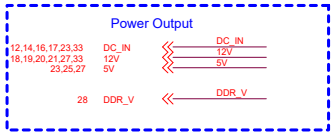


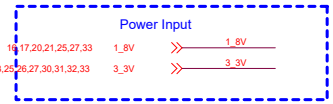


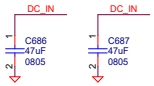




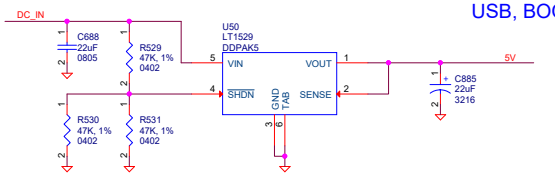


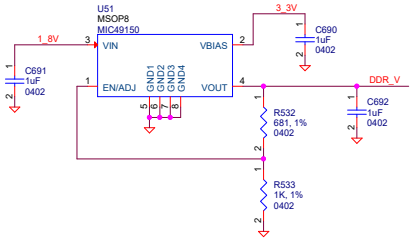


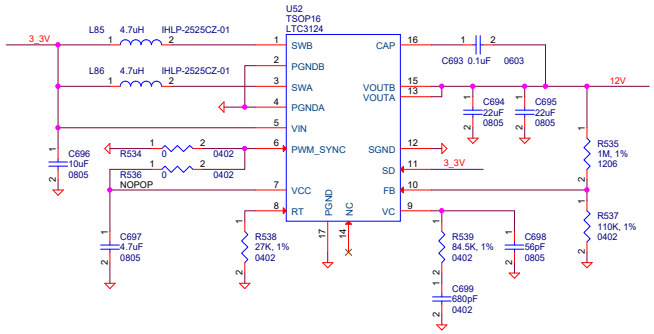


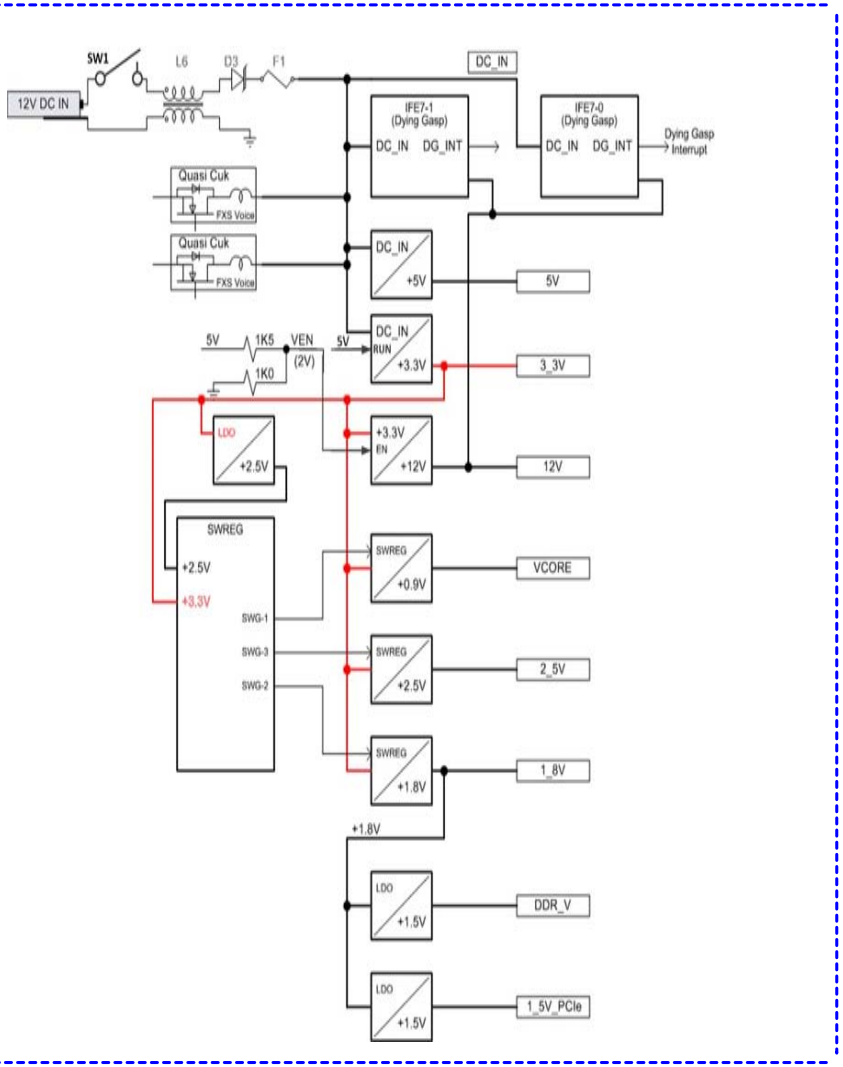


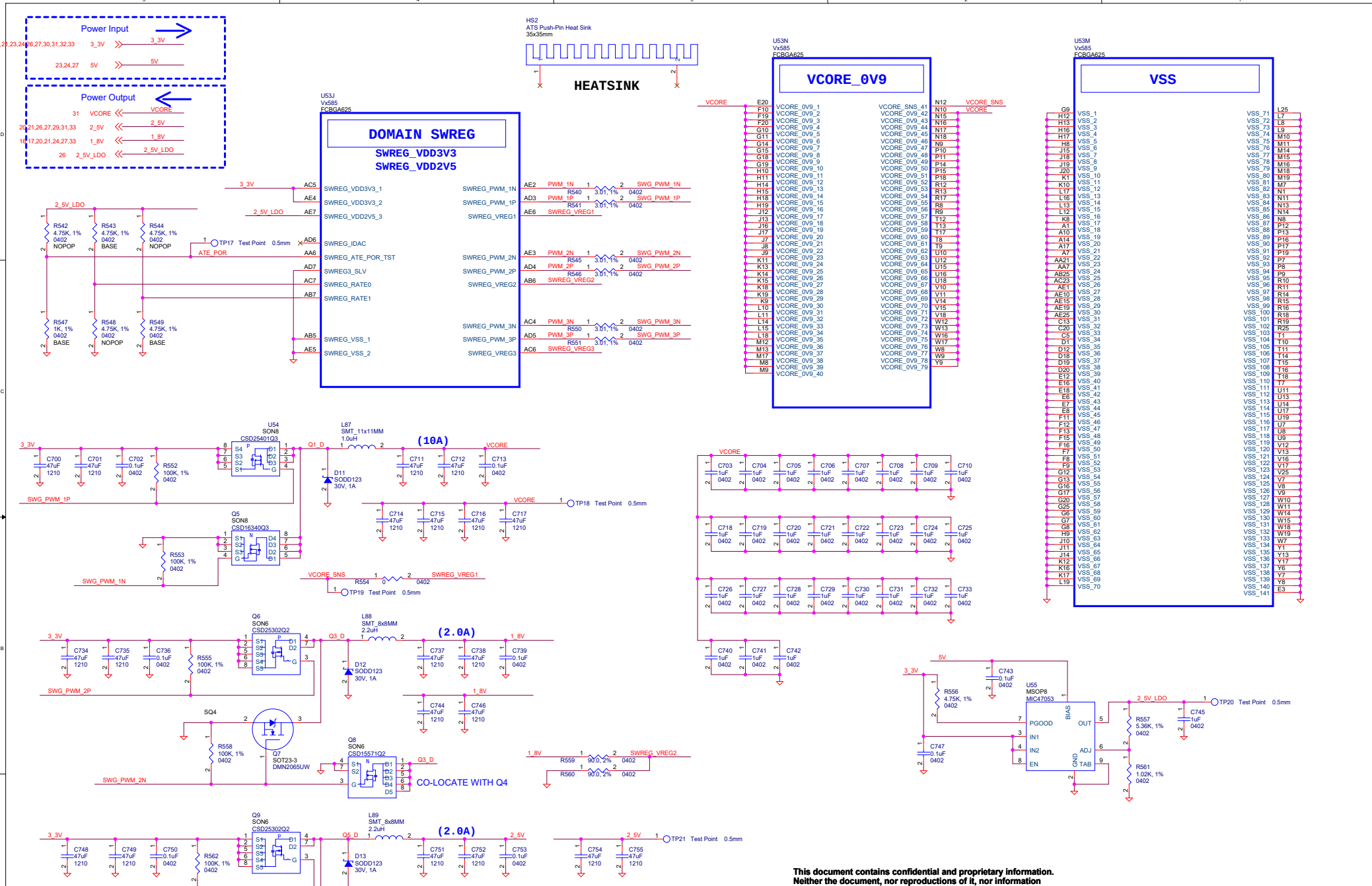
5V FOR:
USB, BOOST OF IFE7

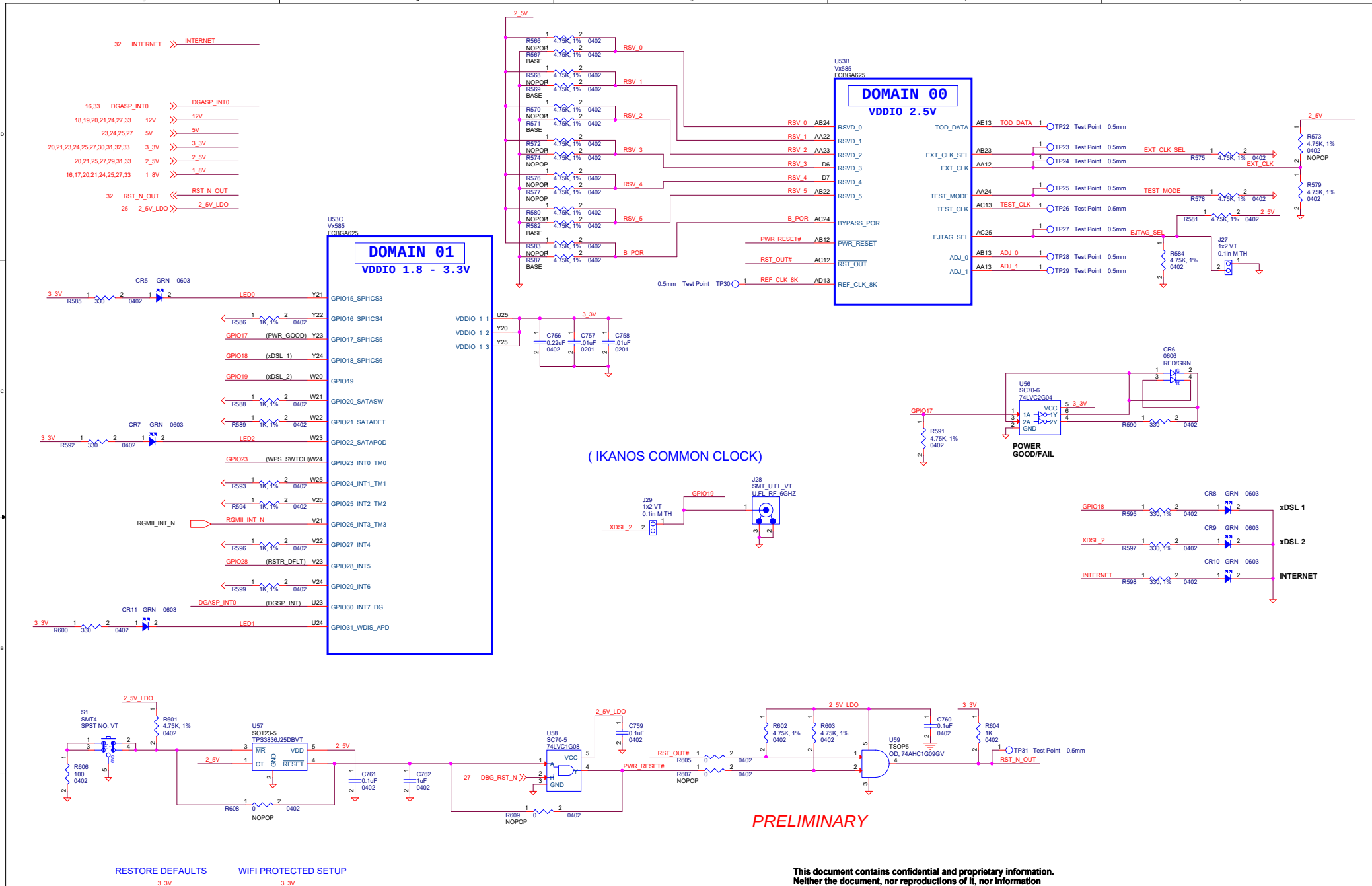











DOMAIN 00
VDDIO 2.5V
U53B
Vx585
FCBGA625
DOMAIN 01
VDDIO 1.8 - 3.3V
U53C
Vx585
FCBGA625
(IKANOS COMMON CLOCK)
POWER
GOOD/FAIL
PRELIMINARY
RESTORE DEFAULTS
WIFI PROTECTED SETUP
xDSL 1
xDSL 2
INTERNET
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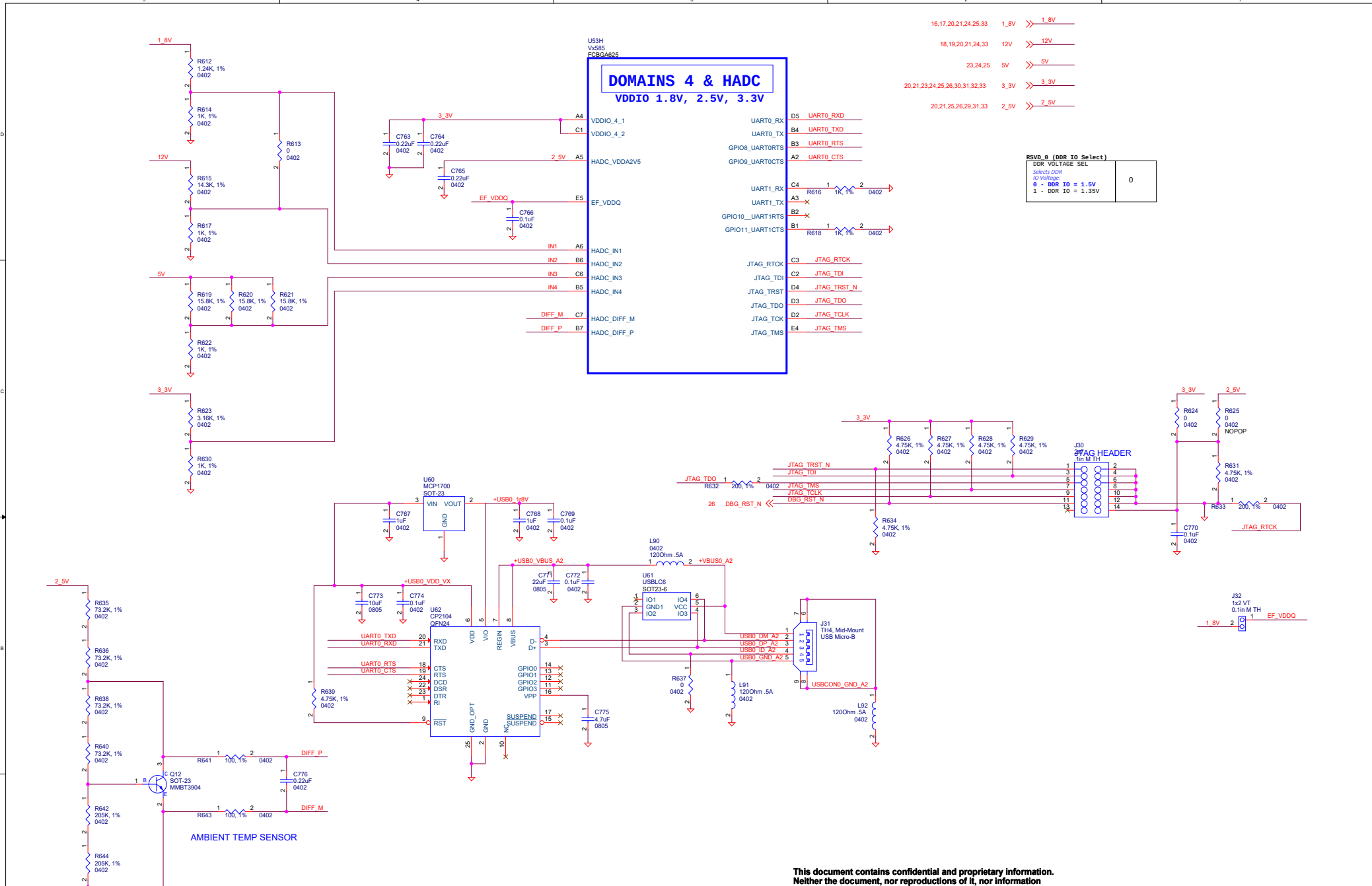
DOMAINS 4 & HADC
VDDIO 1.8V, 2.5V, 3.3V
U53H
Vx585
FCBGA625
VDDIO_4_1
VDDIO_4_2
HADC_VDDA2V5
EF_VDDQ
HADC_IN1
HADC_IN2
HADC_IN3
HADC_IN4
HADC_DIFF_M
HADC_DIFF_P
UART0_RX
UART0_TX
GPIO8_UART0RTS
GPIO9_UART0CTS
UART1_RX
UART1_TX
GPIO10__UART1RTS
GPIO11_UART1CTS
JTAG_RTCK
JTAG_TDI
JTAG_TRST
JTAG_TDO
JTAG_TCK
JTAG_TMS
RSVD_0 (DDR IO Select)
DDR VOLTAGE SEL
Selects DDR IO Voltage:
0 - DDR IO = 1.5V
1 - DDR IO = 1.35V
AMBIENT TEMP SENSOR
JTAG HEADER
2mm 1in M TH
MCP1700 SOT-23
CP2104 QFN24
USBLC6 SOT23-6
TH4, Mid-Mount USB Micro-B
1x2 VT 0.1in M TH
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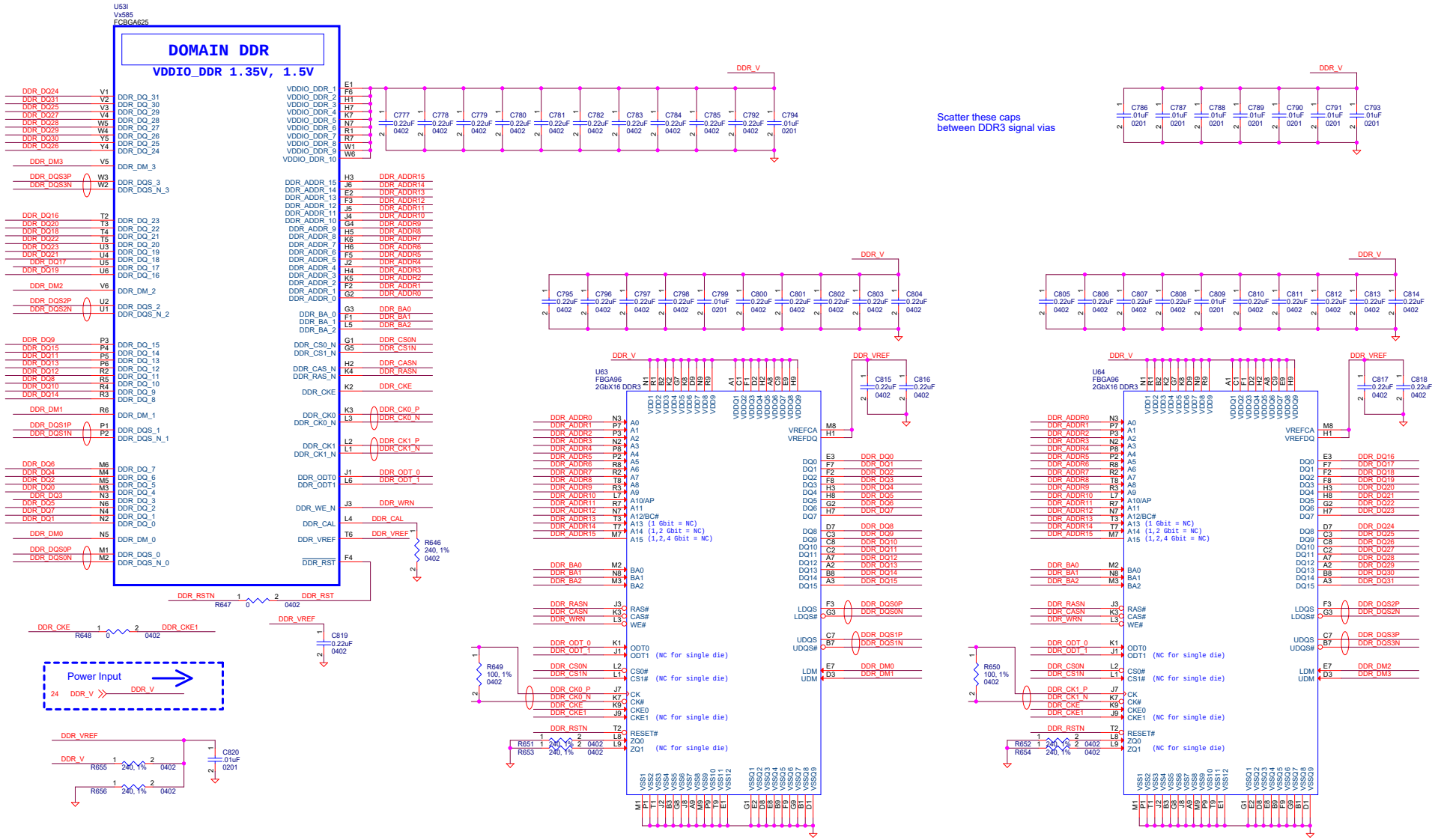
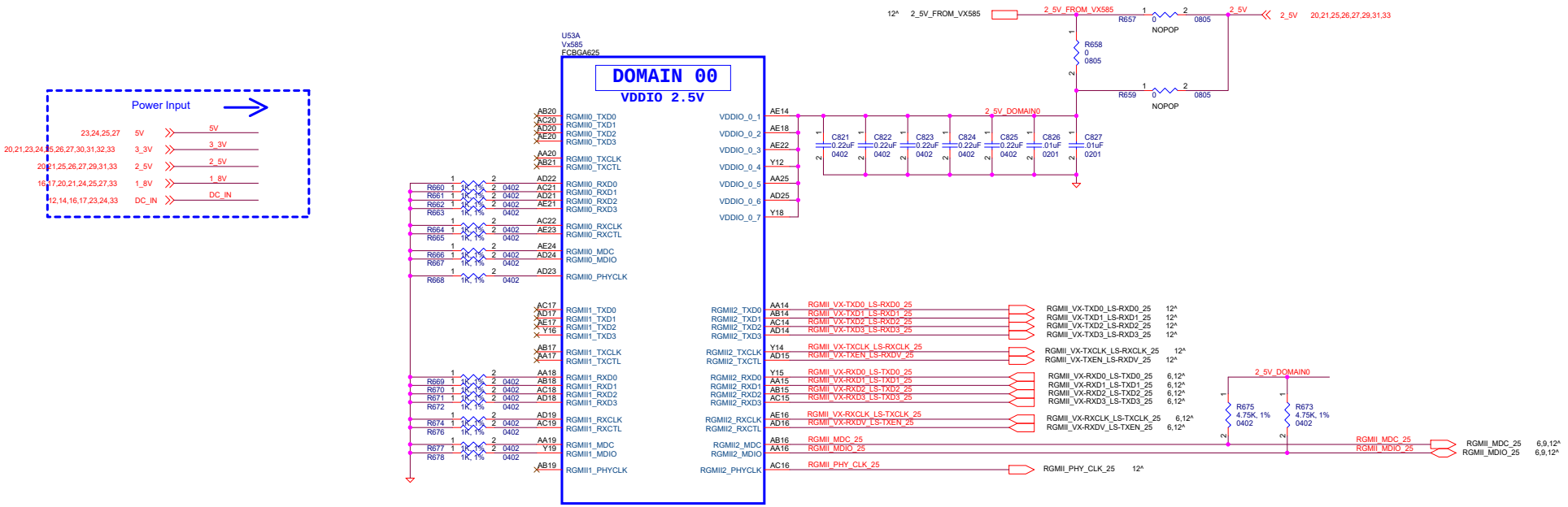
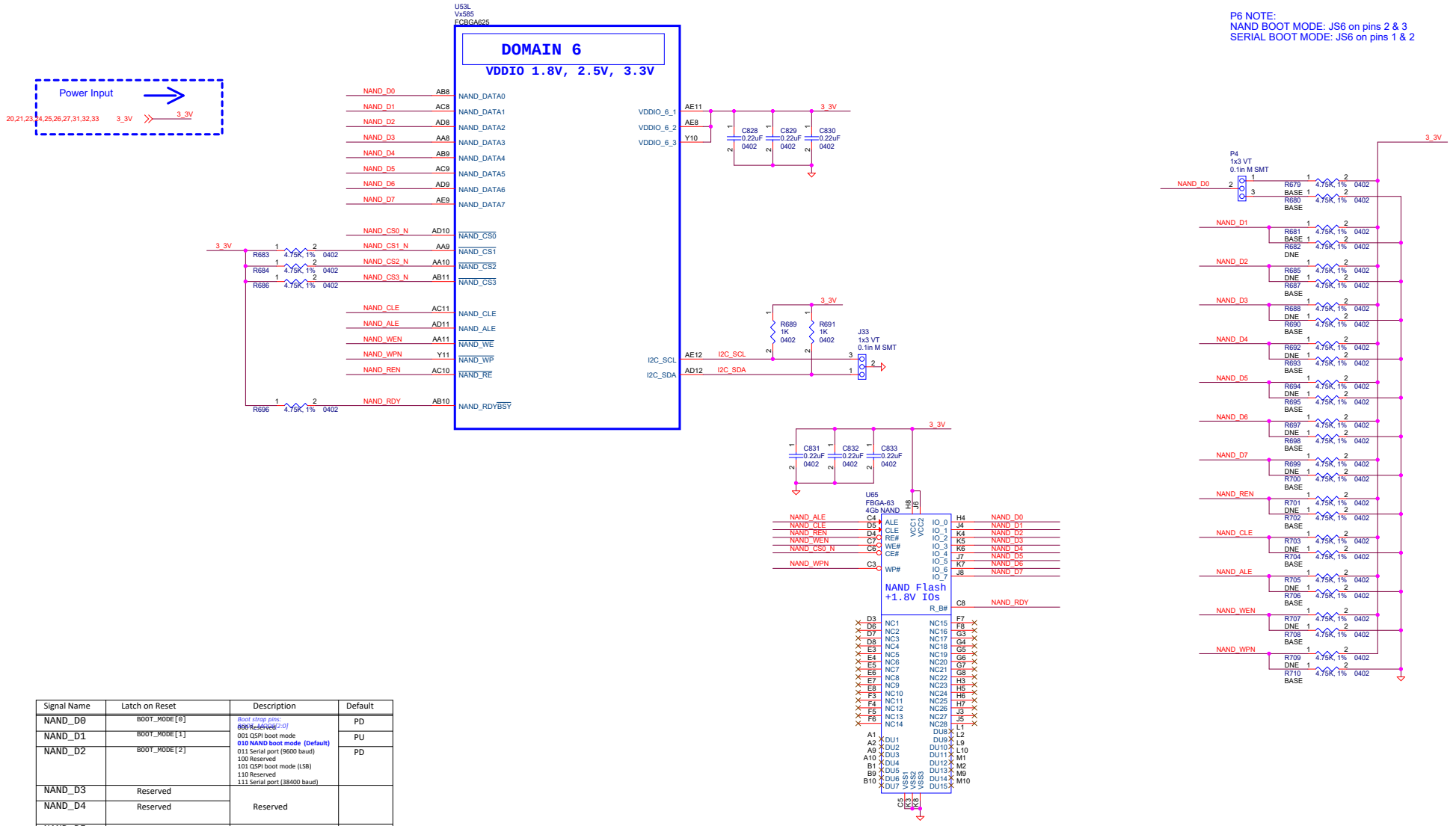
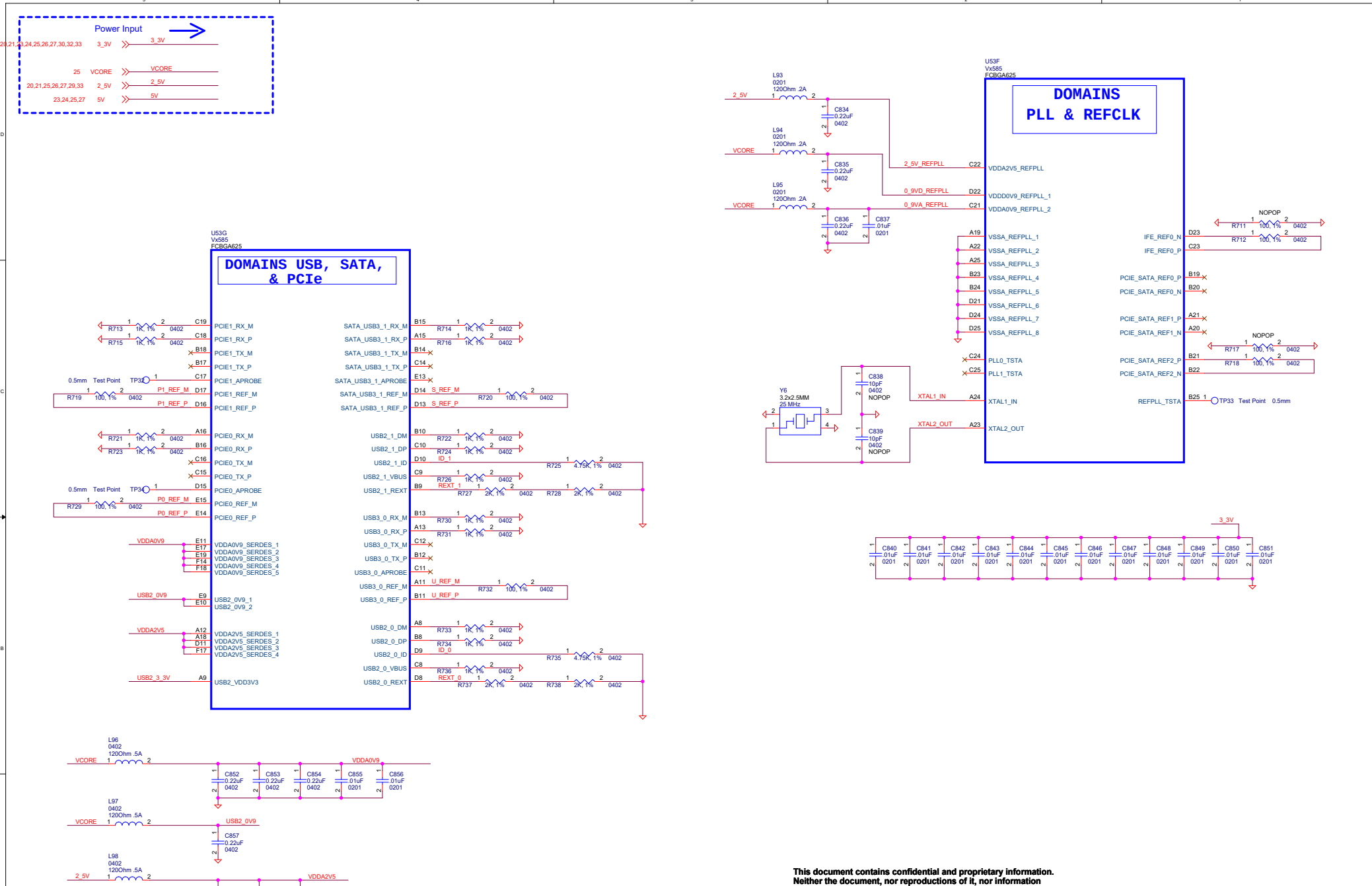






Signal Name	Latch on Reset	Description	Default
NAND_D0	BOOT_MODE[0]	Boot strap pins: BOOT_MODE[2:0] 000 Reserved 001 QSPI boot mode 010 NAND boot mode (Default) 011 Serial port (9600 baud) 100 Reserved 101 QSPI boot mode (LSB) 110 Reserved 111 Serial port (38400 baud)	PD
NAND_D1	BOOT_MODE[1]		PU
NAND_D2	BOOT_MODE[2]		PD
NAND_D3	Reserved		
NAND_D4	Reserved	Reserved	
NAND_D5	Reserved		
NAND_D6	Reserved	Reserved	
NAND_D7	Reserved		
NAND_REN	Reserved	Reserved	
NAND_CLE	Reserved		


Power Input
3_3V
VCORE
2_5V
5V
DOMAINS USB, SATA, & PCIe
DOMAINS PLL & REFCLK
U53G
Vx585
FCBGA625
U53F
Vx585
FCBGA625
PCIE1_RX_M
PCIE1_RX_P
PCIE1_TX_M
PCIE1_TX_P
PCIE1_APROBE
PCIE1_REF_M
PCIE1_REF_P
PCIE0_RX_M
PCIE0_RX_P
PCIE0_TX_M
PCIE0_TX_P
PCIE0_APROBE
PCIE0_REF_M
PCIE0_REF_P
SATA_USB3_1_RX_M
SATA_USB3_1_RX_P
SATA_USB3_1_TX_M
SATA_USB3_1_TX_P
SATA_USB3_1_APROBE
SATA_USB3_1_REF_M
SATA_USB3_1_REF_P
USB2_1_DM
USB2_1_DP
USB2_1_ID
USB2_1_VBUS
USB2_1_REXT
USB3_0_RX_M
USB3_0_RX_P
USB3_0_TX_M
USB3_0_TX_P
USB3_0_APROBE
USB3_0_REF_M
USB3_0_REF_P
USB2_0_DM
USB2_0_DP
USB2_0_ID
USB2_0_VBUS
USB2_0_REXT
VDDA0V9_SERDES_1
VDDA0V9_SERDES_2
VDDA0V9_SERDES_3
VDDA0V9_SERDES_4
VDDA0V9_SERDES_5
USB2_0V9_1
USB2_0V9_2
VDDA2V5_SERDES_1
VDDA2V5_SERDES_2
VDDA2V5_SERDES_3
VDDA2V5_SERDES_4
USB2_VDD3V3
VDDA2V5_REFPLL
VDDD0V9_REFPLL_1
VDDA0V9_REFPLL_2
VSSA_REFPLL_1
VSSA_REFPLL_2
VSSA_REFPLL_3
VSSA_REFPLL_4
VSSA_REFPLL_5
VSSA_REFPLL_6
VSSA_REFPLL_7
VSSA_REFPLL_8
PLL0_TSTA
PLL1_TSTA
XTAL1_IN
XTAL2_OUT
PCIE_SATA_REF0_P
PCIE_SATA_REF0_N
PCIE_SATA_REF1_P
PCIE_SATA_REF1_N
PCIE_SATA_REF2_P
PCIE_SATA_REF2_N
REFPLL_TSTA
IFE_REF0_N
IFE_REF0_P
Y6
25 MHz
NOPOP
Test Point
TP32
TP33
TP34
L93
L94
L95
L96
L97
L98
C834
C835
C836
C837
C838
C839
C840
C841
C842
C843
C844
C845
C846
C847
C848
C849
C850
C851
C852
C853
C854
C855
C856
C857
R711
R712
R713
R714
R715
R716
R717
R718
R719
R720
R721
R722
R723
R724
R725
R726
R727
R728
R729
R730
R731
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R738
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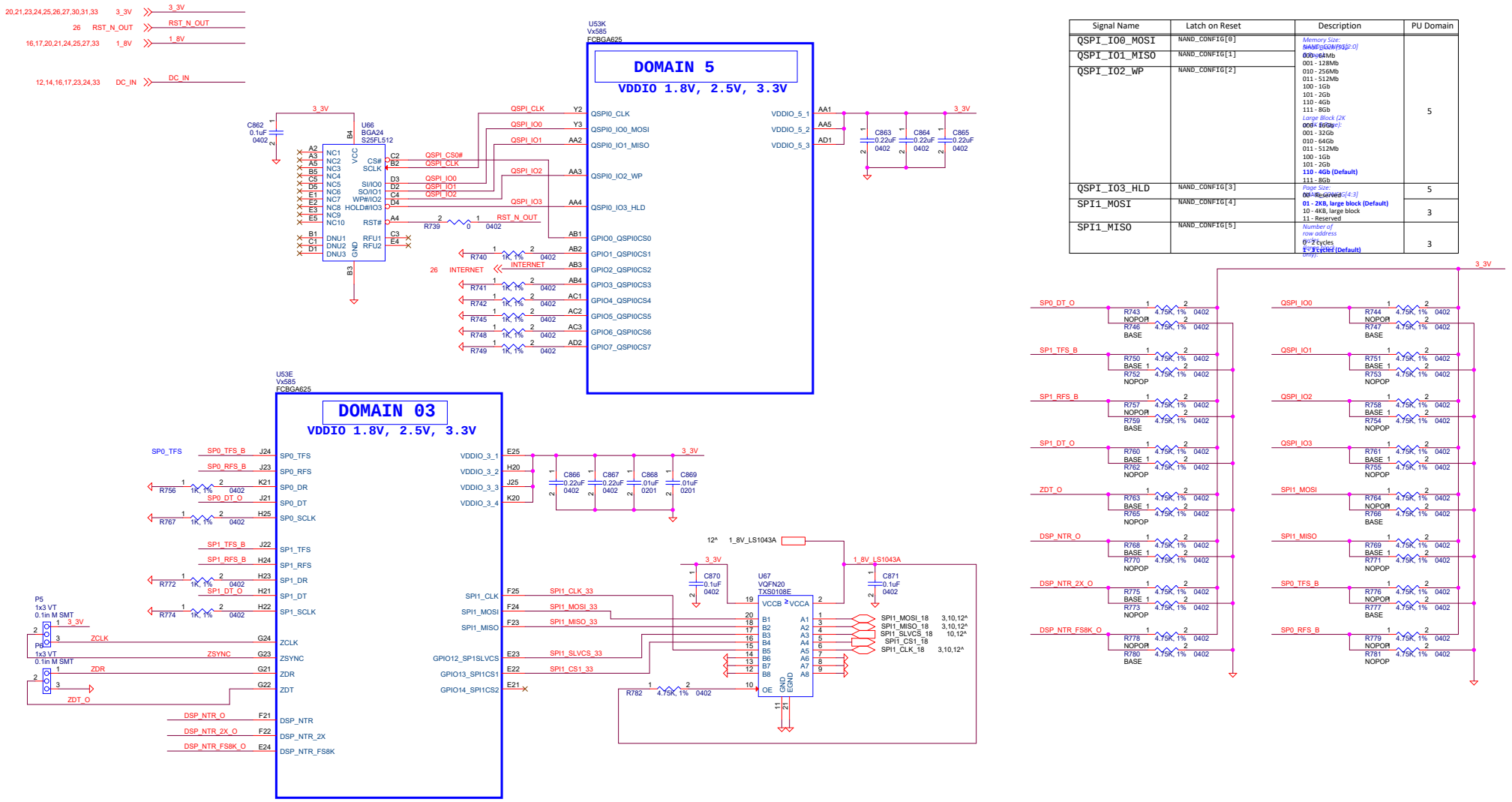

Signal Name	Latch on Reset	Description	PU Domain
QSPI_IO0_MOSI	NAND_CONFIG[0]	*Memory Size: NAND_CONFIG[5:3]* 000 - 64Mb 001 - 128Mb 010 - 256Mb 011 - 512Mb 100 - 1Gb 101 - 2Gb 110 - 4Gb 111 - 8Gb *Large Block (2K page size): NAND_CONFIG[2:0]* 000 - 16Gb 001 - 32Gb 010 - 64Gb 011 - 512Mb 100 - 1Gb 101 - 2Gb **110 - 4Gb (Default)** 111 - 8Gb	5
QSPI_IO1_MISO	NAND_CONFIG[1]		
QSPI_IO2_WP	NAND_CONFIG[2]		
QSPI_IO3_HLD	NAND_CONFIG[3]	*Page Size: NAND_CONFIG[4:3]* 00 - Reserved **01 - 2KB, large block (Default)** 10 - 4KB, large block 11 - Reserved	5
SPI1_MOSI	NAND_CONFIG[4]		3
SPI1_MISO	NAND_CONFIG[5]	*Number of row address cycles: NAND_CONFIG[6]* 0 - 2 cycles **1 - 3 cycles (Default)**	3

Pin	Latch on Reset	Description	Power Domain
SP0_TFS	GMAC_CONFIG_0[0]	*Set GIGE interface mode for the 3 GIGE ports:* 00 - RMII 01 - RMII **10 - RGMII (Default)** 11 - Reverse RGMII	3
SP0_RFS	GMAC_CONFIG_0[1]		
SP0_DT	GMAC_CONFIG_1[0]		
SP1_TFS	GMAC_CONFIG_1[1]		
SP1_RFS	GMAC_CONFIG_2[0]		
SP1_DT	GMAC_CONFIG_2[1]		
ZDT	ZARLINK_SILABS_SLIC_SEL	*Select*