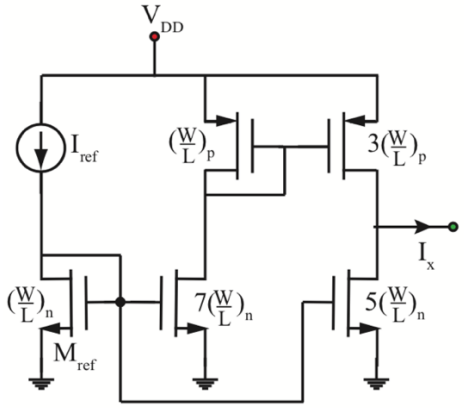
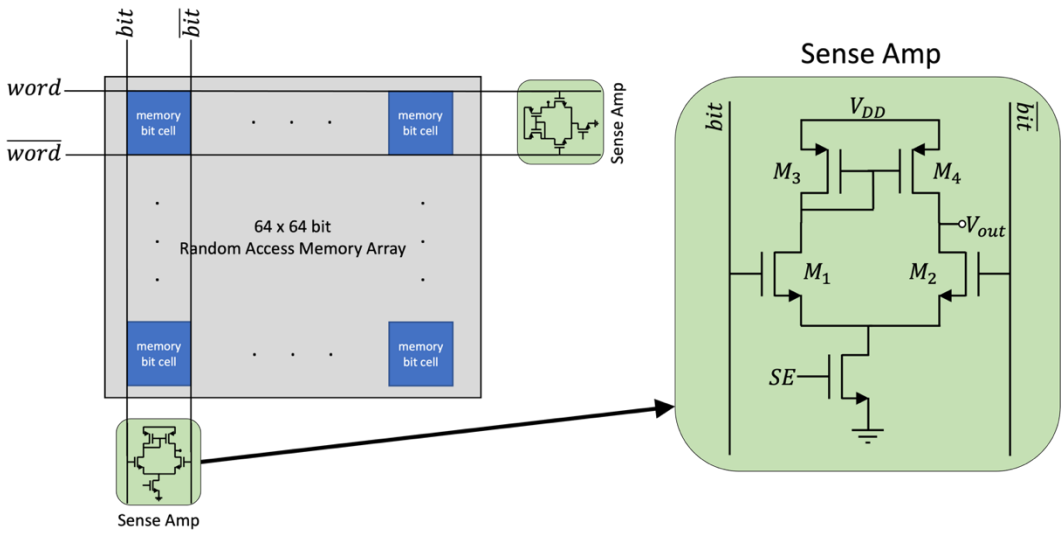
Optional practice problems from Razavi textbook: 10.11, 10.18, 10.20, 10.51, 10.52, 10.55, 10.66, 10.68, 16.13 (or 15.13 in 2nd Edition of book), 16.18 (or 15.18 in 2nd Edition of book), 16.19 (or 15.19 in 2nd Edition of book), 16.22 (or 15.22 in 2nd Edition of book), 11.21, 11.24, 11.25

1. **Scaling Current Mirrors.** Consider the following current mirror circuit with differing aspect ratios of the nmos and pmos devices as shown. If the electron mobility is 3 times the hole mobility, i.e. $\mu_n = 3\mu_p$, find a relationship between I_x and I_{ref}. Prove along the way that the ratio of the mobilities does not matter here. Assume there is a path to ground at the node where I_x is flowing into.



2. **Process Variation.** You are designing a new 64×64 bit Random Access Memory (RAM) array technology and have included differential "sense" amplifiers at the end of each of the rows and columns of the array. The sense amp takes differential inputs from the bit and $\overline{bit}$ (inverted bit signal) lines or $word$ and $\overline{word}$ (inverted word signal) lines as shown in the figure below. However, each of these amplifiers needs a set of identical transistors to form the current mirror at the top of the sense amp (used to provide a single ended output from the amplifier) and another set to form the common source parts of the differential amplifier as in the topology shown. You intentionally design all the transistors in the sense amp to have *the same chosen* $\left(\frac{W}{L}\right)$.



Your memory array needs to operate at a minimum of *98% bit functionality* in order for it to be suitable for the consumer market. You are told by the foundry that will fabricate your memory chip, that *process variation means 0.5% of your devices will be different from your specifications*. However, you realize that if either of the current mirror transistors or if either of the common source transistors has a different $\left(\frac{W}{L}\right)$ compared to its counterpart, it will result in a "failed" (asymmetric) sense amp. *Will you meet your 98% spec?*

Steps to approaching this problem are as follows:

a. Use the process variation rate to calculate the probability that a single sense amp will NOT fail. Keep in mind that there are 4 key transistors in each sense amp and if any one of them sees process variation, the sense amp is said to "fail." (This is obviously a major simplification of process variation… but for simplicity, we won't deal with standard deviations or continuous distributions of $\left(\frac{W}{L}\right)$ sizes.)

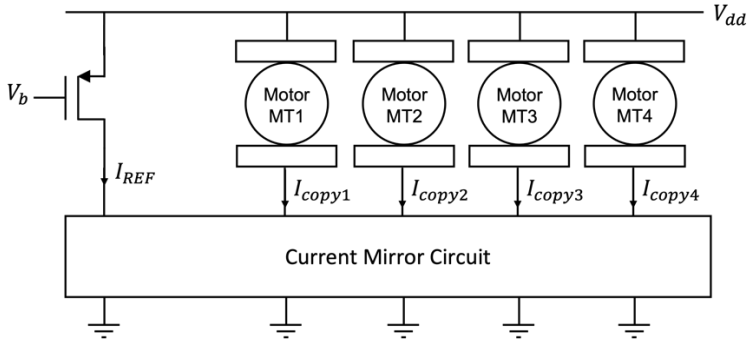
b. Multiply the probability from (a) by the total number of sense amps (which is equal to the number of rows + number of columns in the array), to get the number of fully operational sense amps. The remaining quantity are the number of failed sense amps.

c. Evaluate how many bits in the memory array are inaccessible as a result of these sense amp failures. (The total number of bits is equal to number of rows*number of columns.) In the best-case scenario, half the failed sense amps will be along the rows and the other half of the failed amps will be along the columns. In the worst-case scenario, ALL the failed sense amps will be along one side (either the rows or the columns). Think about why! Calculate the inaccessible bits based on the worst-case scenario. The remaining quantity are the accessible bits.

d. Divide the number of *accessible* bits by the total number of bits to determine the remaining number of functional bits in the array. Did you meet your required memory functionality specification?

3. **Motor Driver Amplifier Design.** A robot car with four wheels has a separate motor to control the rotation speed of each wheel. To move straight, the robot needs to have all of its wheels rotating at the same speed despite inconsistencies across the motors controlling

the wheels. The motors MT1, MT2, MT3, and MT4 shown below control to the front left, front right, back left, and back right wheels, respectively. ***However, for the same amount of current, MT1 rotates twice as fast as MT2; MT2 rotates ¾ the speed of MT3 and 2/3 the speed of MT4.*** Design a current mirror circuit that consumes a maximum power of 60 W and provides the required current copies to enable the four motors to rotate at the same speed. Assume current is directly proportional to rotation speed. Also, ignore channel length modulation ($\lambda = 0$) and assume $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $V_{th,n} = 2\ V$, $|V_{th,p}| = 1.1\ V$.



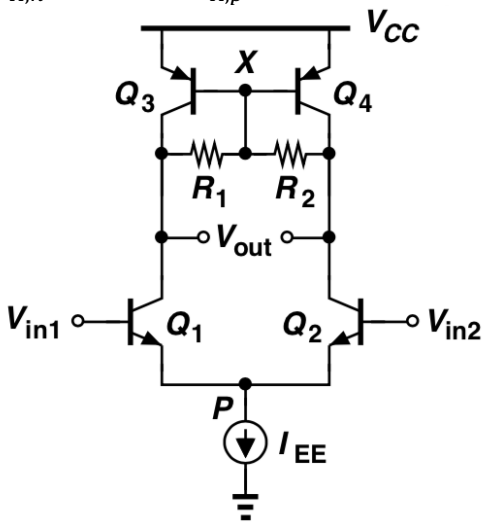
a. Design constraints:
   i. Maximum power consumption is 60 W.
   ii. Your rail voltage is $V_{dd} = 12\ V$.
   iii. Design the circuit by using a single pmos current source to produce the reference current, I_{REF}, as shown. You will need to choose V_b.
   iv. You will need to size all of the transistors, i.e., choose their $\left(\frac{W}{L}\right)$.

b. Simulate the circuit in LTspice **using the framework included with the homework on Canvas**.
   i. You will need to add transistors to the model. To do so:
      1. Select component type: nmos4 and/or pmos4
      2. Wire each bulk terminal to the transistor's source terminal.
      3. In the properties of the transistor, change the MODEL attribute to either 3150NMOS or 3150PMOS for nmos and pmos, respectively.
      4. In the properties of the transistor, enter values for L and W. Set your values in the range μm.
      5. Make the values of L and W visible on the schematic by pressing cntrl (or cmmd) while you right click on the device. Then click toggle the visibility of the L and W attribute so that it has an X.
      6. Assign the pmos transistor's gate voltage to be the value V_b you chose in your analytical design. Run the simulation and check your operating point power consumption. Hint: you may need to slightly tweak the value of V_b to get the power you wanted. This is necessary since the L and W values will be rounded and not exact. So, even the slightest change in V_b affects the saturation current (and power consumption) quadratically. *Make sure your final value for V_b is visible on the schematic.*

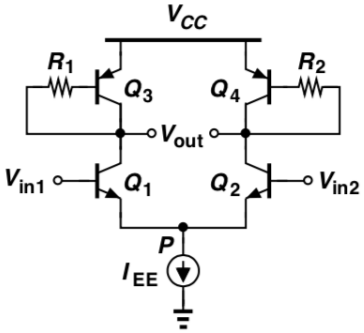
c. Prove that your amplifier works by submitting:
   i. ***a screenshot of your circuit design***

ii. ***a screenshot of your DC bias point*** (If you are on a Mac machine, the operating point does not open automatically. You will need to open the file with a .log extension and submit the "Operating Bias Point Solution" within that.) The current coming out of the power supply will be -I(Vdd). You can use that to check if you are within power spec.

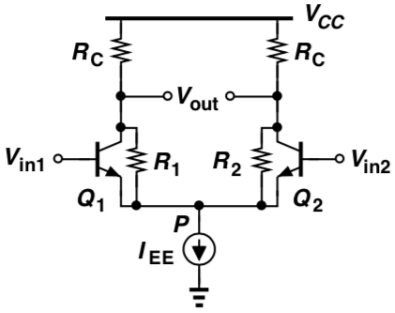
4. **BJT Differential Amplifier Tail Current.** The circuit below must provide a gain of 50 with $R_1 = R_2 = 5\ k\Omega$. If $V_{A,n} = 5\ V$ and $V_{A,p} = 4\ V$, calculate the required tail current.



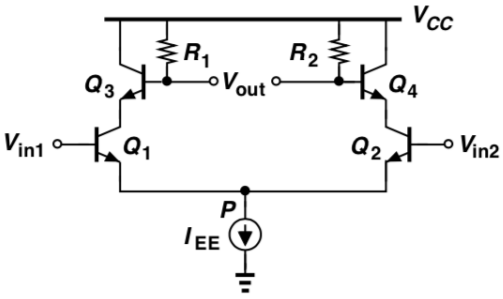
5. **BJT Differential Amplifier Gains.** Assuming perfect symmetry and $V_A < \infty$, compute the differential voltage gain of each stage depicted below.



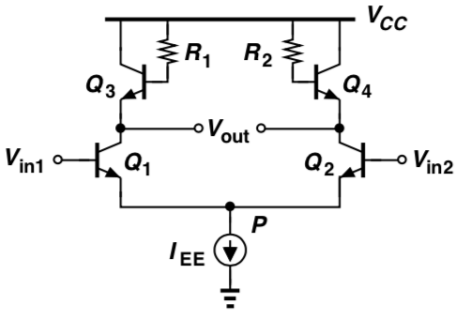
(a)



(b)

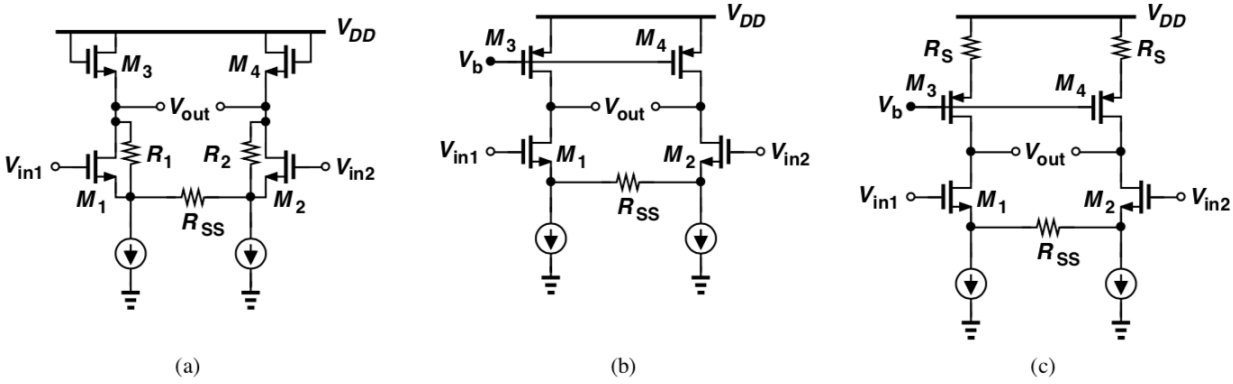


(c)



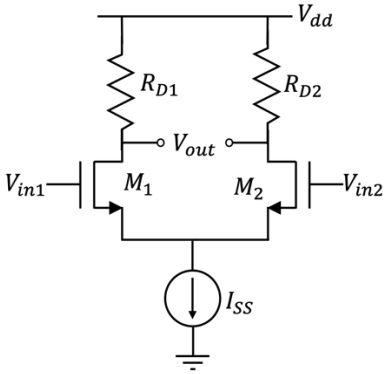
(d)

6. **MOS Differential Amplifier Gains.** Calculate the differential voltage gain for the circuits depicted below. Assume perfect symmetry and $\lambda > 0$. You may need to compute the gain as $A_v = -G_m R_{out}$ in some cases.

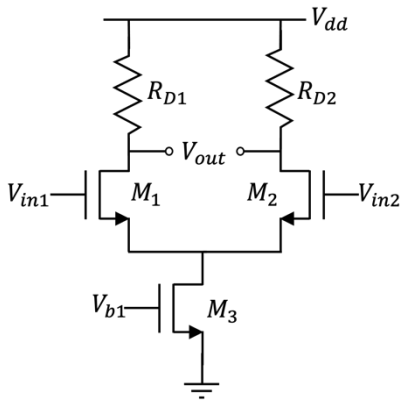


(a) (b) (c)

7. **Common Mode Rejection**. The differential amplifier below has a slight mismatch in resistors, $R_{D1} = 4.7\ k\Omega$ and $R_{D2} = 4.704\ k\Omega$. Assume M1 and M2 are identical and that $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_{th,n} = 0.4\ V$, $V_{DD} = 5\ V$, and $I_{SS} = 1\ mA$.



   a. Derive the expressions (in terms of resistor values and small signal parameters) for the common mode to differential mode conversion gain ($A_{v_{CM-DM}}$) and CMRR in this case when the tail current is given by an ideal current source and the MOSFETs are ideal ($\lambda = 0$). Simulate this scenario in LTspice using the provided framework.
      i. Plot the transient solution for vout1-vout2 by probing the vout1 node on the circuit after running the simulation. Then, in the graph window, right click on the title "V(vout1)" and a new window appears. In this window, revise the graphed parameter to be V(vout1)-V(vout2).
      ii. Add a trace for the input signal to the graph as well, by probing the vin1 terminal. Then, in the graph window, right click on the title "V(vin1)" and a new window appears. In this window, revise the graphed parameter to be V(vin1)-V(vin2).
      iii. Add a trace for the common mode input signal to the graph as well by probing the Vcm terminal.
      iv. ***Submit a screenshot of your graph containing all three signals: output voltage, input voltage, and common mode voltage.***



b. Now consider the more realistic situation where the MOSFETs are non-ideal ($\lambda_n = 0.1\ V^{-1}$) and a MOSFET current source is used for the tail current, instead of the ideal current source, as shown in the figure above.
   i. Derive the expressions (in terms of resistor values and small signal parameters) for the new common mode to differential mode conversion gain ($A_{v_{CM-DM}}$) and CMRR.
   ii. Simulate this scenario in LTspice using the provided framework. ***Again, submit a screenshot of your graph containing all three signals: output voltage, input voltage, and common mode voltage.***
   iii. Calculate the value of the CMRR using the expression you derived in part (i) and the small signal parameters you determine from the simulated circuit behavior. *Remember that the small signal parameters are evaluated based on the DC operating point! Also, keep in mind which transistor is contributing which small signal parameter to the equation.*
   iv. Comment on the magnitude of the CMRR and the degree of common mode noise seen in your output signal.

8. **Miller Theorem.** Use Miller's theorem to estimate the input and output poles of the circuit shown below. Assume $V_A = \infty$ and neglect other capacitances.