Survey on MCU Components Part 01

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Enabling and disabling GPIO peripheral clock (RCC_AHB1ENR):

RCC_AHB1ENR has the ability for enabling and disabling bits to control the clock for various GPIO ports. In RCC_AHB1ENR, we will find the bit positions to control the clock for various GPIO ports from GPIOA to GPIOI. GPIO peripheral clock will be enabled if the corresponding bit is “1”. If the corresponding bit is “0” then the clock is disabled.

General-purpose I/Os (GPIO)

Each General-Purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection register (GPIOx_AFRH and GPIOx_AFRL).

Registers related with GPIO Port and Pins with their Abbreviations:

The following abbreviations are used in register descriptions (x = A to H):

GPIO Registers	Small Description / Abbreviation
• **GPIOx_MODER**	GPIO port Mode Register.
• **GPIOx_OTYPER**	GPIO Output Type Register. a) **Push-Pull** b) **Open Drain**
• **GPIOx_OSPEEDR**	GPIO Output Speed Register.

• **GPIOx_PUPDR**	GPIO port Pull-Up / Pull-Down Register.
• **GPIOx_BSRR**	GPIO port Bit Set and Reset Register.
• **Alternate Function (AF):** **a) GPIOx_AFRL** **b) GPIOx_AFRH**	a) GPIO Alternate Function Low Register. b) GPIO Alternate Function High Register.

Other related Registers with GPIO Port and Pins are:

The following abbreviations are used in register descriptions (x = A to H):

GPIO Registers	Small Description / Abbreviation
GPIOx_IDR	GPIO port Input Data Register.
GPIOx_ODR	GPIO port Output Data Register.
GPIOx_LCKR	GPIO port configuration Lock Register.
GPIOx_ASCR	GPIO port Analog Switch Control Register.

Functions and roles of the GPIOx registers:

- **Mode Register** (GPIOx_MODER)**:**

The GPIOx_MODER register is a 32-bit memory-mapped control register to configure upto 16 I/Os. The GPIOx_MODER register is used to select the I/O direction (input, output, AF, analog). The configuration length of each port mode register is 2 bits.

Bits 2y:2y+1:
These configuration bits are written by software to configure the I/O direction mode:

00: Input (reset state)
01: General purpose output mode
10: Alternate function mode
11: Analog mode

Very commonly used modes are input mode, general purpose output mode and alternate function mode. ADC or DAC uses Analog mode. Also, whenever a microcontroller undergoes reset all the pins of different GPIO ports will be by default in the input state.

- **Output Type Register** (GPIOx_OTYPER):

The GPIOx_OTYPER register is a 32-bit memory-mapped control register to configure upto 16 I/Os. The GPIOx_OTYPER register is used to select the output type-

a) **Push-Pull mode:** In push-pull mode “0” in the Output data register activates the N-MOS whereas a “1” in the Output data register activates the P-MOS. The data present on the I/O pin is sampled into the input data register over every AHB1 clock cycle. Read access to the input data register gets the I/O state. Read access to the output data register gets the last written value. To set GPIO output type register in push-pull mode, in GPIO_OTYPER register bit is set to “0”.

b) **Open Drain mode:** In Open-drain configuration, PMOS doesn’t exist, and two output possibilities are high or floating. A “0” in the Output data register activates the N-MOS and the I/O pin driven to the ground. Whereas “1” in the Output data register leaves the port in Hi-Z (the P-MOS is never activated), so I/O state is not defined. To solve this issue either activate an internal pull-up resistor or give an external pull-up resistor. So, once a pull-up resistor is activated, the I/O pin gets its state to VDD. To set GPIO output type register in open-drain mode, in GPIO_OTYPER register bit is set to “1”.

Bits 31:16 are Reserved. Only Bits 15:0 are used.
The configuration bits are written by software to configure the output type of the I/O port.

0: Output Push-Pull (reset state)
1: Output Open-Drain

- **Speed Register** (GPIOx_OSPEEDR):

The GPIOx_OSPEEDR register is a 32-bit memory-mapped control register to configure upto 16 I/Os. The GPIOx_OSPEED register is used to select the speed (the I/O speed pins are directly connected to the corresponding GPIOx_OSPEEDR register bits whatever the I/O direction). It is only applicable when the GPIO pin is in output mode. By using the GPIO output speed register, one can configure the GPIO transitions from

high to low and low to high, which means the slew rate of a pin can be controlled by GPIO output speed register.

Bits 2y:2y+1:
These bits are written by software to configure the I/O output speed.

00: Low speed
01: Medium speed
10: Fast speed
11: High speed

- **Pull-UP / Pull-Down Register** (GPIOx_PUPDR):

The GPIOx_PUPDR register is a 32-bit memory-mapped control register to configure upto 16 I/Os. The GPIOx_PUPDR register is used to select the Pull-Up / Pull-Down whatever the I/O direction. GPIO Pull-Up and Pull-Down registers are used to control the internal or external Pull-Up and Pull-Down registers.

Bits 2y:2y+1:
These bits are written by software to configure the I/O pull-up or pull-down.

00: No pull-up, pull-down
01: Pull-Up
10: Pull-Down
11: Reserved

- **GPIO port Bit Set and Reset Register** (GPIOx_BSRR):

The Bit Set and Reset register (GPIOx_BSRR) is a 32-bit register which allows the application to set and reset each individual bit in the output data register (GPIOx_ODR). The purpose of the GPIOx_BSRR register is to allow atomic read/modify accesses to any of the GPIO registers. In this way, there is no risk of an IRQ occurring between the read and the modify access. The GPIOx_BSRR register provides a way of performing atomic bitwise handling. It is possible to modify one or more bits in a single atomic AHB1 write access. This register consists of two write-only bit masks, each 16-bit wide. The high half- 16 bits to 31 is the reset mask. Writing a 1 to any of these bits clear bit N-16 in the GPIO_ODR. The low half - bits 0 to 15 is the set mask. Writing a 1 to any of these bits sets the corresponding bit in the GPIO_ODR.

Bits 31:16 BRy: Port x reset bit y
These bits are write-only and can be accessed in word, half-word or byte mode. A read to these bits return the value 0x0000.

0: No action on the corresponding ODRx bit
1: Resets the corresponding ODRx bit

Bits 15:0 BSy: Post x set bit y
These bits are write-only and can be accessed in word, half-word or byte mode. A read to these bits return the value 0x0000.

0: No action on the corresponding ODRx bit
1: Sets the corresponding ODRx bit

- **Alternate Function (AF):**

Two registers are provided to select one out of the sixteen Alternate Function inputs/outputs available for each I/O. With these registers, one can connect an alternate function to some other pin as required by an application. This means that a number of possible peripheral functions are multiplexed on each GPIO using these two alternate registers-

a) **GPIO Alternate Function Low Register** (GPIOx_AFRL): GPIOx_AFRL contains the multiplexer settings for port bits 0 to 7.

   Bits 31:0 Alternate function selection for port x bit y
   These bits are written by software to configure alternate functions I/Os.

   AFRLy selection:

0000: AF0	1000: AF8
0001: AF1	1001: AF9
0010: AF2	1010: AF10
0011: AF3	1011: AF11
0100: AF4	1100: AF12
0101: AF5	1101: AF13
0110: AF6	1110: AF14
0111: AF7	1111: AF15

b) **GPIO Alternate Function High Register** (GPIOx_AFRH): GPIOx_AFRH contains the multiplexer settings for port bits 8 to 15.

Bits 31:0 Alternate function selection for port x bit y
These bits are written by software to configure alternate functions I/Os.
AFRHy selection:

0000: AF0	1000: AF8
0001: AF1	1001: AF9
0010: AF2	1010: AF10
0011: AF3	1011: AF11
0100: AF4	1100: AF12
0101: AF5	1101: AF13
0110: AF6	1110: AF14
0111: AF7	1111: AF15

The application can thus select any one of the possible functions for each I/O. The AF selection signal being common to the alternate function input and alternate function output, a single channel is selected for the alternate function input/output of one I/O.

Some more functions and roles of related Registers with GPIO Port and Pins:

- **Input Data Register** (GPIOx_IDR):

The input data register (GPIOx_IDR) is a 16-bit memory-mapped data register. The input data register (GPIOx_IDR) captures the data present on the I/O pin at every AHB1 clock cycle. The data input through the I/O are stored into the input data register (GPIOx_IDR), a read-only register. Here only Bits 15:0 are used and 31:16 bits are reserved.

- **Output Data Register** (GPIOx_ODR):

The output data register (GPIOx_ODR) is a 16-bit memory-mapped data register. When the pin is configured as output, the value written to the output data register (GPIOx_ODR) is output on the I/O pin. It is possible to use the output driver in push-pull mode or open-drain mode (only the N-MOS is activated when 0 is output). GPIOx_ODR stores the data to be output, it is read/write accessible. Here only 16-bits are used in this register. So, 16 to 31 are reserved, and the 0th-bit position will control the I/O pin 0.

- **Configuration Lock Register** (GPIOx_LCKR):

It is possible to freeze the GPIO control registers by applying a specific write sequence to the GPIOx_LCKR register. The frozen registers are GPIOx_MODER, GPIOx_OTYPER,GPIOx_OSPEEDR,GPIOx_PUPDR,GPIOx_AFRL, GPIOx_AFRH.

- **Analog Switch Control Register** (GPIOx_ASCR):

GPIOx_ASCR register helps to control analog interconnection between an I/O pin and ADC input.