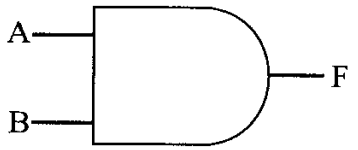
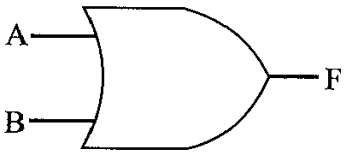
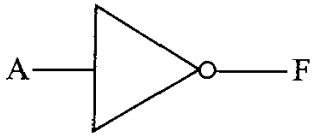
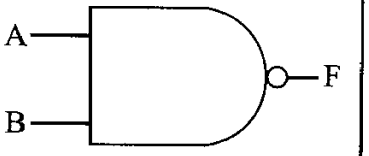
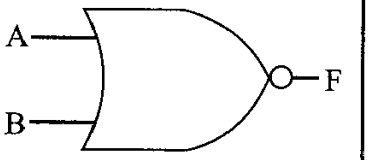
Nazwa	Symbol graficzny	Funkcja algebraiczna	Tablica prawdy
AND		$F = A \cdot B$ lub $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT		$F = \overline{A}$ lub $F = A'$	A | F 0 | 1 1 | 0
NAND		$F = (\overline{AB})$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = (\overline{A + B})$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0

RYSUNEK A.1. Podstawowe bramki logiczne

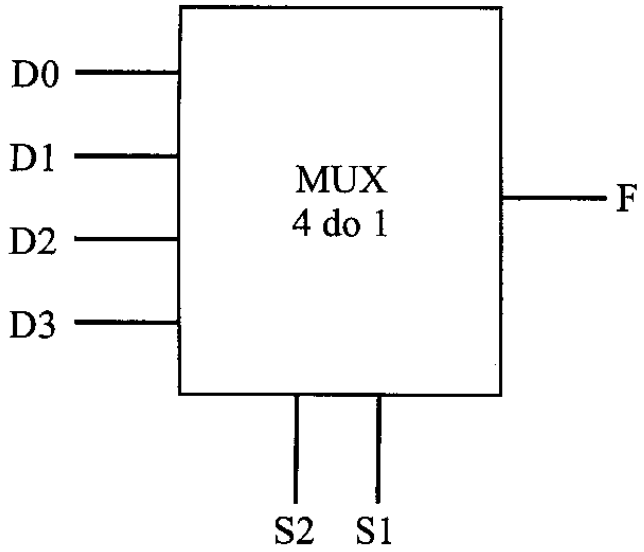
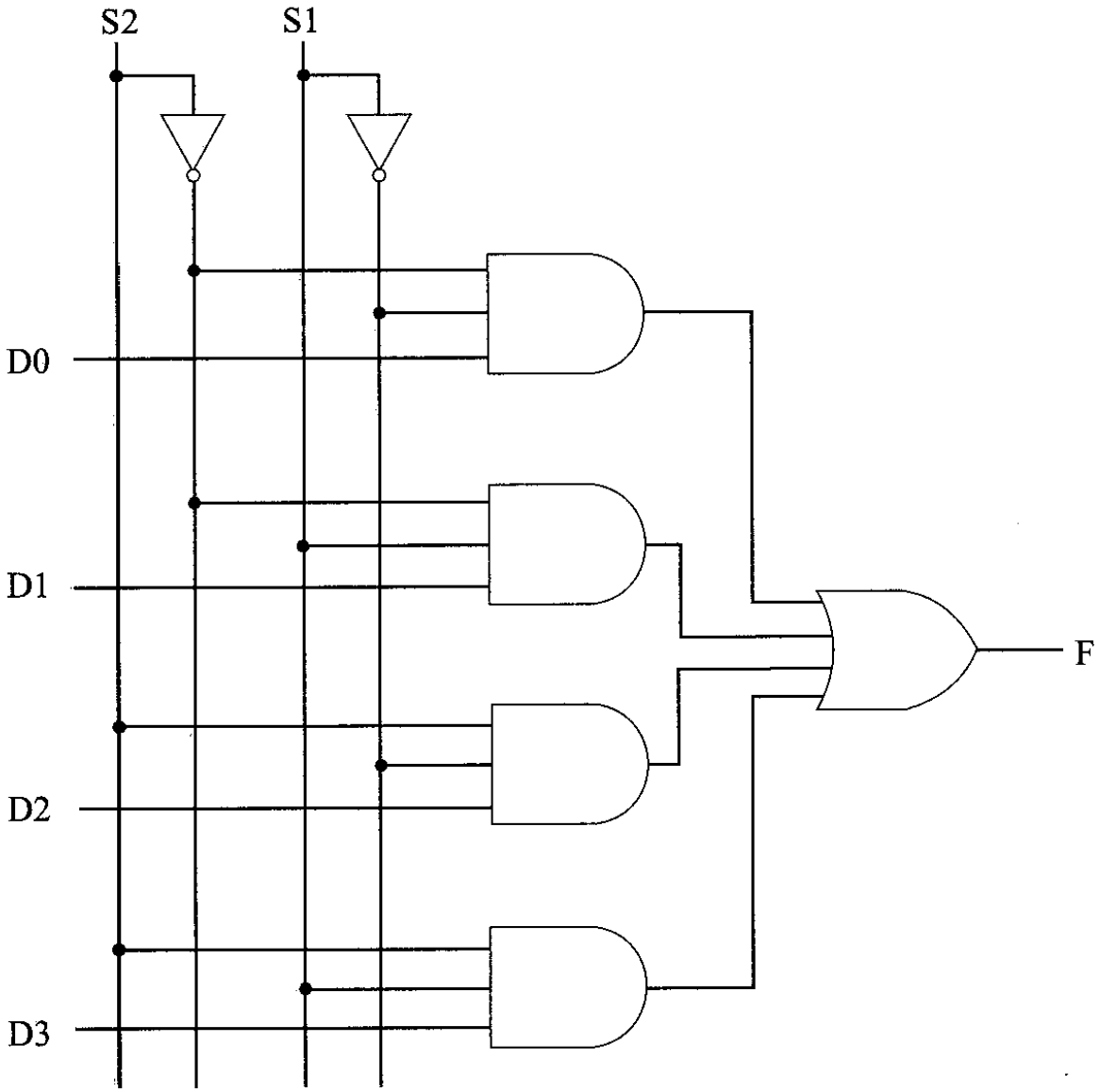


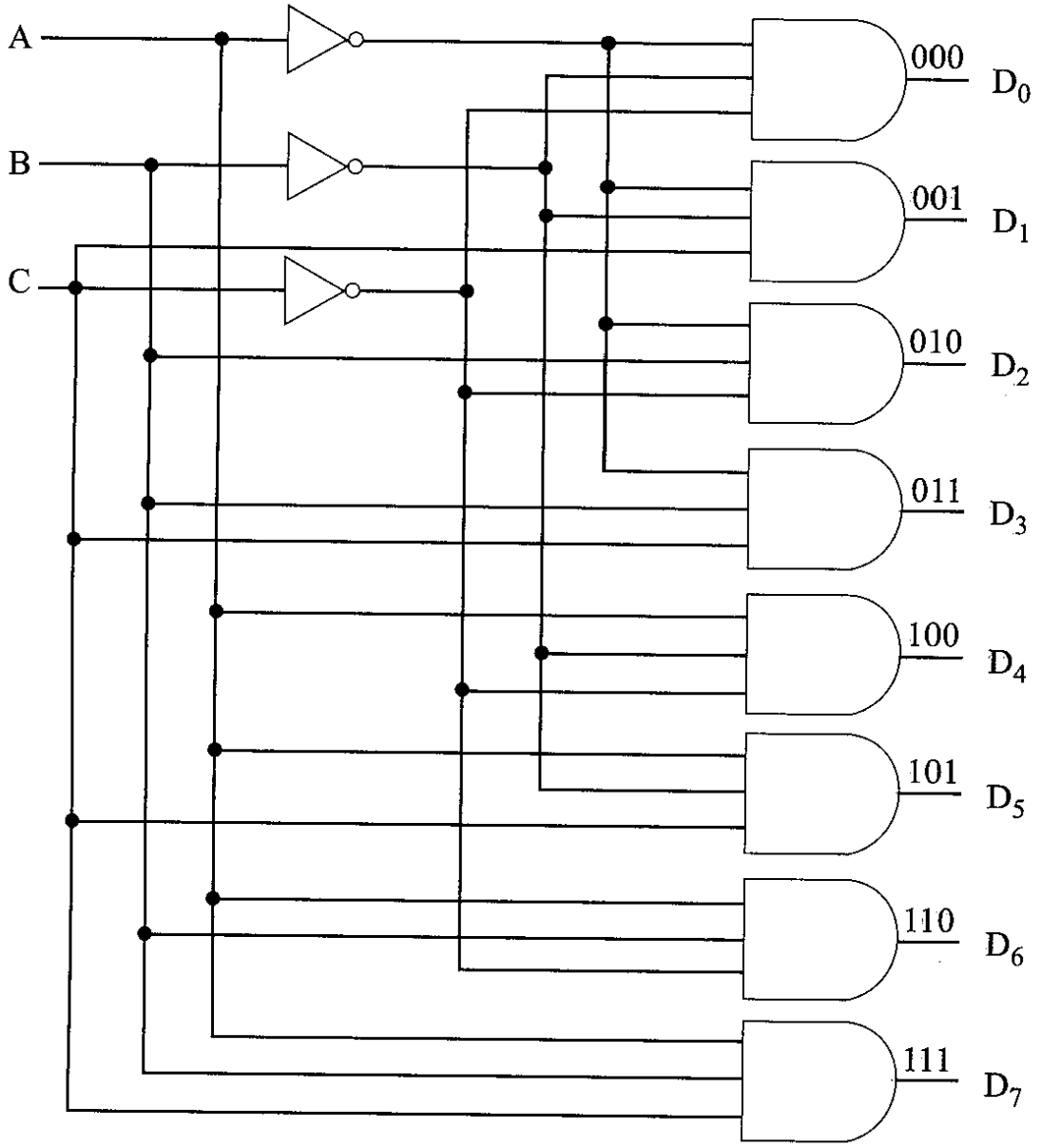
TABELA A.7. Tablica prawdy multipleksera 4 do 1

S2	S1	F
0	0	D0
0	1	D1
1	0	D2
1	1	D3

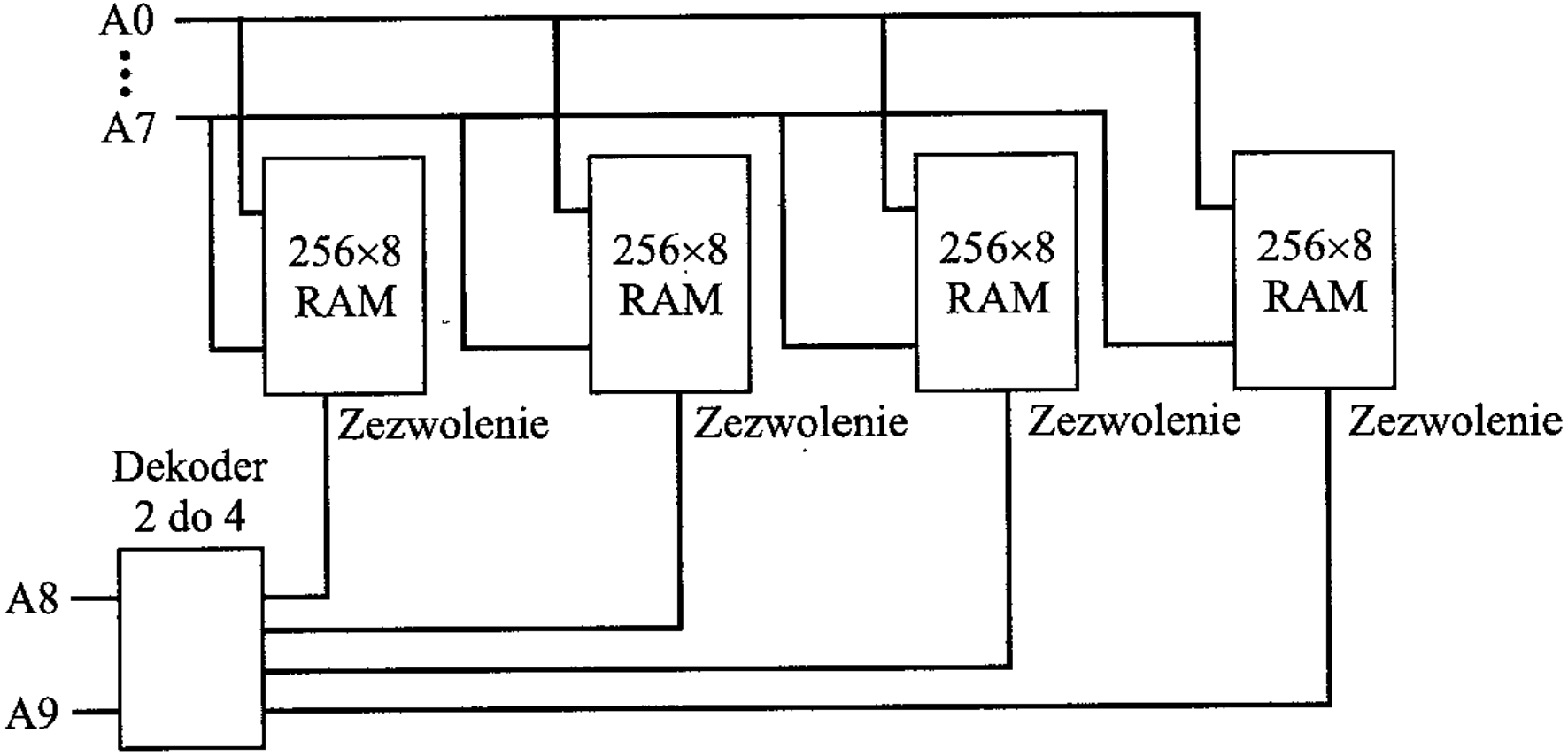
RYSUNEK A.12. Reprezentacja multipleksera 4 do 1



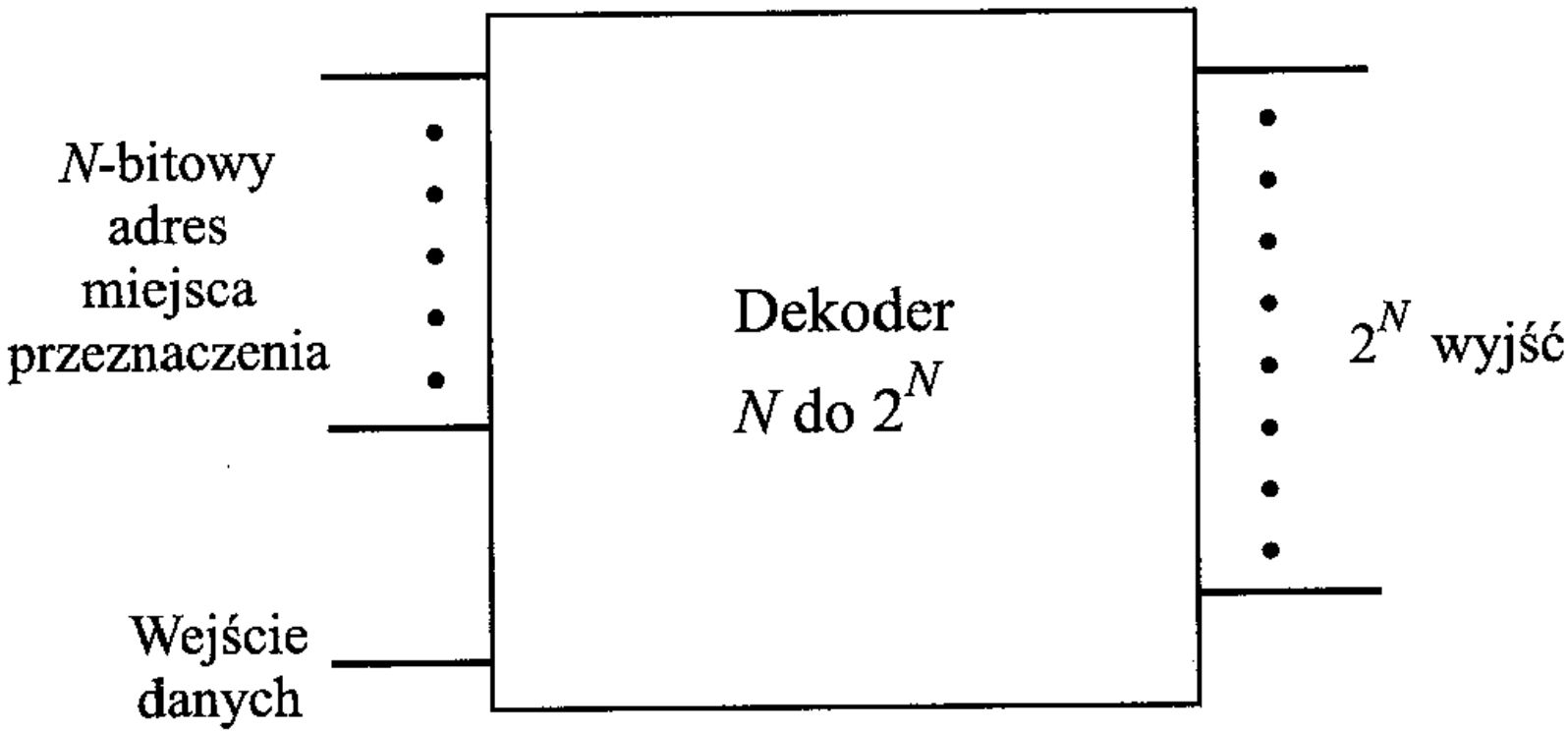
RYSUNEK A.13. Realizacja multipleksera



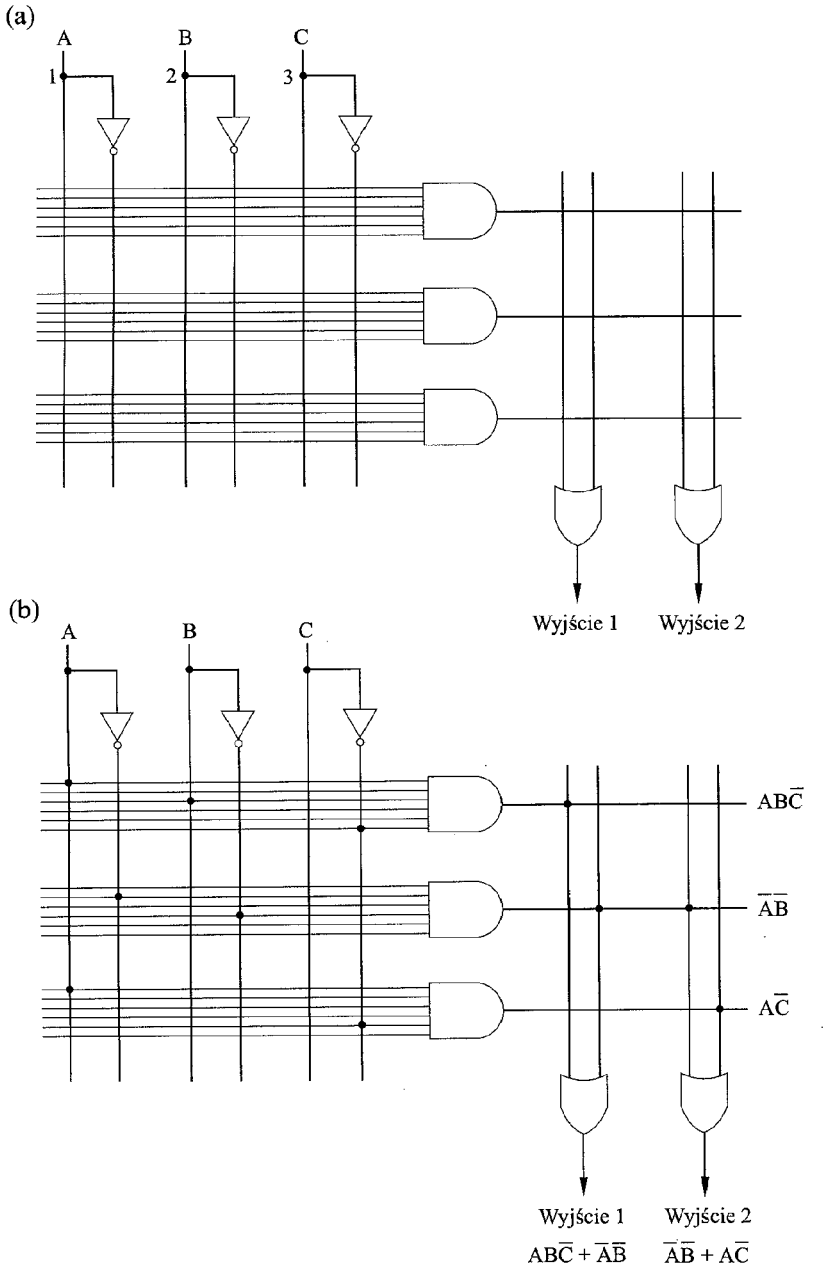
RYSUNEK A.15. Dekoder z trzema wejściami i $2^3 = 8$ wyjściami



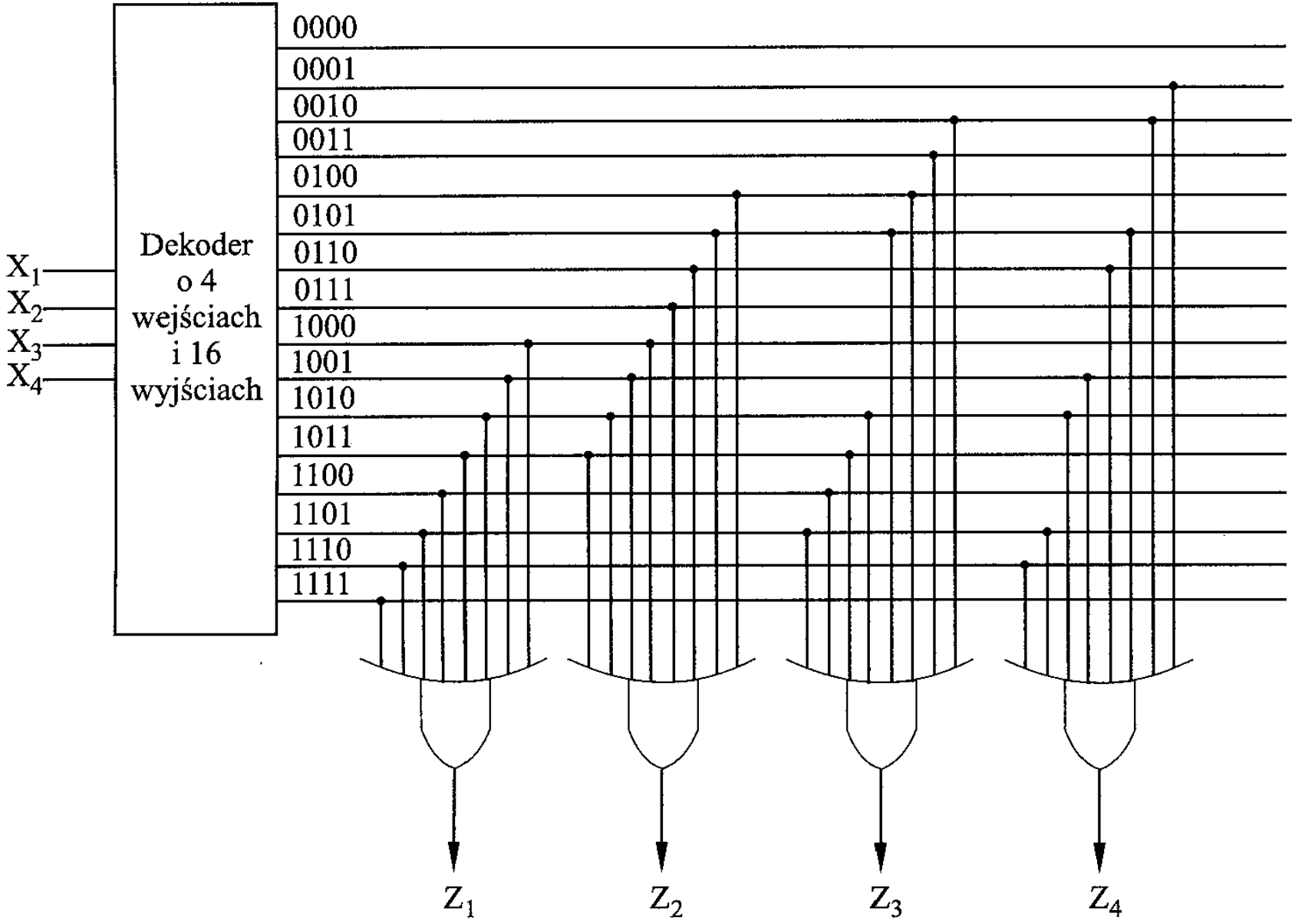
RYSUNEK A.16. Dekodowanie adresu



RYSUNEK A.17. Realizacja demultipleksera za pomocą dekodera



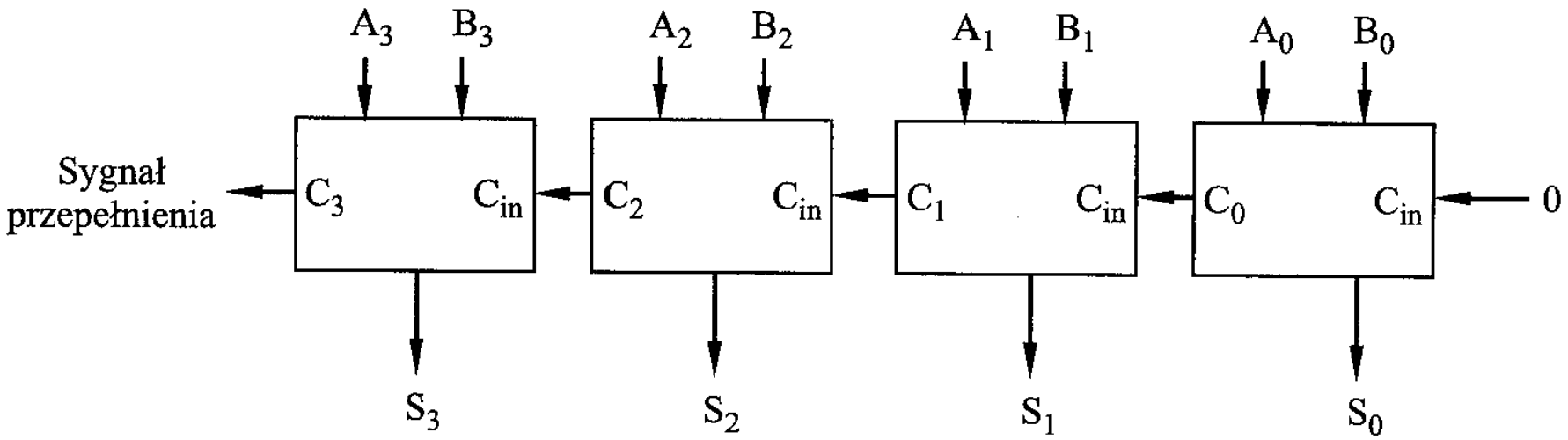
RYSUNEK A.19. Przykład programowalnej tablicy logicznej: (a) PLA o 3 wejściach i 2 wyjściach; (b) schemat połączeń PLA o 3 wejściach i 2 wyjściach



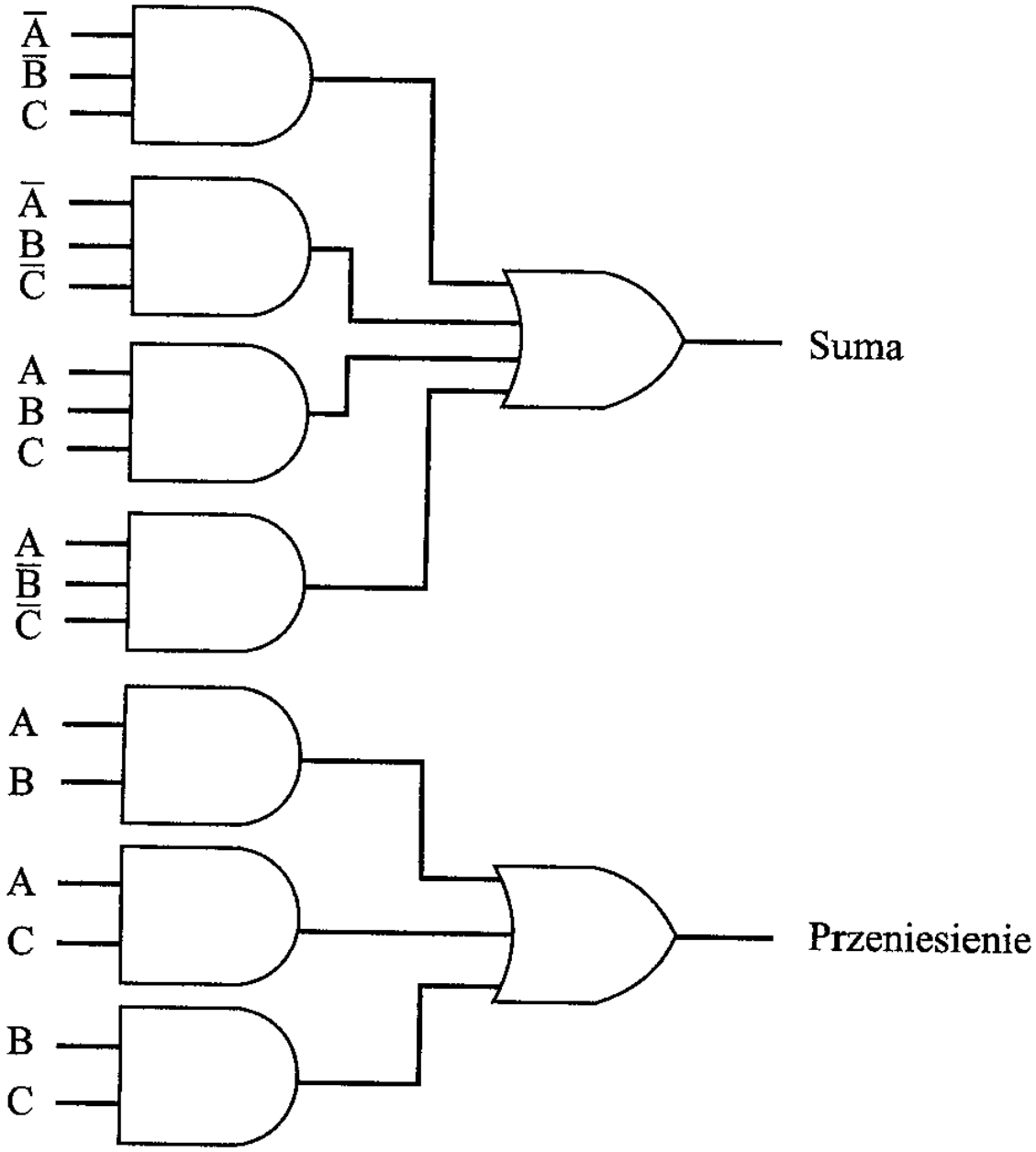
RYSUNEK A.20. 64-bitowa pamięć ROM

TABELA A.9. Tablica prawdy dodawania binarnego

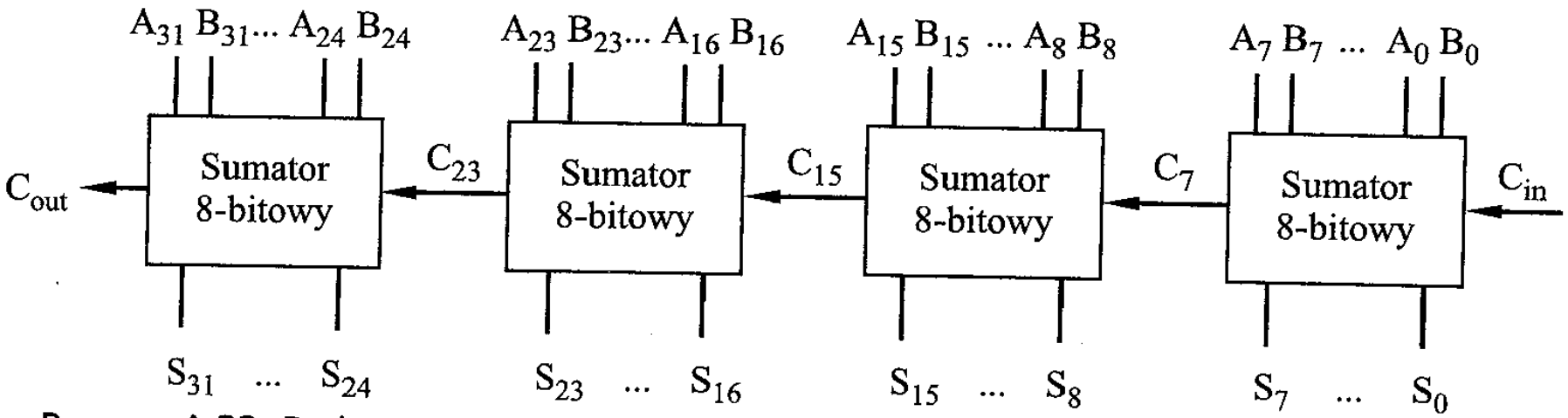
(a) Dodawanie pojedynczych bitów				(b) Dodawanie wraz z przeniesieniem				
A	B	Suma	Przeniesienie	C_{in}	A	B	Suma	C_{out}
0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	1	1	0
1	0	1	0	0	1	0	1	0
1	1	0	1	0	1	1	0	1
				1	0	0	1	0
				1	0	1	0	1
				1	1	0	0	1
				1	1	1	1	1



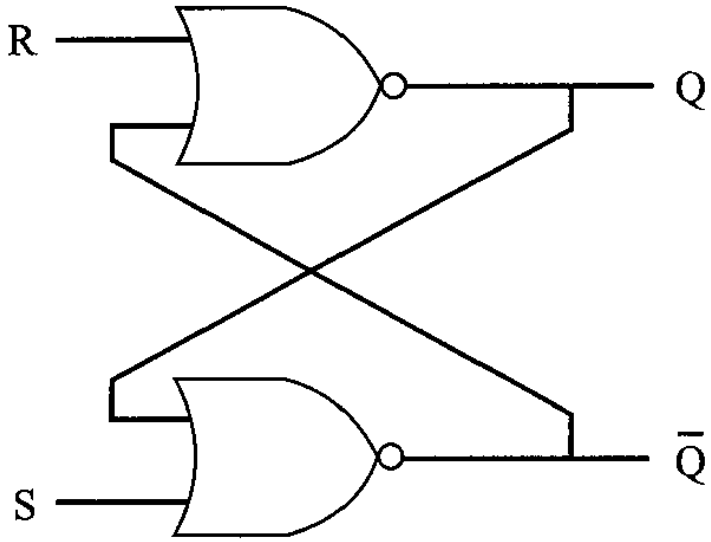
RYSUNEK A.21. Sumator 4-bitowy



RYSUNEK A.22. Realizacja sumatora



RYSUNEK A.23. Budowanie sumatora 32-bitowego za pomocą sumatorów 8-bitowych



RYSUNEK A.24. Przerzutnik S-R typu zatrzask zrealizowany za pomocą bramek NOR

TABELA A.10. Przerzutnik S-R

(a) Tablica własności

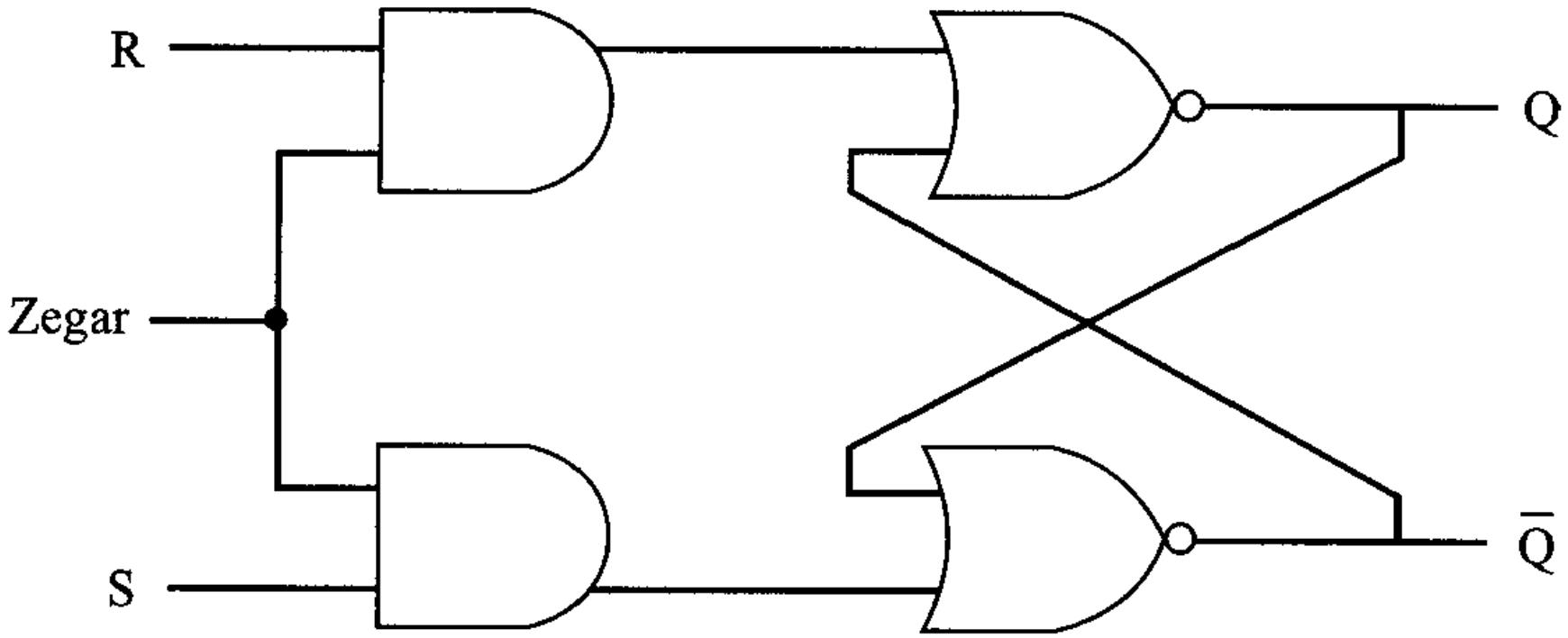
Bieżące wejścia	Stan bieżący	Stan następny
SR	Q_n	Q_{n+1}
00	0	0
00	1	1
01	0	0
01	1	0
10	0	1
10	1	1
11	0	–
11	1	–

(b) Uproszczona tablica własności

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

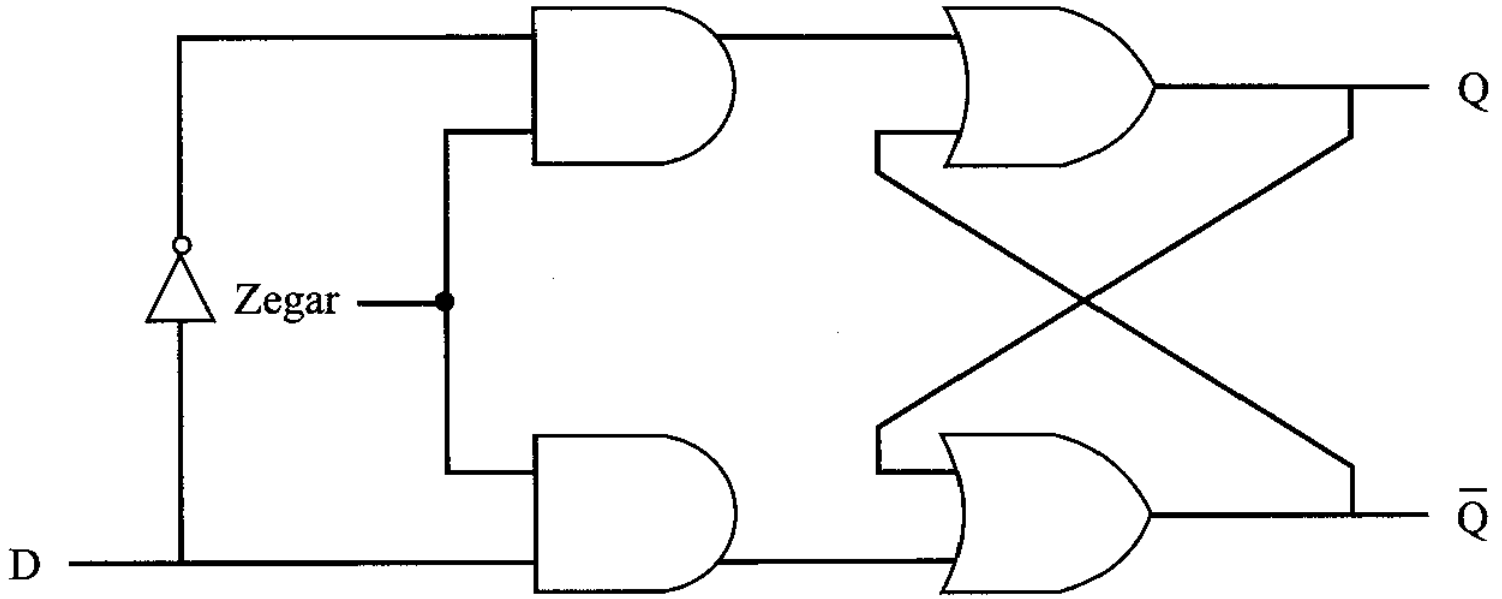
(c) Odpowiedź na szereg sygnałów wejściowych

t	0	1	2	3	4	5	6	7	8	9
S	1	0	0	0	0	0	0	0	1	0
R	0	0	0	1	0	0	1	0	0	0
Q_{n+1}	1	1	1	0	0	0	0	0	1	1

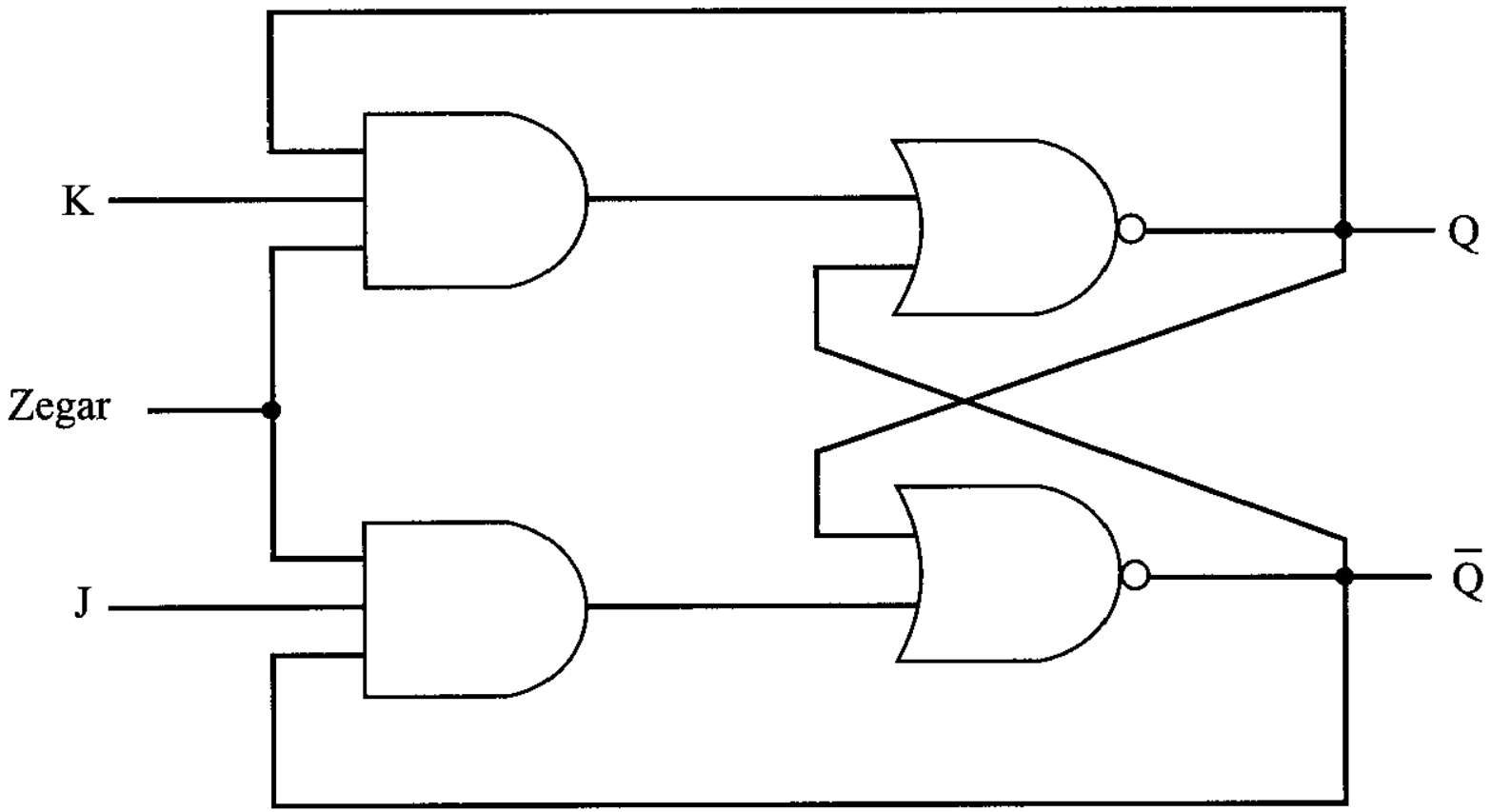


RYSUNEK A.26. Synchronizowany przerzutnik S-R

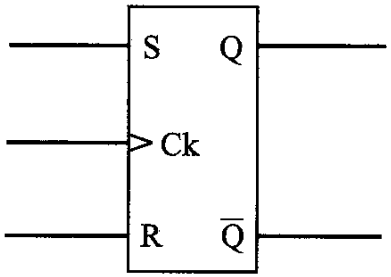
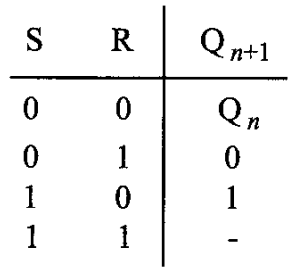
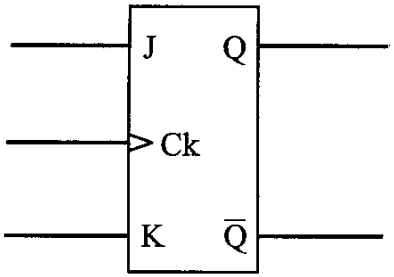
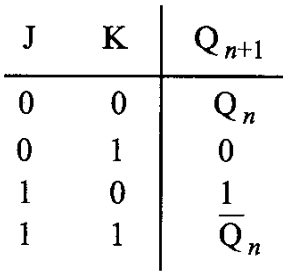
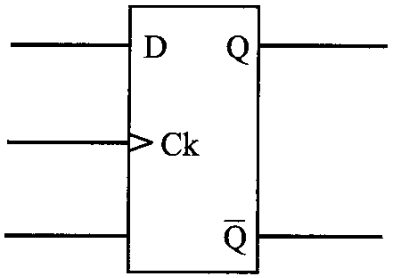
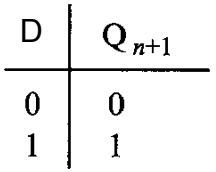
D	Q_{n+1}
0	0
1	1



RYSUNEK A.27. Przerzutnik D



RYSUNEK A.28. Przerzutnik J-K

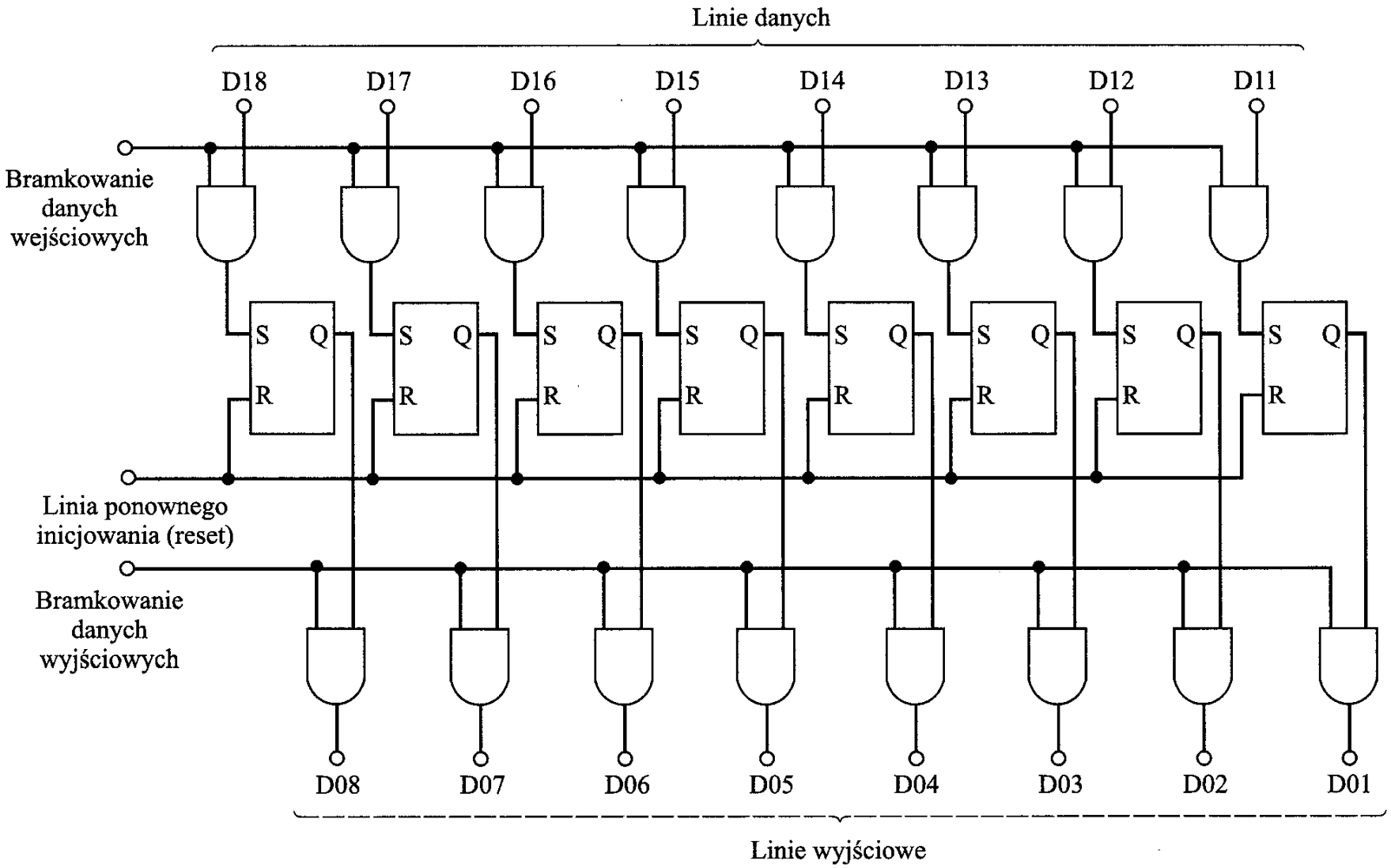
Nazwa	Symbol graficzny	Tablica stanów
S-R		
J-K		
D		

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	-

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

D	Q_{n+1}
0	0
1	1

RYSUNEK A.29. Podstawowe przerzutniki



RYSUNEK A.30. 8-bitowy rejestr równoległy