Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?

   Program and Data stored in Separate Memory
   Program and Data stored in the same Memory
   Program and data stored in Cache Memory
   All of the Above

2. Which of the following is the working cycle of the CPU?

   Decode, Execute, Fetch
   Fetch, Decode, Execute
   Fetch, Execute, Decode
   All of the Above

3. Any condition that causes a processor to stall is called _____

   Hazard
   Page fault
   System error
   None of the mentioned

4. What does the control unit generate to control other units?

   Transfer signals
   Command Signal
   Control signals
   Timing signals

5. What must the processors of all computers have?
   Control unit
   ALU
   Register
   All of these

6. Which is the fastest memory in the computer?

Cache
RAM
Register
Hard disk

7. With the help of _____, we reduce the memory access time:

SDRAM
Cache
Heaps
Higher capacity RAMs

8. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?

ISA
ANSA
Super-scalar
All of the mentioned

9. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

Super-scaling
Pipe-lining
Parallel Computation
None of the mentioned

10. A 24 bit address generates an address space of _____ locations.

1024
4096
2 48
16,777,216

11. The USA contains about 3100 counties. Suppose you have a table that
stores, for each county, its name (up to 40 characters in 8-bit ASCII), its
state (a two-letter code), its population, and its median income (both as 32-
bit numbers). How much space would the whole database take in memory?

For 1 County

Name = 40 Characters (i.e.) = 40 Byte = 40*8 = 320 Bits

State = 2 Characters = 2 Bytes = 2*8 = 16 Bits

Population = 32 Bits

Median Income = 32 Bits

Adding all the bits,

320 + 16 + 32 + 32 = 400 Bits

Total Bits for 3100 Counties

400 Bits * 3100 = 1240000 Bits

In Bytes

1240000 / 8 = 155000 Bytes

In Kilobytes

155000 / 1024 = 151.36 Kilobytes.

12. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.

a) Calculate the width of the data bus.

Max address memory = 16gb-2^34
Address bus width = 32
Total address bus = 26^32

Now,

Maximum addressable memory = total address memory * width of dress bus
2^34 = 2^32 *(WD)
2^34 – 2^32 = WD
4 = WD

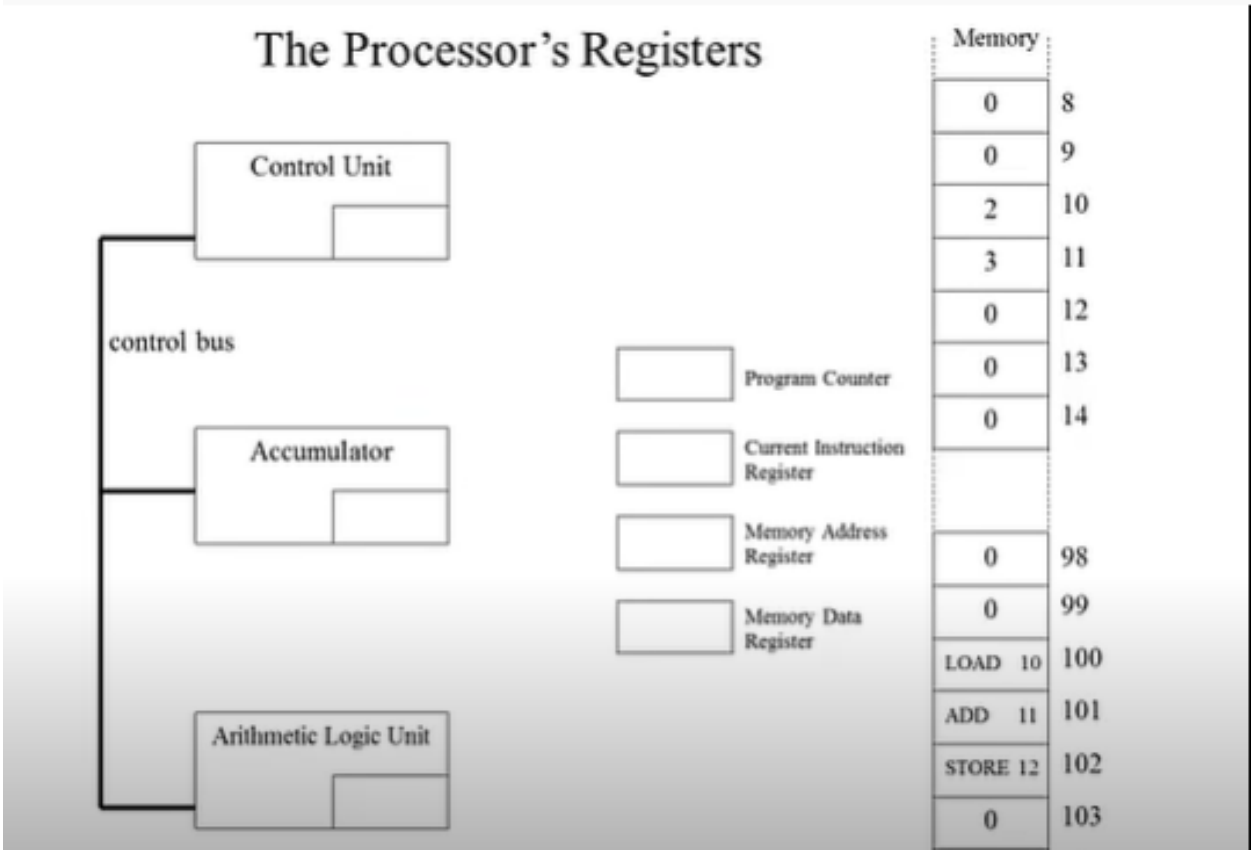
4 bytes *8 = 32 bits

b) State the effect that adding one new line to the address bus would have on the maximum addressable memory.

Adding one new line bus
32 +1 = 33

Adding bytes
2^33 *4
32 GB

13. Explain the Instruction cycle of the processor by taking an example of the
program
Load: [10]
Add : [11]
Store: [12]



As we can see there are assembly language source code which are given. As we can see in the processes register in the CPU. We have got Control unit, accumulator, and arithmetic logic unit.
Also, we have got other register they are program counter, current instruction registers, memory address register and memory data register. On the right side there is memory, and the program are stored.
Starting the program first the program counter stores the address of the next instruction to be fetched. Before the fetch the memory address must be placed into the Memory address memory then the contents of that memory address can then be loaded into the memory data register. Then we area fetching first number {load10}. Then the

instruction needs it placed inside the current instruction register. Then the program counter will increment by one, so the program counter is always pointing to the memory address of the next instruction to fetch. Now, we decode the instruction into the control unit which it play and its open various pathways then, now we are fetching the memory address register 10 and place it on the accumulator and it is the first instruction exerted. Now we are fetching the next instruction the program counter is already pointing of the next instruction and it is copied into the memory address register. Then the same process goes on like first instruction but this instruction add whatever in the accumulator, so this ALU is ready to play. The add instruction is passed to AKU to another place ready to work. Now, we got number of adding instruction for the fetch the memory address it has to place into the MDR. Then, the content of MDR goes to accumulator then the ALU add that to the first instruction and place back to accumulator. Now, the store instruction is done as second instruction like same it increment the PC it stop on that position. It says that store the result in the accumulator back into location 12.

14. Write short notes on the following topic:

a) Von Neumann and Harvard Architecture

- Von Neumann
  It is a type of digital computer architecture in which the design follows the concept of the computers with stored programs where they store the program data along with the instruction data in the very same memory. This architecture basically requires less space.

- Harvard
  It is a type of digital computer architecture in which the design follows a basic concept of having separate signal paths and separate storage for data and instructions. This type of architecture basically surfaced to overcome the overall bottleneck of the Von Neumann Architecture. This architecture basically requires more space.

b) RISC vs CISC architecture

The purpose of both RISC and CISC architectures is to increase CPU performance, but they try to achieve that goal in different ways. Generally speaking, RISC is seen by many as an improvement over CISC. The argument for RISC over CISC is that having a less complicated set of instructions makes designing a CPU easier, cheaper, and quicker.

The primary difference between RISC and CISC architecture is that RISC-based machines execute one instruction per clock cycle. In a CISC processor, each instruction performs so many actions that it takes several clock cycles to complete. In a RISC processor, every instruction also has a fixed memory size, which makes them easier to decode and execute. In a CISC machine, the instructions can be variable lengths, which increases the processing time.