1.

a. Define half adder.

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder can add two single binary digits and provide the output plus a carry value.

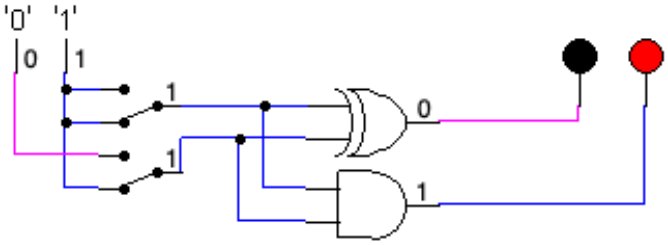
b. Draw a truth table for the sum and carry of half adder.

INPUT A	INPUT B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

c. Write the sop expression from the truth table.

Sum of product =A'B+AB'
Carry of product =A.B

d. Draw the circuit using logsim.



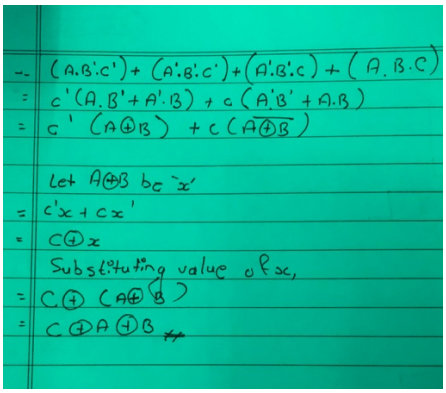
prepared by ABHISHEK

2. a. Draw the truth table for the outputs of the full adder.

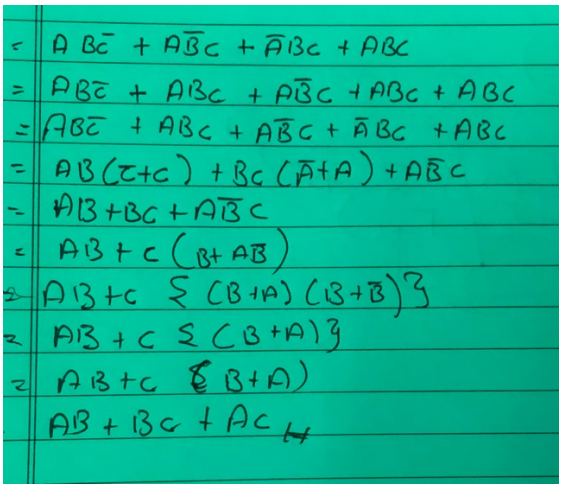
INPUT A	INPUT B	CARRY IN	SUM	CARRY OUT
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

b. Write the corresponding sop expression for sum and carry of full adder and simplify the expression

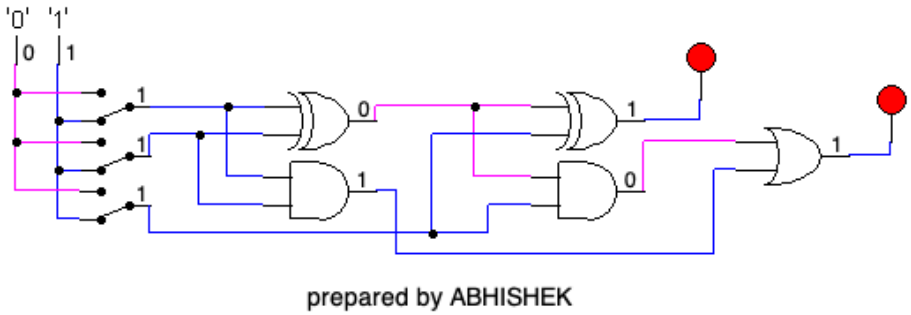
(A.B.C')+(A.B'.C)+(A'.B.C)+(A.B.C)



(A.B.C)+A.B’C)+(A’B.C)+(A.B.C)



c. Draw full adder using two half adder and an OR gate.



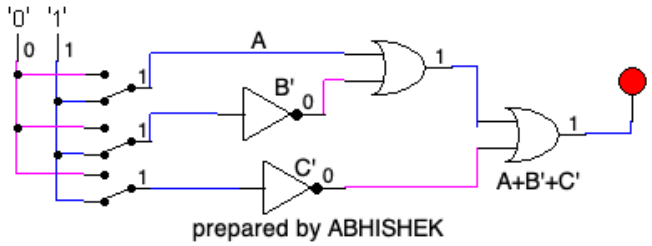
prepared by ABHISHEK

3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B and C are the inputs whereas D, E, F, G, H and I are outputs. Note: Draw circuit diagram using logsim corresponding to the simplified expression of outputs D, E, F, G, H and I.

A	B	C	D	E	F	G	H	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

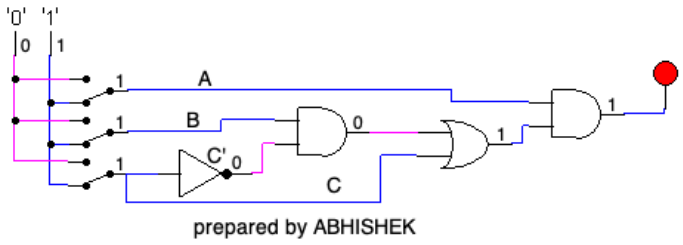
Output: D

A+B'+C'



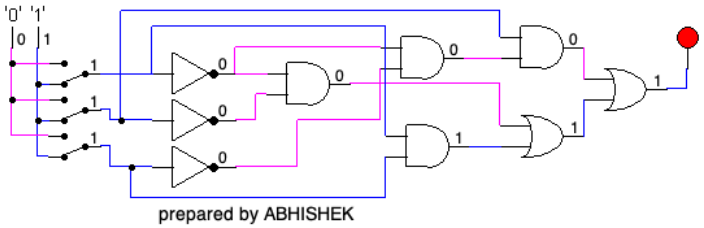
Output: E

A(C+B.C')



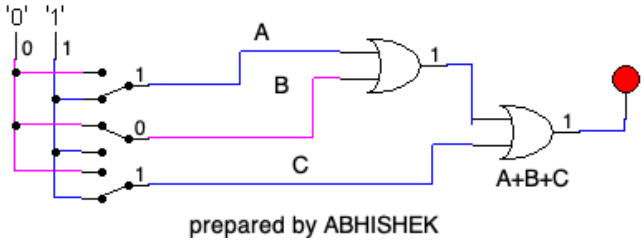
OUTPUT: F

A.C+A’.B’+A’.B.C’



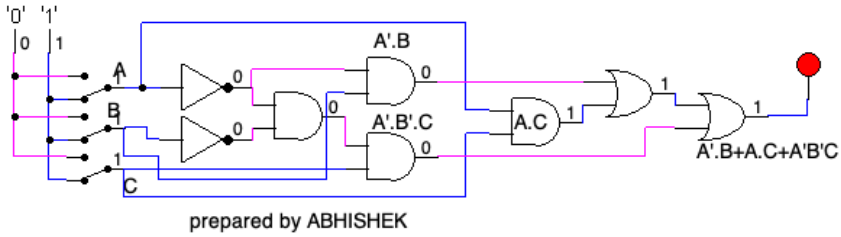
Output: G

A+B+C



Output: H

A’.B+A.C+A’.B’.C



Output: I

A’+B+C’