**4CS015 – Workshop #5 TO BE SUBMITTED**

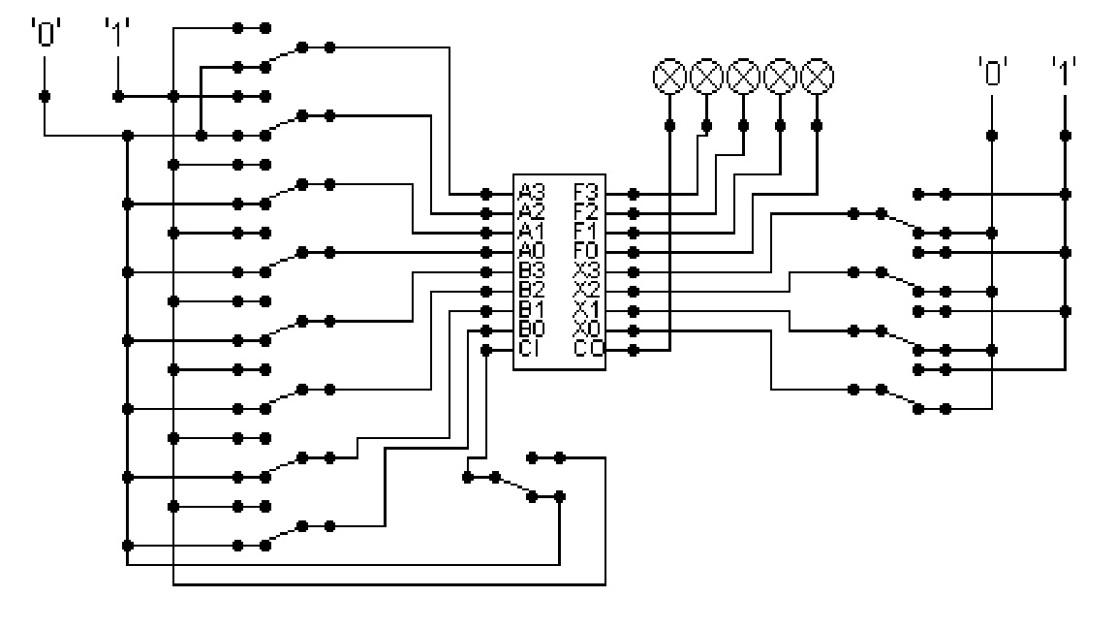
Name: Abhishek K.C.

Student ID: 2330790

This is a marked workshop. It forms the second part of your portfolio. You will need to complete the workshop and then submit a copy of this document with a title that follows the following format (“DENNETT 1234567 wsp5.docx”), via CANVAS, by the deadline.

**Workshop tasks:**

Arithmetic Logic Unit:

Load the LogSim Arithmetic Logic Unit Circuit **alu.cct** from inside the logsim application (You'll find it in the logsim folder) (***You may need to right-click on the link to download the file instead of opening it in the browser)***. It should look like this:  
  
  
  
The circuit behaves like a simple arithmetic logic unit. The inputs A0-A3 represent a 4 bit binary number. Inputs B0-B3 represent another binary number. A0 and B0 are the least significant bits respectively. The following table details the functions supported by the chip. All other control lines = 0.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Function | AND | OR | XOR | NAND | NOR | NOT A | ADD | SUBTRACT |
| X3 – X0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 1010 | 1011 |

|  |  |
| --- | --- |
| FUNCTION | OUTPUT |
| AND(0000) |  |
| OR(0001) |  |
| XOR(0010) |  |
| NAND (0011) |  |
| NOR(0100) |  |
| NOT A(0101) |  |
| ADD(1010) |  |
| SUBTRACT (1011) |  |

Use A= 11 B=4, complete the following table in binary ***(15 marks)***:

|  |  |  |
| --- | --- | --- |
| AND | OR | XOR |
| 1011  0100 AND operation  0000 | 1011  0100 OR operation  1111 | 1011  0100 XOR operation  1111 |

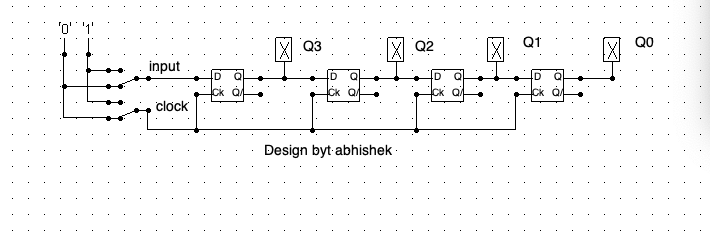
|  |  |  |
| --- | --- | --- |
| NAND | NOR | NOT A |
| 1011  0100 NAND operation  1111 | 1011  0100 NOR operation  0000 | 1011  0100 NOT A operation  0100 |

|  |  |
| --- | --- |
| ADD | SUBTRACT |
| 1011  0100 ADD operation  1111 | 1011  0100 SUBTRACT operation  0111 |

The logical operations are bitwise. Manually prove each operation has returned the correct result by  ***(15 marks)***:  
Example:  1 0 1 1  
                 1 0 1 0 AND OPERATION  
                 1 0 1 0 RESULT  
 Serial to Parallel Decoder ***(30 marks)***:  
Diagram, schematic

Description automatically generated

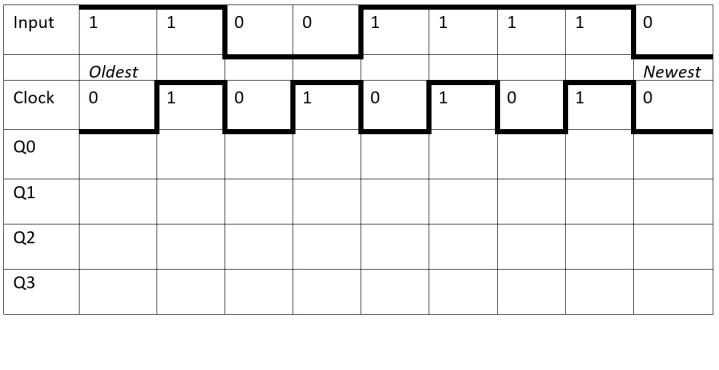
Build the circuit above and complete the following timing diagram by filling in the table spaces with ‘1’ or ‘0’. ***(15 marks)***



Describe what the circuit does. ***(15 marks)***

*Ans:*

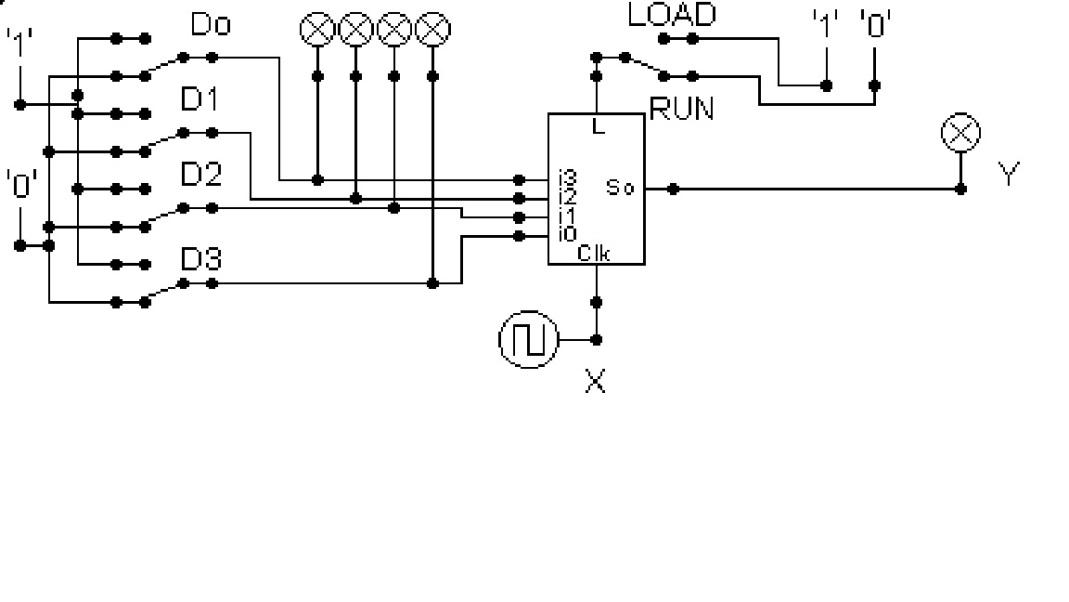
As we can see there are four inputs Q0, Q1, Q2 and Q3. The given circuit is serial to parallel decoder in which input is given once and output is given parallel. Input is for input which given by user and clock is given for clock unit. In figure we can see input is given in serial where output is given parallel. While given input in circuit than Q3 come out. Then another input is given in circuit than first output Q3 is pass to Q2 and new output is record in Q3. In same more input will give to circuit and pervious output will shift from Q3 to Q2, Q2 to Q1, Q1 to Q0. In this way output will come out parallel. In Timing table, we can output are shift from right to left when each clock. We can see output of timing table is shifting from right to left when clock is changing every time. In table we input1 is 1, input2 is 1 and input3 is 0 in Q3 but in Q2 input1 is Q1 is 1 Q2 is 0 and Q3 is 0. Such result is given because of output is shift from left to right. In this way serial in parallel circuit works.



Diagram

Description automatically generated

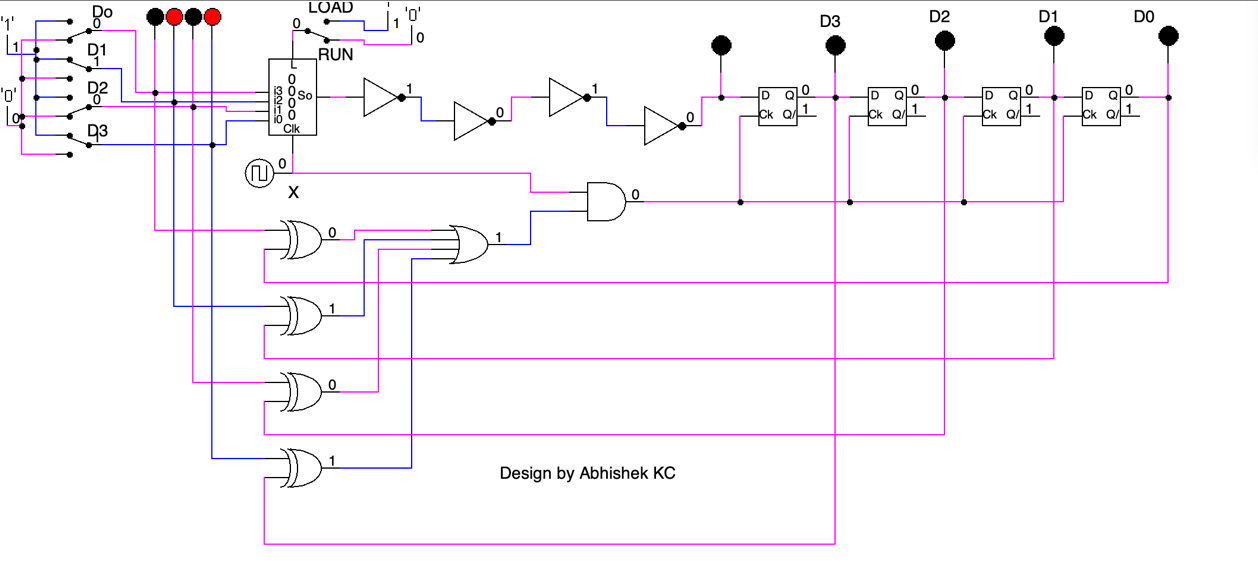
Parallel to Serial converter

Open the LogSim circuit **week5.cct** from the Logsim folder. It should look like this:  
  
  
  
Describe what this circuit does. ***(15 marks)***

*Ans:*  
similarly,   
In above given table there are four input which represent by D0, D1, D2, and D3. Similarly, y is given the output. In given circuit these two modes. There are load and shift mode. In load mode the mode input is load in circuit. Run mode is mode in which input is given to circuit, then output is also given but it is continuously changing because of clock. First, we load the four inputs in given circuit when load value is 1. Then we will change load mode into run mode than input is given to circuit, then circuit is gives output which is keep change with clock. Output is changing with the clock because the output is shift to Q3 TO Q0. We can see this shift when we change this clock with another clock. Parallel in serial output is a circuit which take input parallel and given the output serial. This computer to take input at once but tis circuit given the slow output. In this way above circuit words.

Design and add to the above circuit an additional circuit that takes the Clock X and the Output Y and decodes Y into 4 output indicators so that they match D0 – D3. Insert the LogSim GIF output of your design in the space below.

The highest marks will go to those who design the circuit such that it **AUTOMATICALLY** stops (not pauses) when the input to the circuit matches the output to the circuit



*ANS:*

In this diagram, we make a circuit that automatically stops, when the input, input by the suer matches with the output of the circuit. Similarly, in this circuit, we used 4 NOT gates, ‘XOR’ gates , following up by a ‘OR’ gate and a ‘AND’ gate. We have also used 4 D – Type flip-flop for the execution of the circuit.

In details, in this circuit, input ( 1001 ) is given. Similarly, the given input is transferred into D – Type circuit when the load is turned on. Moving on, the run, when the run is turned on, the circuit is run and paused according to the given input.