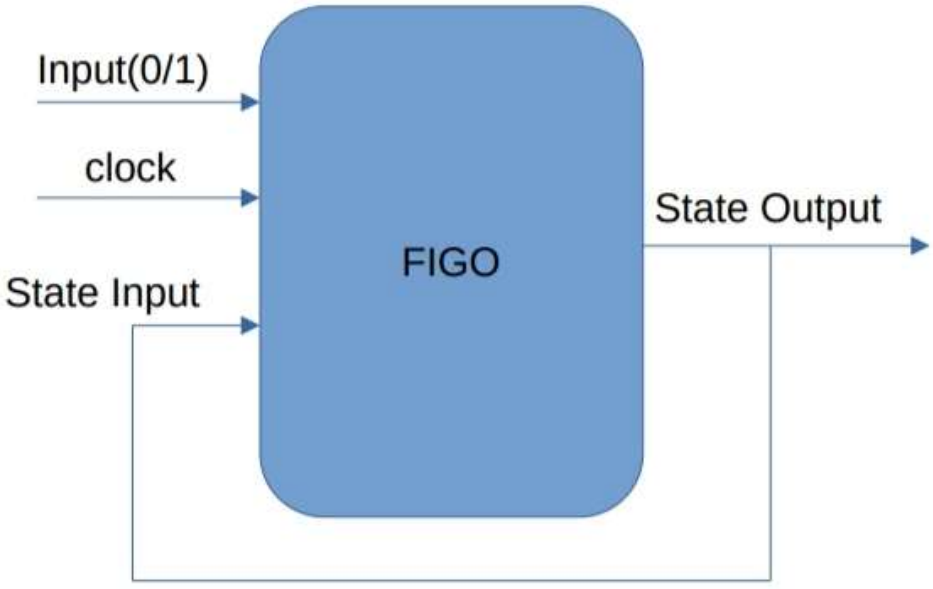
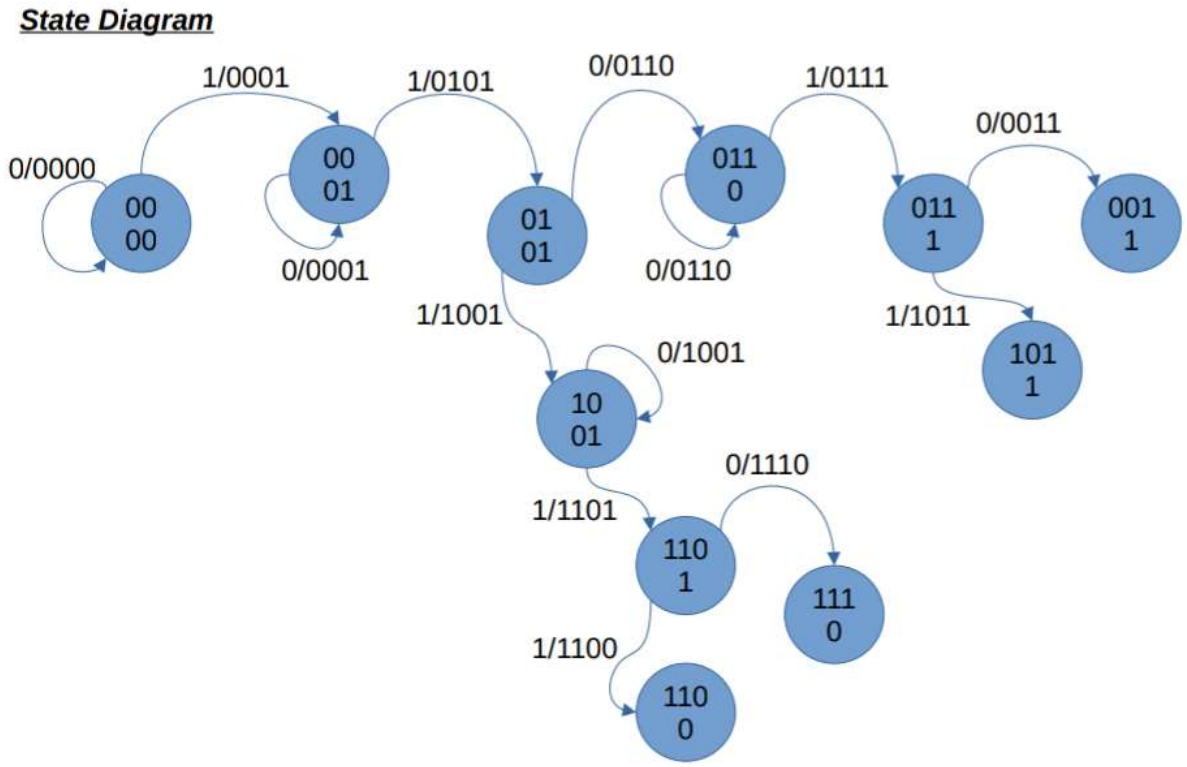
Intel Unnati Industrial Training

Design and Functional Simulation of Land Rover FIGO FSM

Team SGK

FIGO block diagram





Approach:

Firstly, the problem statement “Design and Functional Simulation of Land Rover FIGO FSM” along with its objectives and deliverables are analyzed for the requirements and the requirements are listed.

The requirements are:

- Verilog HDL
- Verilog mealy machine example
- Intel Quartus prime (lite) tool workflow and navigation.

The objective is to build a Verilog model which can indicate the current state of the room number assigned to it.

Our team initially started to search for the available resources either to learn Verilog or to have some starter code for the model and the testbench.

After having a look at many different Verilog examples, the most suitable one was the mealy machine. As we moved through the examples, we found out that our problem was like that of a sequence detector.

During the meetings with the industry mentors, we were informed of the available default templates available in the Intel Quartus Prime Lite software.

Our project's coding part started with the default template. We developed the testbench by taking motivation from available examples from the online tutorials and the example provided during tutorials.

This was the approach taken by us to start the project.

Complete workflow:

The first week of the training was spent in learning Verilog and different coding conventions for writing the code in Intel Quartus Prime Lite software.

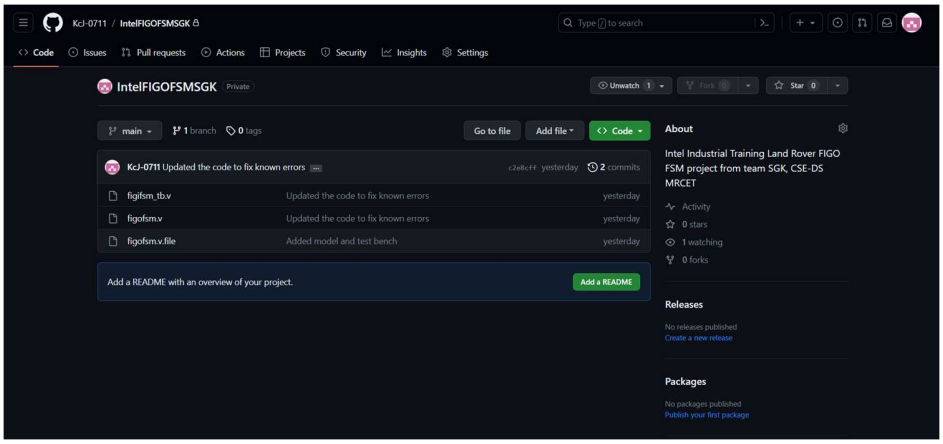
It was followed by choosing the type of machine (mealy/ Moore) and backed up by designing the state machine diagram and logic of the machine.

The second and third weeks of the training were occupied by developing the code and the testbench included fixing the errors and issues.

All the finishing and final implementation of the project and the deliverables are being fulfilled during the last week of the training.

This is the workflow for the whole training session.

Code upload to the repository



The main files (Verilog code for model and the testbench) have been uploaded to the GitHub repository.

Results:

The model works as expected and almost produces the output as in the state diagram.

Assumptions:

As the problem statement mentions that the FSM will be tested around the ISRO labs, so a small assumption has been made that there will be some obstructions in the area. The assumption is represented in the image below.

Room Assumption