Power Report:

Total thermal power estimate for the design is 420.14 mW.

Area Report:

Logic utilization (in ALMs): 18 / 32,070 (< 1 %)
Total registers: 11
Total pins: 7 / 457 (2 %)

Resource Usage Summary:

Logic utilization (ALMs needed / total ALMs on device): 18 / 32,070 (< 1 %)
ALMs needed [=A+B+C]: 18
    [A] ALMs used in final placement [=a+b+c+d]: 21 / 32,070 (< 1 %)
        [a] ALMs used for LUT logic and registers: 4
        [b] ALMs used for LUT logic: 15
        [c] ALMs used for registers: 2
        [d] ALMs used for memory (up to half of total ALMs): 0
    [B] Estimate of ALMs recoverable by dense packing: 3 / 32,070 (< 1 %)
    [C] Estimate of ALMs unavailable: 0 / 32,070 (0 %)
    Difficulty packing design: Low
Total LABs: partially or completely used: 3 / 3,207 (< 1 %)
    --Logic LABs: 3
    --Memory LABs (up to half of total LABs): 0
Combinational ALUT usage for logic: 34
    -- 7 input functions: 0
    -- 6 input functions: 2
    -- 5 input functions: 3
    -- 4 input functions: 1
    -- < = 3 input functions: 28
Combinational ALUT usage for route-throughs: 0
Dedicated logic registers: 11
    --by type:
        -- Primary logic registers: 11 / 64,140 (< 1 %)
        -- Secondary logic registers: 0 / 64,140 (0 %)
    -- by function:
        -- Design implementation registers: 11
        -- Routing optimization registers: 0
    Virtual pins: 0
I/O pins: 7 / 457 (2 %)
    -- Clock pins: 1 / 8 (13 %)
    -- Dedicated input pins: 0 / 21 (0 %)
Hard processor system peripheral utilization
    -- Boot from FPGA: 0 / 1 (0 %)
    -- Clock resets: 0 / 1 (0 %)
    -- Cross trigger: 0 / 1 (0 %)
    -- S2F AXI: 0 / 1 (0 %)
    -- F2S AXI: 0 / 1 (0 %)

-- AXI Lightweight: 0 / 1 (0 %)
-- SDRAM: 0 / 1 (0 %)
-- Interrupts: 0 / 1 (0 %)
-- JTAG: 0 / 1 (0 %)
-- Loan I/O: 0 / 1 (0 %)
-- MPU event standby: 0 / 1 (0 %)
-- STM event: 0 / 1 (0 %)
-- TPIU trace: 0 / 1 (0 %)
-- DMA: 0 / 1 (0 %)
-- CAN: 0 / 2 (0 %)
-- EMAC: 0 / 2 (0 %)
-- I2C: 0 / 4 (0 %)
-- NAND Flash: 0 / 1 (0 %)
-- QSPI: 0 / 1 (0 %)
-- SDMMC: 0 / 1 (0 %)
-- SPI Master: 0 / 2 (0 %)
-- SPI Slave: 0 / 2 (0 %)
-- UART: 0 / 2 (0 %)
-- USB: 0 / 2 (0 %)
M10K blocks: 0 / 397 (0 %)
Total MLAB memory bits: 0
Total block memory bits: 0 / 4,065,280 (0 %)
Total block memory implementation bits: 0 / 4,065,280 (0 %)
Total DSP Blocks: 0 / 87 (0 %)
Fractional PLLs: 0 / 6 (0 %)
Global signals: 1
-- Global clocks: 1 / 16 (6 %)
--Quadrant clocks: 0 / 66 (0 %)
-- Horizontal periphery clocks: 0 / 18 (0 %)
SERDES transmitters: 0 / 100 (0 %)
SERDES receivers: 0 / 100 (0 %)
JTAGs: 0 / 1 (0 %)
ASMI blocks: 0 / 1 (0 %)
CRC blocks: 0 / 1 (0 %)
Remote update blocks: 0 / 1 (0 %)
Oscillator blocks: 0 / 1 (0 %)
Impedance control blocks: 0 / 4 (0 %)
Hard Memory Controllers: 0 / 2 (0 %)
Average interconnect usage (total/H/V): 0.0% / 0.0% / 0.0%
Peak interconnect usage (total/H/V): 0.3% / 0.4% / 0.2%
Maximum fan-out: 15
Highest non-global fan-out: 15
Total fan-out: 147
Average fan-out: 2.45