PRE-LAB WORK

Post-Lab report is on page 8

3.2.1 to 3.2.2

74HCT00

QUADRUPLE 2-INPUT NAND GATES

Description

The 74HCT00 provides provides four independent 2-input NAND gates with standard push-pull outputs. The device is designed for operation with a power supply range of 4.5V to 5.5V.

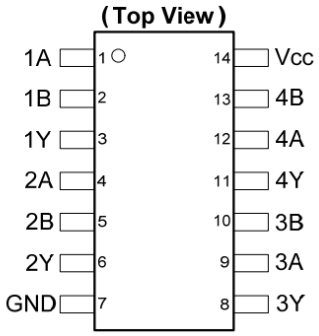
The gates perform the Boolean function:

$$Y = \overline{A \bullet B} \text{ or } Y = \overline{A} + \overline{B}$$

Features

- Wide Supply Voltage Range from 4.5V to 5.5V
- Pin Compatible with Low Power Schottky (LSTTL)
- Inputs Are TTL Voltage Level Compatible
- Sinks or sources 4mA at Vcc = 4.5V
- CMOS low power consumption
- Schmitt Trigger Action at All Inputs
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115-A)
  - 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments



SO-14 / TSSOP-14

Applications

- General Purpose Logic
- Wide array of products such as:
  - PCs, networking, notebooks, netbooks
  - Computer peripherals, hard drives, CD/DVD ROM
  - TV, DVD, DVR, set top box

Function Table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

4. Functional diagram

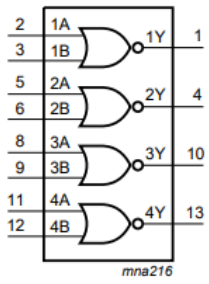


Fig. 1. Logic symbol

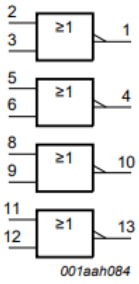


Fig. 2. IEC logic symbol

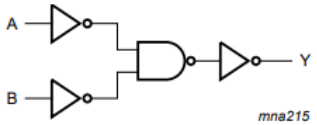
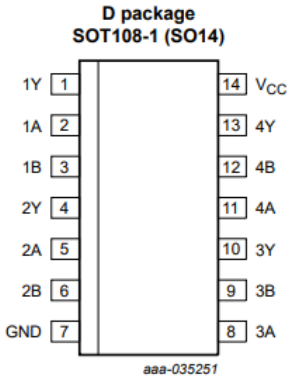


Fig. 3. Logic diagram (one gate)

5. Pinning information

5.1. Pinning



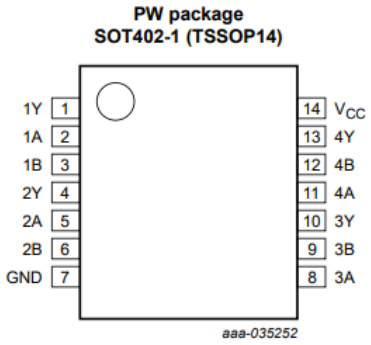


Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	data output
1A, 2A, 3A, 4A	2, 5, 8, 11	data input
1B, 2B, 3B, 4B	3, 6, 9,12	data input
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	**nB**	**nY**
L	L	H
X	H	L
H	X	L

DIODES INCORPORATED

74HC04

HEX INVERTERS

Description

The 74HC04 provides provides six independent inverters with standard push-pull outputs. The device is designed for operation with a power supply range of 2.0V to 6.0V.

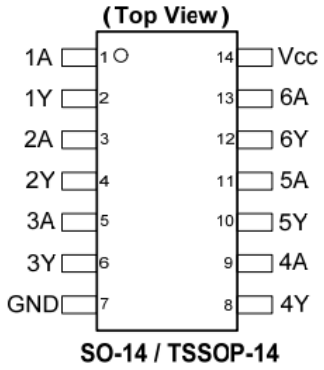
The gates perform the Boolean function:

$Y = \overline{A}$

Features

- Wide Supply Voltage Range from 2.0V to 6.0V
- Sinks or sources 4mA at Vcc = 4.5V
- CMOS low power consumption
- Schmitt Trigger Action at All Inputs
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115-A)
  - 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments



SO-14 / TSSOP-14

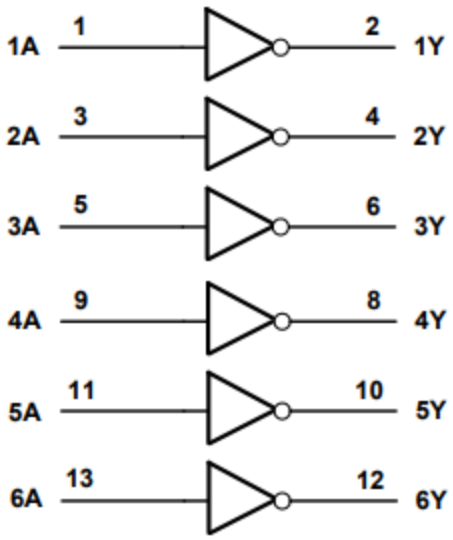
Applications

- General Purpose Logic
- Wide array of products such as:
  - PCs, networking, notebooks, netbooks
  - Computer peripherals, hard drives, CD/DVD ROM
  - TV, DVD, DVR, set top box

Pin Descriptions

Pin Number	Pin Name	Function
1	1A	Data Input
2	1Y	Data Output
3	2A	Data Input
4	2Y	Data Output
5	3A	Data Input
6	3Y	Data Output
7	GND	Ground
8	4Y	Data Output
9	4A	Data Input
10	5Y	Data Output
11	5A	Data Input
12	6Y	Data Output
13	6A	Data Input
14	V_{CC}	Supply Voltage

Logic Diagram

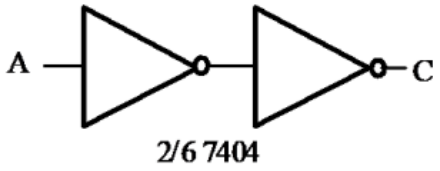


Function Table

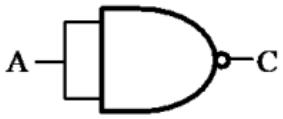
Input	Output
A	**Y**
H	L
L	H

3.2.3

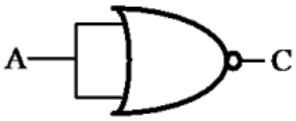
3.2.3 Establish truth tables relating the inputs A and B to the output C for the circuits below. Summarise the truth tables with algebraic expressions which reflect the relevant theorems of Boolean algebra.



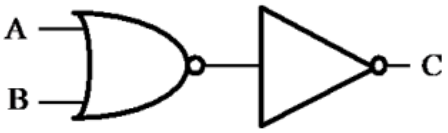
2/6 7404

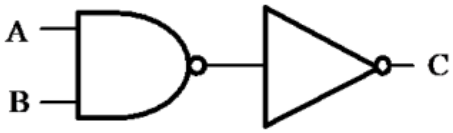


1/4 7400



1/4 7402





* = inversion

A** = C

A	C
1	1
0	0
1	1

(AA)* = C

A	C
1	0
0	1
1	0

(A + A)* = C

A	C
1	0
0	1
1	0

(A + B)** = C

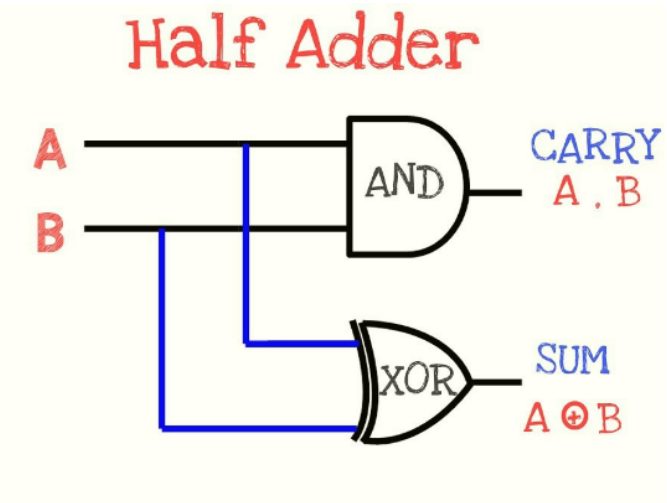
A	B	C
1	1	1
0	1	1
1	0	1

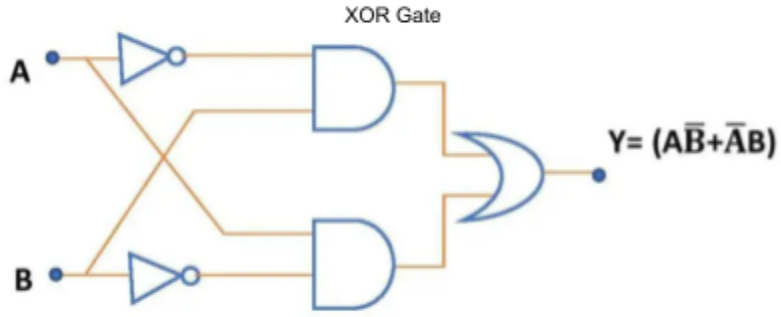
(AB)** = C

A	B	C
1	1	1
0	1	0
1	0	0

3.2.4 A One-Bit Half Adder

Write down the truth table for a one-bit adder with inputs A, B, and outputs CARRY & SUM. Write expressions for the two outputs, and sketch the logic circuit that you will construct to implement this function.





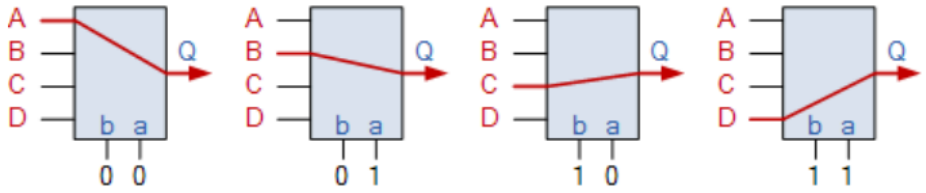
A	B	SUM	CARRY
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	0

3.2.5 The 74HCT153 MUX

Get the data sheet of the above dual 4:1 MUX and study the operation of this device. Pay particular attention to the use of the ENABLE inputs. Explain what function this has in the operation of the IC. Now sketch in your lab book the logic levels that needs to be connected to the input lines in order to make this 4:1 MUX function as (i) a NAND gate and (ii) an XOR gate.

The multiplexer, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

The Function of a 4:1 Multiplexer with A,B,C,D as input lines and a,b as select inputs. Output Q is selected among A,B,C,D based on select inputs a,b.

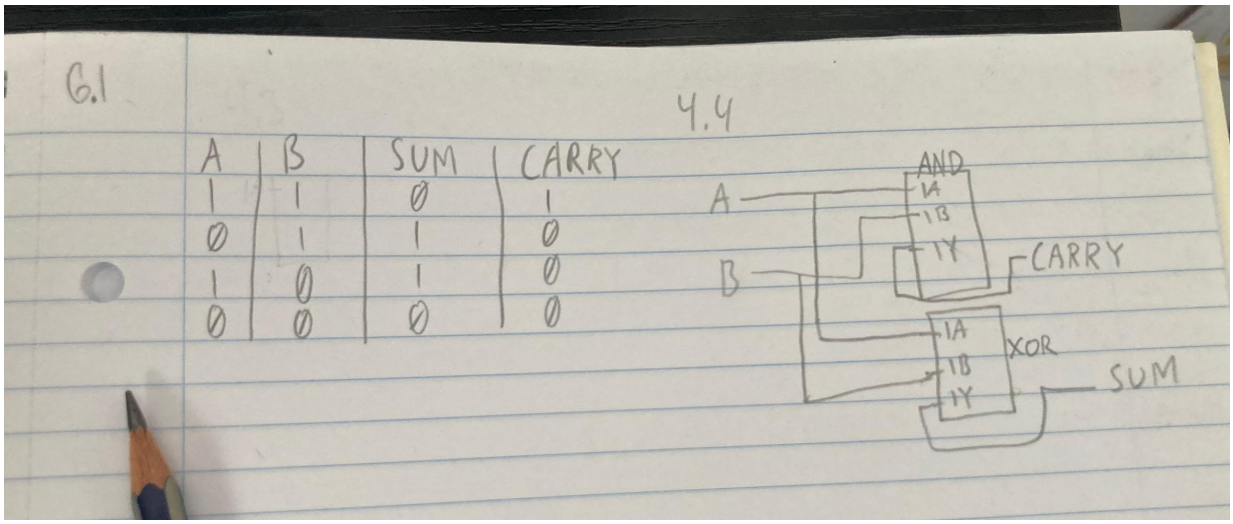


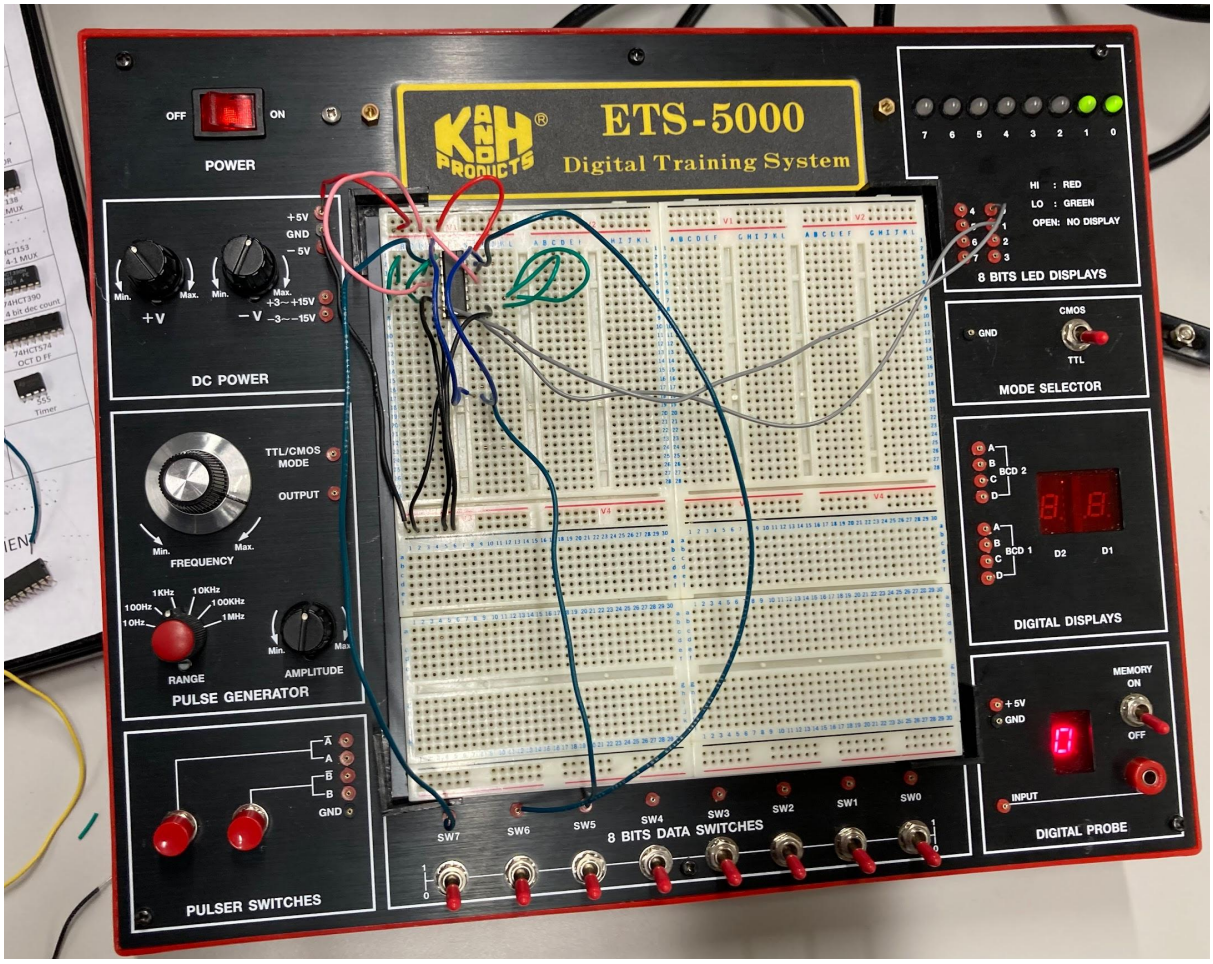
b	a	Q
0	0	A
0	1	B
1	0	C
1	1	D

i) A
ii) B+C

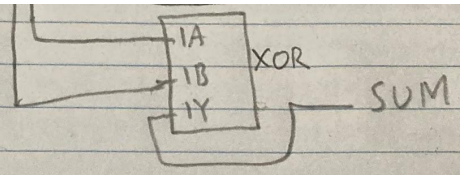
POST-LAB REPORT

6.1





6.2



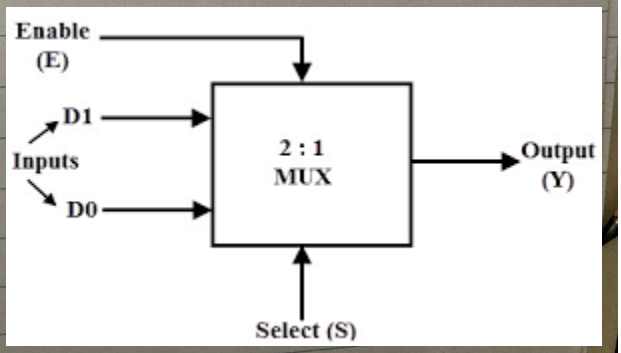
x = don't care

6.2

A	B	C	D	S_1	S_0	Output
1	x	x	x	0	0	1
x	1	x	x	0	1	1
x	x	1	x	1	0	1
x	x	x	1	1	1	1

The multiplexer is used to switch between multiple states, in this case: 4, by using the specific combination of 0/1, OFF/ON, or Low volt / High volt states of two inputs. This allows for implementing multiple gates on the MUX for making more complex functions such as the half bit adder

ENABLE INPUTS manage the multiplexing by being active low, letting the two inputs be active when the ENABLE is low and deadivating the inputs when high.



6.3

...LEDs when High.

6.3

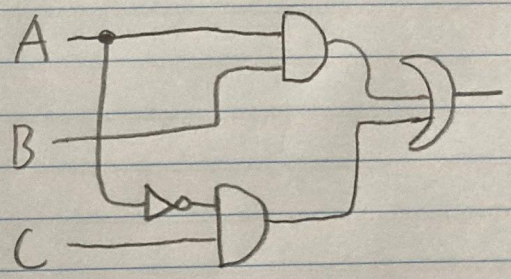
A	B	C	#	Prime?
0	0	0	0	0
0	1	0	1	0
0	0	1	2	1
0	1	1	3	1
1	0	0	4	0
1	1	0	5	1
1	0	1	6	0
1	1	1	7	1

$\bar{A}\bar{B}C + \bar{A}BC + AB\bar{C} + ABC$

$\bar{A}C(\bar{B}+B) + AB\bar{C} + ABC$

$\bar{A}C + AB(\bar{C}+C)$

$\bar{A}C + AB$



4 ICs

The MUX can simulate two ICs as shown in the half-adder activity so we already know that it would take 2 Muxes, which counts as 2 ICs, to perform this function.