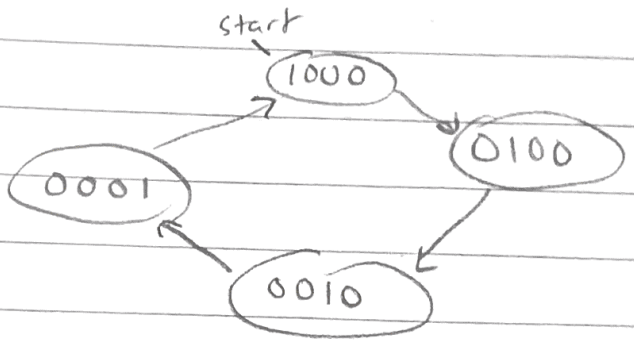
Homework 7

1a.

	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1
9	1	0	0	0
10	0	1	0	0
11	0	0	1	0
12	0	0	0	1
13	1	0	0	0
14	0	1	0	0
15	0	0	1	0
16	0	0	0	1



1b. There are 4 different 4-bit values for Q_0 Q_1 Q_2 Q_3.

1c. Only one flip-flop can have an output value of 1 at the same time.

1d. Two flip-flops change value on a single active clock edge. One changes from 1 to 0 and the other changes from 0 to 1.

1e.

	Q_0	Q_1	Q_2	Q_3
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1
4	1	0	0	1
5	1	1	0	0
6	0	1	1	0
7	0	0	1	1
8	1	0	0	1
9	1	1	0	0
10	0	1	1	0
11	0	0	1	1
12	1	0	0	1
13	1	1	0	0
14	0	1	1	0
15	0	0	1	1
16	1	0	0	1

1f.

	Q_0	Q_1	Q_2	Q_3
1	1	0	1	0
2	0	1	0	1
3	1	0	1	0
4	0	1	0	1
5	1	0	1	0
6	0	1	0	1
7	1	0	1	0
8	0	1	0	1
9	1	0	1	0
10	0	1	0	1
11	1	0	1	0
12	0	1	0	1
13	1	0	1	0
14	0	1	0	1
15	1	0	1	0
16	0	1	0	1

2a.

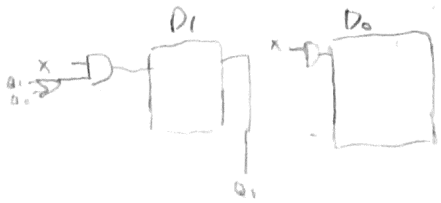
	Q_0	Q_1	Q_2	Q_3
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1
9	0	0	0	0
10	1	0	0	0
11	1	1	0	0
12	1	1	1	0
13	1	1	1	1
14	0	1	1	1
15	0	0	1	1
16	0	0	0	1

2b. For a twisted ring counter, there are 2N states for N flipflops, therefore there are 8 different 4-bit values for $Q_0 Q_1 Q_2 Q_3$

2c. Only one flip flop changes value on a single active clock edge

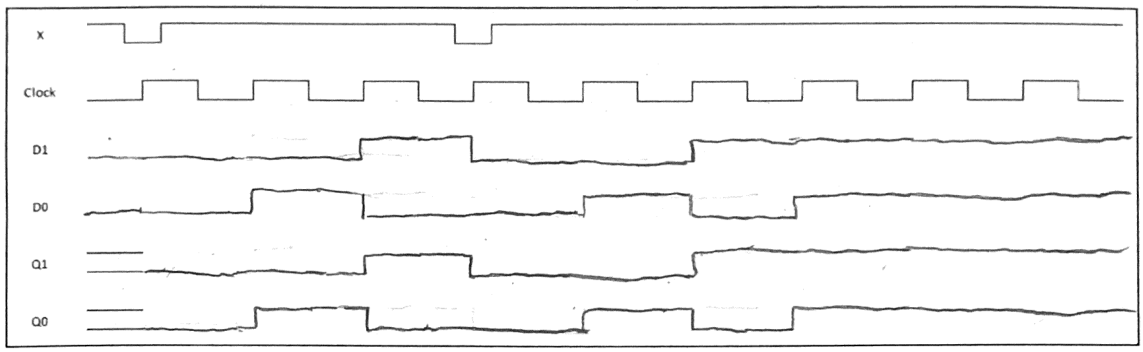
2d.

	Q_0	Q_1	Q_2	Q_3
1	0	1	0	0
2	1	0	1	0
3	1	1	0	1
4	0	1	1	0
5	1	0	1	1
6	0	1	0	1
7	0	0	1	0
8	1	0	0	1
9	0	1	0	0
10	1	0	1	0
11	1	1	0	1
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	0	0	1	0
16	1	0	0	1



3. A circuit has two positive edge-triggered D-type flip-flops which have a common clock signal. The two D inputs are $D_0 = X \cdot (Q_1 + Q_0')$ and $D_1 = X \cdot (Q_1 + Q_0)$ where X is an external input signal. Based on the operation of D-type flip-flops, complete the timing diagram below for the D's and Qs by stepping one clock cycle at a time to first evaluate the Ds before each active clock edge, and then set the value of the Qs after the clock edge until the following active cock edge. Assume that set-up and hold time requirements have been met. Do not explicitly show propagation delays through the flip-flops.

D1	D0	Q1	Q0
0	0	0	0
0	1	0	1
1	0	1	0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1
1	1	1	1



* Assuming D1 is the first Flip Flop

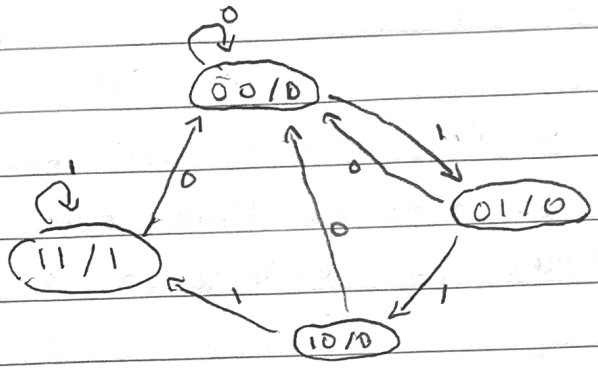
4. For the circuit in the previous problem, add a circuit output Z which is $Z = Q_1 \cdot Q_0$. Analyze this circuit operation for all inputs with a next state table and a state transition diagram instead of doing a simple timing diagram for one specific input sequence.
   a. Show the next state table for this circuit in the style of Figure 6.6 with present state Q1 Q0 in place of y2 y1 and input X instead of w. For the next state, evaluate D2 D1, which will be the next state since it will be the value of the flip-flop outputs after the active clock edge.
   b. Draw the state transition diagram in the style of Figure 6.3. Use the actual state values of Q_1, Q_0 rather than A, B, C, and D.
   c. What does this circuit do? When is the output 1?
   d. Create the timing diagram from the previous problem directly from the state table for the specific input sequence given and make sure that they are the same.

5. A 4-bit shift register with outputs Q_0, Q_1, Q_2, Q_3 has serial input $D_0 = Q_0 \oplus Q_3$. Note that there is no external input to this shift register. However, the shift register will have a synchronous load capability so that its starting state can be specified.
   a. Show the next state table for this shift register in the style of Figure 6.6. Use Q_0, Q_1, Q_2, Q_3 to define the states.
   b. Draw the state transition diagram for the case where the shift register is initialized to 0000.
   c. Draw the state transition diagram for the case where the shift register is initialized to 1000.

4a.

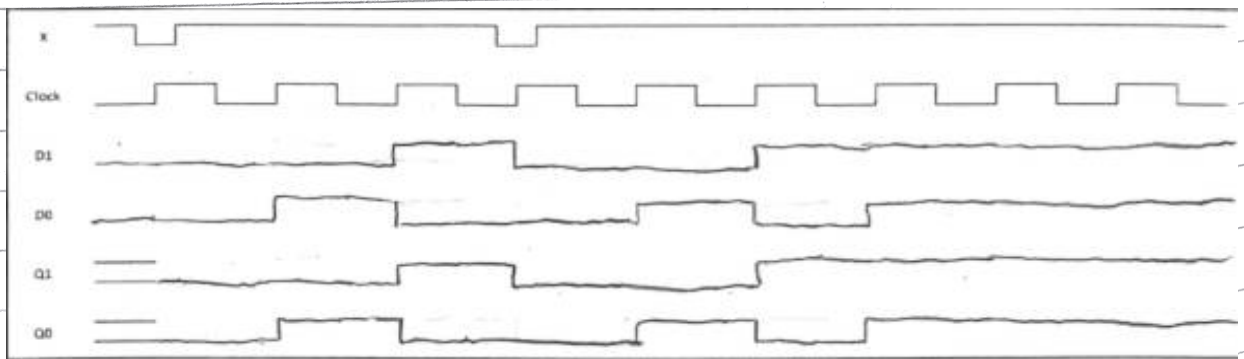
Present State / Input		Next State				Output
		x=0		x=1		
Q_1	Q_0	D_1	D_0	D_1	D_0	z
0	0	0	0	0	1	0
0	1	0	0	1	0	0
1	0	0	0	1	1	0
1	1	0	0	1	1	1

4b. $Q_1 Q_0 / z$



4c. This circuit starts from $Q_1 Q_0 = 00$. When the input $x=1$, the circuit moves to the next state. At any state if the input $x=0$, then the circuit moves to the first/starting state $Q_1 Q_0 = 00$. When the output is 1, the circuit's present state is the fourth state and moves to the fourth state if the input $x=1$ on the next positive clock edge.

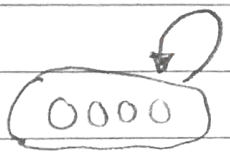
4d.



5a.

Present State / Input	Next State
	$D_0 = Q_0 \oplus Q_3$
$Q_0\ Q_1\ Q_2\ Q_3$	$Q_0\ Q_1\ Q_2\ Q_3$
0 0 0 0	0 0 0 0
0 0 0 1	1 0 0 0
0 0 1 0	0 0 0 1
0 0 1 1	1 0 0 1
0 1 0 0	0 0 1 0
0 1 0 1	1 0 1 0
0 1 1 0	0 0 1 1
0 1 1 1	1 0 1 1
1 0 0 0	1 1 0 0
1 0 0 1	0 1 0 0
1 0 1 0	1 1 0 1
1 0 1 1	0 1 0 1
1 1 0 0	1 1 1 0
1 1 0 1	0 1 1 0
1 1 1 0	1 1 1 1
1 1 1 1	0 1 1 1

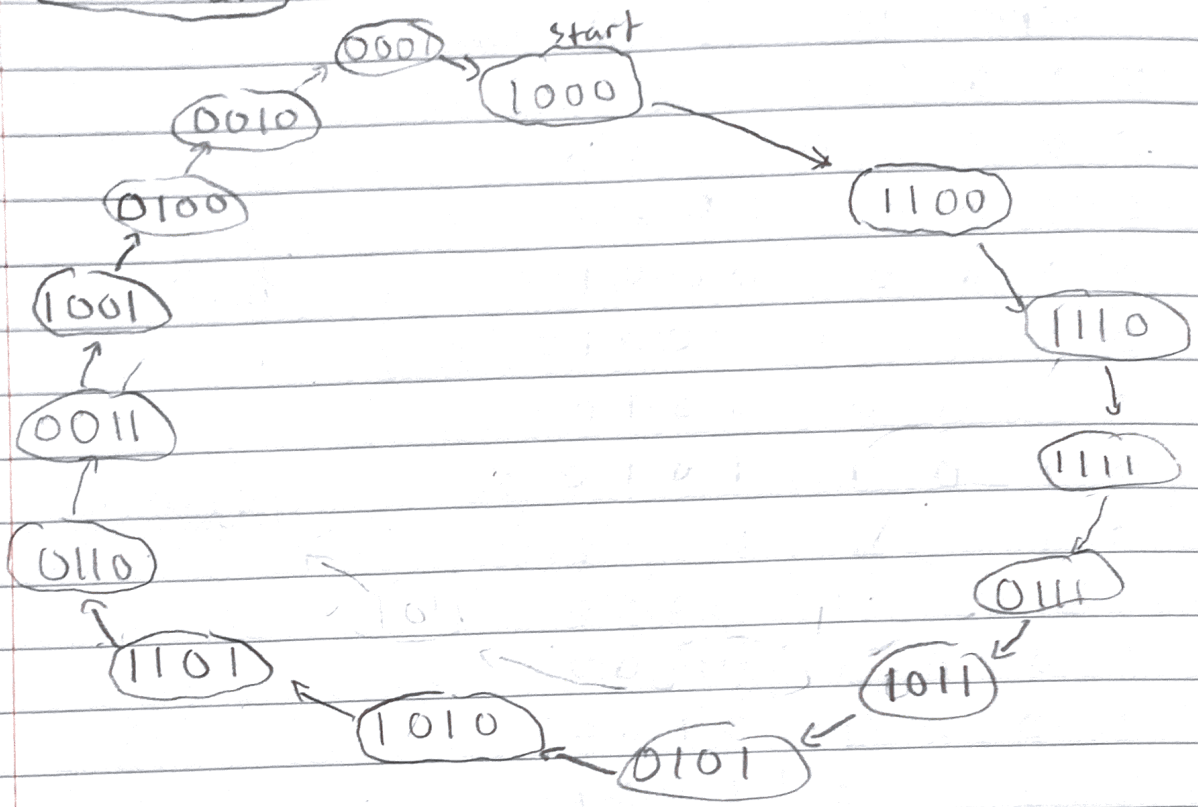
5b. $Q_0Q_1Q_2Q_3$



since $D_0 = Q_0 \oplus Q_3$

∴ Next state equal 0000 and repeats over again

5a. $Q_0Q_1Q_2Q_3$


start
1000
1100
1110
1111
0111
1011
0101
1010
1101
0110
0011
1001
0100
0010
0001