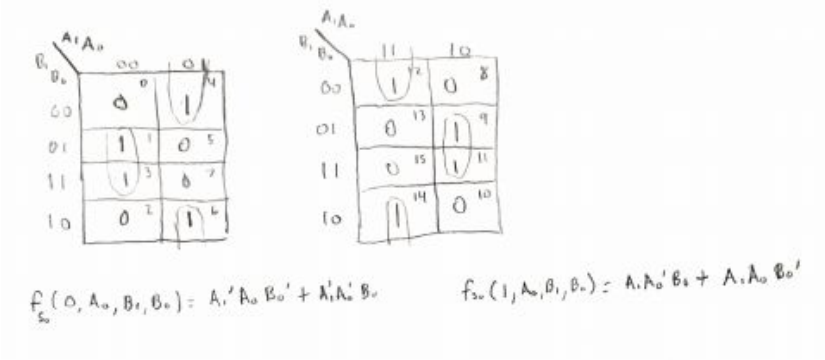
Kendall Won
Matt Seminatore

COEN 21 Lab 4

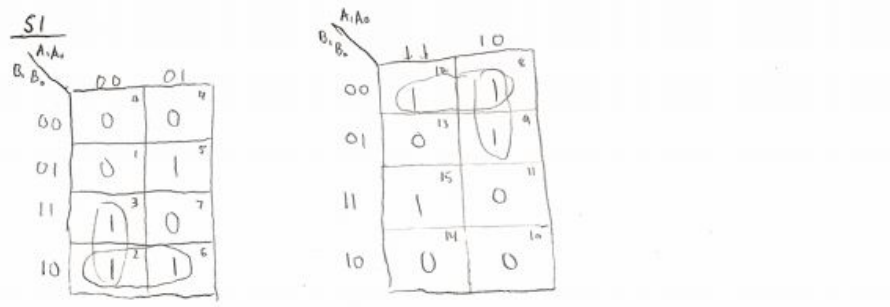
In this lab, we are creating an adder for two-bit integers. It takes in the three inputs and a fourth selector input using multiplexers to select which functions to use. We made two function blocks for each output, and a multiplexer chose between them using the input A1. We used Shannon's expansion to design the functions. As a result, we created a circuit that added two numbers between 0-3 and added them to get a number from 0-6.

S0F0=A0'B0+A0B0'
S0F1=A0'B0+A0B0'
S1F0 = A0'B1+B1B0'+A0B1'B0
S1F1 = A0'B1'+B1'B0'+A0B1B0
S2F0=A0B1B0
S2F1=B1+A0B0

S0



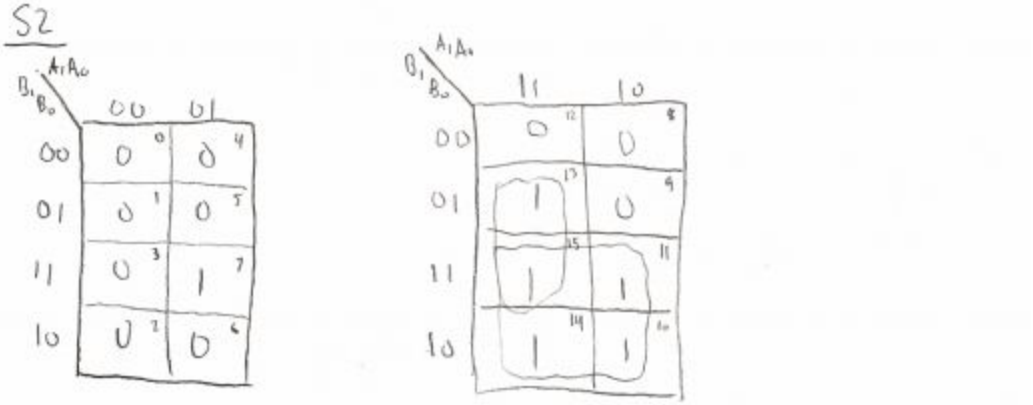
S1



$f_{s_1}(0, A_0, B_1, B_0) = A_1'A_0'B_1 + A_1'B_1B_0' + A_1'A_0B_1'B_0$

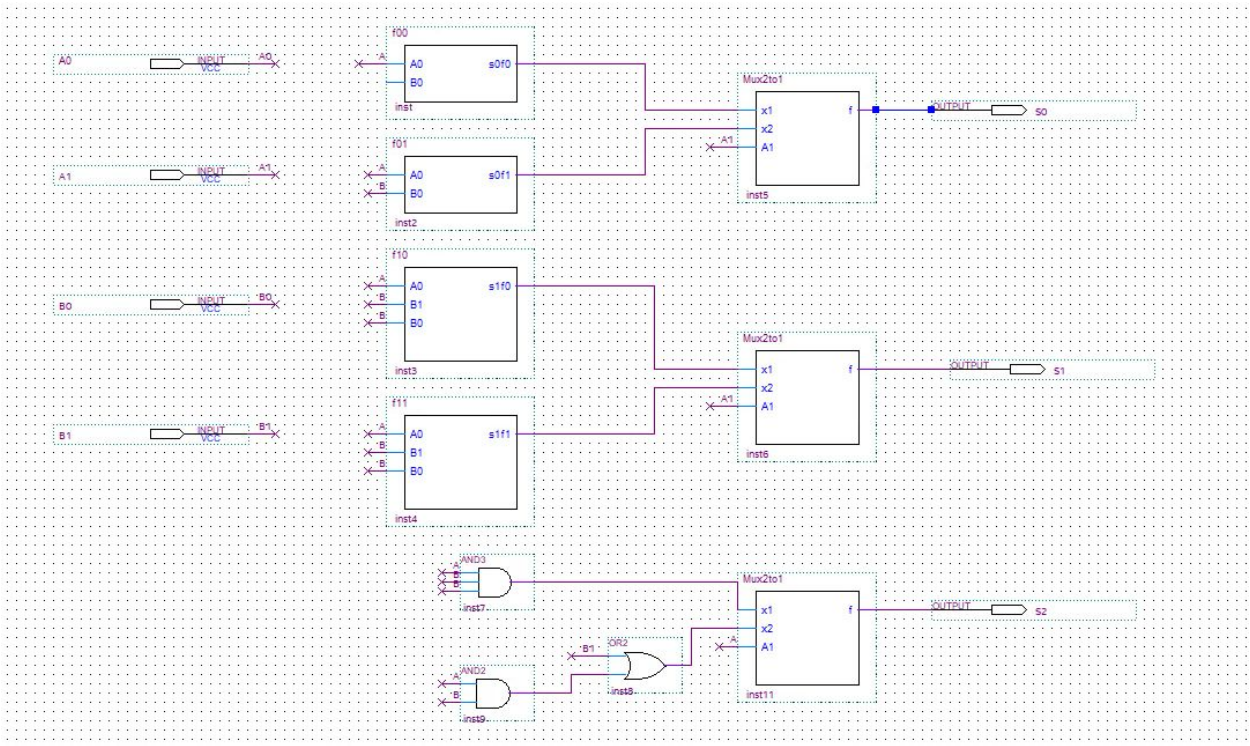
$f_{s_1}(1, A_0, B_1, B_0) = A_1A_0'B_1' + A_1B_1'B_0' + A_1A_0B_1B_0$

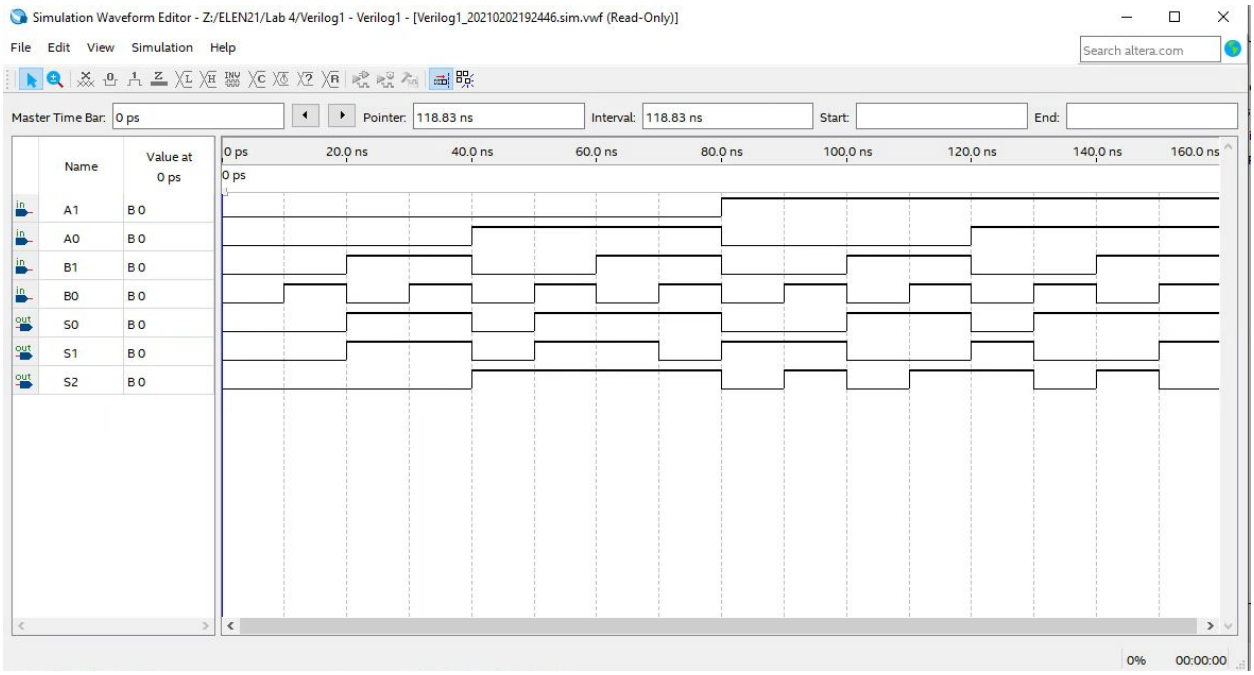
S2



$f_{s_2}(0, A_0, B_1, B_0) = A_1'A_0B_1B_0$

$f_{s_2}(1, A_0, B_1, B_0) = A_1B_1 + A_1A_0B_0$


A0
INPUT
VCC
A1
B0
B1
f00
f01
f10
f11
A0
B0
B1
s0f0
s0f1
s1f0
s1f1
inst1
inst2
inst3
inst4
Mux2to1
x1
x2
A1
f
inst5
inst6
inst11
OUTPUT
S0
S1
S2
AND3
AND2
OR2
inst7
inst9
inst10


Simulation Waveform Editor - Z:/ELEN21/Lab 4/Verilog1 - Verilog1 - [Verilog1_20210202192446.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 118.83 ns
Interval: 118.83 ns
Start:
End:
Name
Value at 0 ps
A1 B 0
A0 B 0
B1 B 0
B0 B 0
S0 B 0
S1 B 0
S2 B 0
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
0%
00:00:00

```
module Mux2to1 (x1,x2,A1,f);
	input x1,x2,A1;
	output f;

	assign f= (~A1&x1)|(A1&x2);

endmodule



module f00 (A0,B0,s0f0);
	input A0,B0;
	output s0f0;

	assign s0f0=A0^B0;

endmodule



module f01 (A0,B0,s0f1);
	input A0,B0;
	output s0f1;

	assign s0f1=A0^B0;

endmodule



module f10(A0,B1,B0,s1f0);
	input A0,B1,B0;
	output s1f0;

	assign s1f0=(~A0 & B1)|(B1 & ~B0)|(A0 & ~B1 & B0);

endmodule
```

```
module f11(A0,B1,B0,s1f1);
	input A0,B1,B0;
	output s1f1;

	assign s1f1=(~A0 & ~B1)|(~B1 & ~B0)|(A0 & B1 & B0);

endmodule
```

Conclusion

In this lab, we learned how to implement Verilog designs and the usefulness of Verilog in organizing logical circuit schematics at higher levels of complexity. We didn't face any challenges with our Verilog or schematics. The only challenges we faced were small errors that required the TA's assistance to fix. For example, having to change the name of Waveform.vwf to Waveform4.vwf in the simulation settings.