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COEN 21 Lab5

- Find one pair of X and Y inputs (with C0=0) that would result in the following:
    - C4 = 0 and V = 0: X = 1 and Y = 0
    - C4 = 0 and V = 1: X = 4 and Y = 4
    - C4 = 1 and V = 0: X = 9 and Y = 7
    - C4 = 1 and V = 1: X = C and Y = A

- If you had to make an 8-bit adder, show how would you do it using only instances of the 4-bit module you have built in this lab? Specifically, show how you would create the C8 output and the V output.
    - To make an 8-bit adder, we would use two 4-bit modules. C4 would connect to the CIN of the second 4-bit module, and that second 4-bit module's COUT would be C8. X[3:0] and Y[3:0] would go into the first 4-bit module and X[7:4] and Y[7:4] would go into the second 4-bit module. V would equal technically be C[7] ^ C8 but will be assigned in the second 4-bit adder.

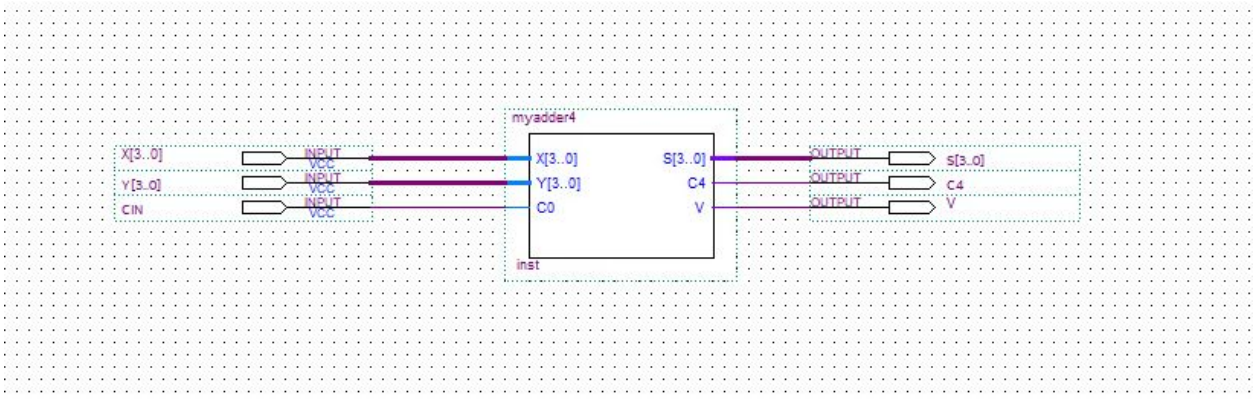
- Did the initial testing of your circuit go smoothly or did you encounter incorrect results? If the latter, describe how you determined what was wrong.
    - In our initial testing, we did have incorrect results. Our problem was that we messed up the variable (input/output) order in the Verilog code, switching the S and the CIN. We determined it was wrong by looking over our code again and noticing from the results that the COUT S was wrong.

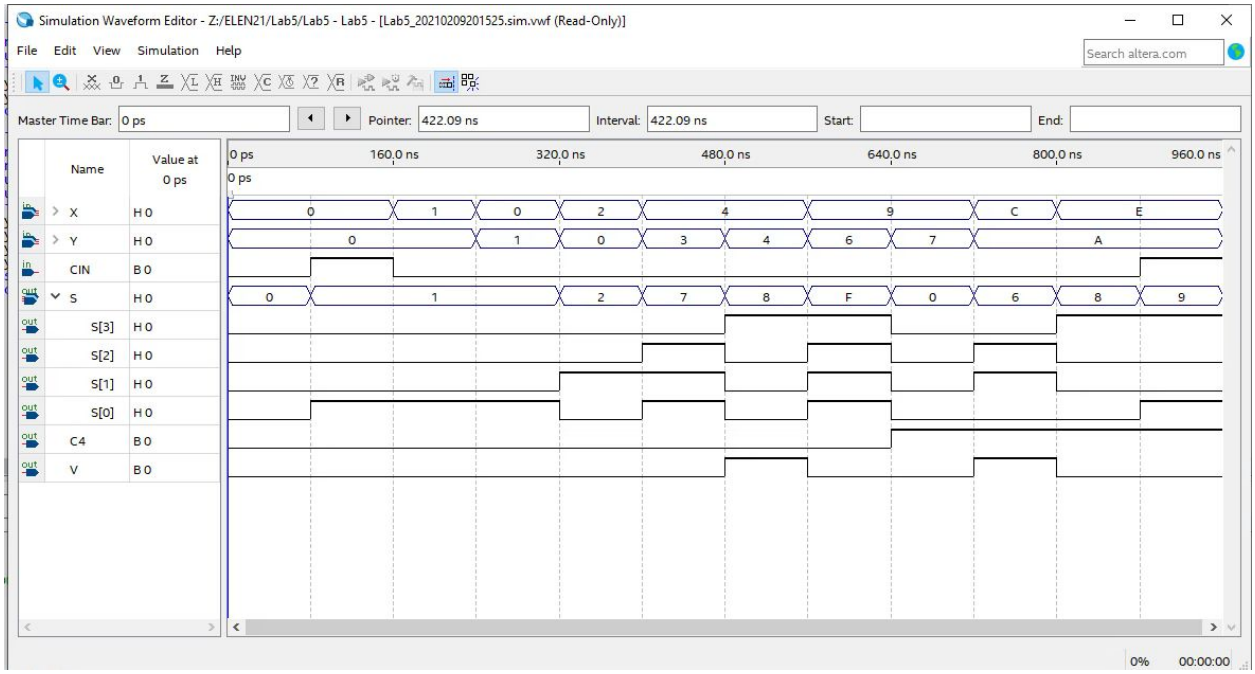
- If the circuit were completely correct except that X[1] and Y[1] were interchanged in a full adder input, would you be able to detect this based on observing outputs during testing? Why or why not?
    - You would not be able to detect that X[1] and Y[1] were interchanged because they would both be added together to get a sum that would be the same even if the order was different.

- Your TA will make available to you a waveform showing an adder circuit that is not behaving correctly; there is some incorrect wiring inside the adder.
    - Identify exactly where it's misbehaving, i.e., where it showing incorrect results.
        - Column 3 and 4 have the wrong sum. (240 ns - 480 ns)
        - Also the lat 4 columns have the wrong sums (600 ns - 1000 ns)

    - Make a guess (a hypothesis) about what might be wrong, which would explain the incorrect behavior.
        - Our hypothesis is that the carry_in and carry_out between the full adders is wrong.
    - Identify another test (i.e., a set of input stimulus) that might help prove or disprove your hypothesis.
        - We can test this hypothesis by checking each carry_in and carry_out of each smaller adder is working properly by checking them one at a time. We would set our input to stimulate one carry out and carry in connection while the others are set to zero.

```
1
2   module myfulladd(X,Y,CIN,SOUT,COUT);
3      input X,Y,CIN;
4      output SOUT,COUT;
5
6      assign SOUT = X ^ Y ^ CIN;
7      assign COUT = (X & Y) | (Y & CIN) | (X & CIN);
8   endmodule
9
10
11  module myadder2(X1,X0,Y1,Y0,C0,S1,S0,C2);
12     input X1,X0,Y1,Y0,C0;
13     output S1,S0,C2;
14     wire C1;
15     myfulladd(X0,Y0,C0,S0,C1);
16     myfulladd(X1,Y1,C1,S1,C2);
17  endmodule
18
19  module myadder4(X,Y,C0,S,C4,V);
20     input C0;
21     input [3:0]X,Y;
22     output [3:0]S;
23     output C4,V;
24     wire [3:1]C;
25     myfulladd(X[0],Y[0],C0,S[0],C[1]);
26     myfulladd(X[1],Y[1],C[1],S[1],C[2]);
27     myfulladd(X[2],Y[2],C[2],S[2],C[3]);
28     myfulladd(X[3],Y[3],C[3],S[3],C4);
29     assign V= C[3] ^ C4;
30  endmodule
```


myadder4
X[3..0]
Y[3..0]
CIN
INPUT
VCC
X[3..0]
Y[3..0]
C0
S[3..0]
C4
V
OUTPUT
S[3..0]
C4
V
inst


Simulation Waveform Editor - Z:/ELEN21/Lab5/Lab5 - Lab5 - [Lab5_20210209201525.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 422.09 ns
Interval: 422.09 ns
Start:
End:
Name
Value at 0 ps
X H 0
Y H 0
CIN B 0
S H 0
S[3] H 0
S[2] H 0
S[1] H 0
S[0] H 0
C4 B 0
V B 0
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
0 1 0 2 4 9 C E
0 1 0 3 4 6 7 A
0 1 2 7 8 F 0 6 8 9
0%
00:00:00

Inputs				Outputs Observed			
4-bit inputs (in hex)				4-bit sum		Extra outputs	
X	Y	C0		S		V	C4
0	0	0		0		0	0
0	0	1		1		0	0
1	0	0		1		0	0
0	1	0		1		0	0
2	0	0		2		0	0
4	3	0		7		0	0
4	4	0		8		1	0
9	6	0		15		0	0
9	7	0		0		0	1
C	A	0		6		1	1
E	A	0		8		0	1
E	A	1		9		0	1