Homework 5

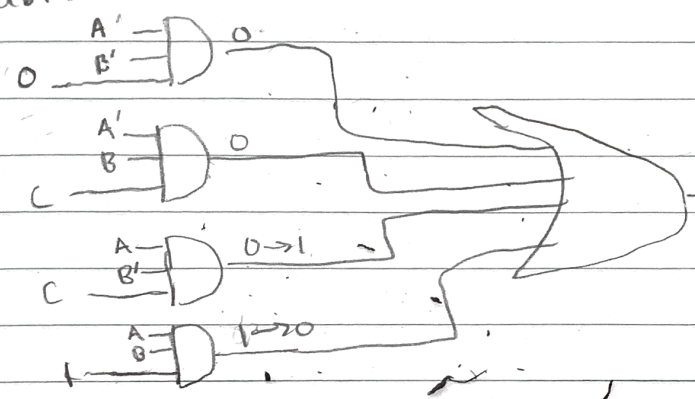
1(a)

c \ ab	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$X = Ac' + BC$

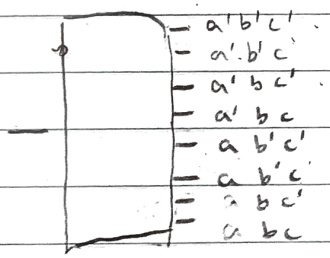
If A=B=1 and C changes there can be a static 1 hazard due to gate delays and changing.

1(c) $X = ab + c(a \oplus b)$



If B flips, it can change the output to zero for a moment between gate delays before switching back to 1

1(d)



In a 3:8 decoder, there is a static 1 hazard between all minterms because any change will change all to zero but one will change to 1 after going through gate delays with in the decoder.

1(b) $X = ab + c(a \oplus b)$

C \ ab	00	01	11	10
0	0	0	1	0
1	0	1	1	1

static hazard

If a flips or b flips when the other one equals 1, then they can cause a static hazard, due to gate delay.

ELEN 21, COEN 21: Logic Design Winter 2021

Homework 5

due Wednesday 10 February 2021

1. For the following implementations of a three-input majority circuit, identify any static 1 hazards. For each static 1 hazard, specify the input values and the single input change that would cause the hazard to appear.

   a. In a minimized SOP form
   b. In the form of the carry out of the full adder: $c_{k+1} \equiv a_k \cdot b_k + c_k \cdot (a_k \oplus b_k)$
   c. Using a 4:1 Mux with two of the three inputs connected to the selects
   d. Using a 3:8 decoder

2. Complete the timing diagram below for the circuit in Figure 5.4a, explicitly including the effect a delay of ΔT between a change in the input values and the response at the output. Each square has a duration of ΔT and the initial state is Qa=0 and Qb=1.

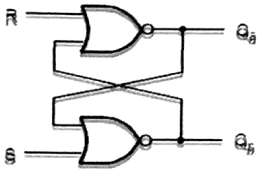
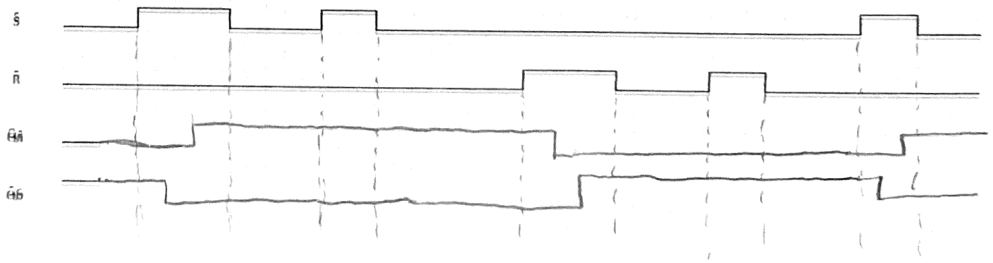
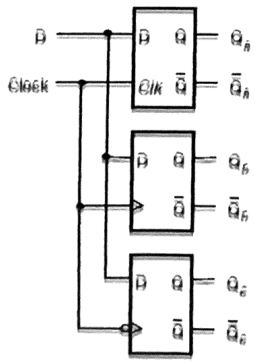
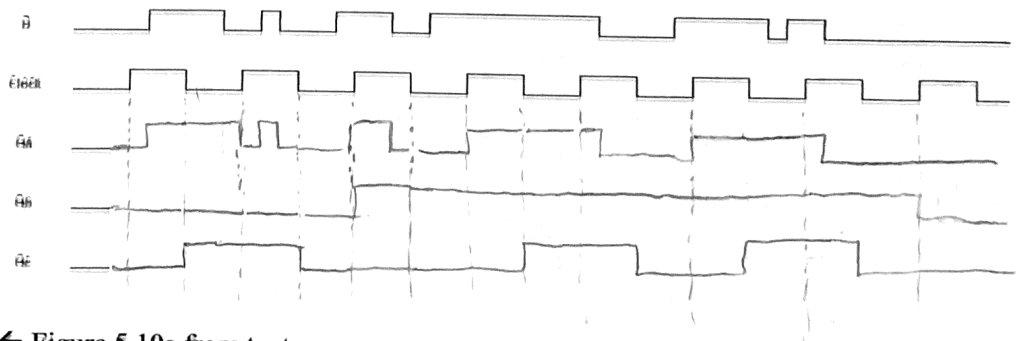


Figure 5.4 a from text



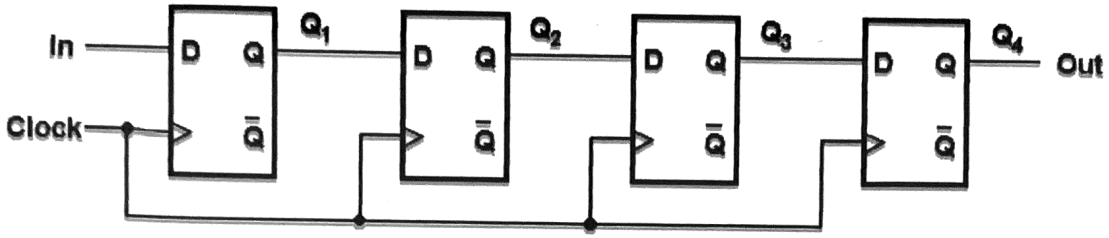
3. Complete the timing diagram below for the circuit shown in Figure 5.10a. Do not explicitly show gate delays. Use the functional definition for the latch and flip-flop, and assume that the setup and hold requirements are satisfied.

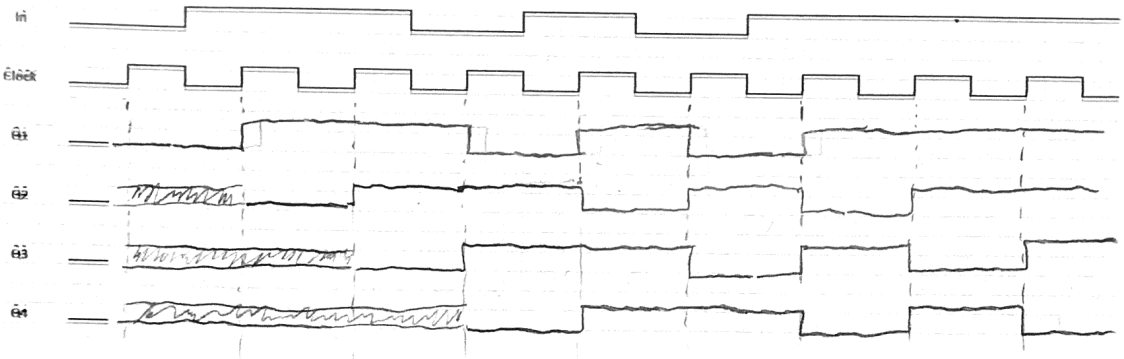




← Figure 5.10a from text

4. For the circuit in Figure 5.17a, complete the timing diagram below. Assume set-up and hold time requirements are met. Do not explicitly show propagation delays through the flip-flops.





5. Modify the circuit in Figure 5.17a to allow a synchronous clear option. If an input ClearReg is 1, all four flip-flops should be cleared on a rising clock edge. If the input ClearReg is 0 the circuit should function as it did before the modification.