ELEN 21, COEN 21: Logic Design Winter 2021

Homework 3

due Wednesday, January 27 at 11:59 pm

1. (15 points) The following functions below are implemented with multiplexers with select and data input connections specified. For each circuit, write an algebraic expression for the output, f, in terms of the function input variables. Also show a truth table and a K-map for each function.
    a. f(a,b) is implemented with a 4:1 MUX with the following connections: s1=a, s0=b, w0=0, w1=1, w2=1, w3=0.
    b. f(a,b) is implemented with a 2:1 MUX with the following connections: s=b, w0=a, w1=a'.
    c. f(a,b,c) is implemented with a 4:1 MUX with the following connections: s1=b, s0=c, w0=0, w1=a, w2=a, w3=1.
    d. f(a,b,c) is implemented with a 2:1 MUX with the following connections: s=c, w0=a', w1=b.
    e. f(a,b,c) is implemented with a 2:1 MUX with the following connections: s=a, w0=(b+c'), w1=(bc).

2. (10 points)A multiplexer can be used as a general building block for synthesis of logic functions. For the function $f(w_1, w_2, w_3) = \sum m\,(0,4,6,7)$:
    a. Show the implementation of this function using a single 8:1 MUX. Clearly label all the inputs to the MUX. Use a block graphical symbol for the 8:1 MUX.
    b. Write the algebraic expression for the function as the Shannon expansion: $f(w_1, w_2, w_3) = {w_1}' \cdot f(0, w_2, w_3) + w_1 \cdot f(1, w_2, w_3)$.
    Show the implementation of this function using a single 2:1 MUX with s=w_1 and as many AND, OR, and NOT gates as needed. Clearly label all the inputs to the MUX. Use a block graphical symbol for the 2:1 MUX.
    c. Repeat (b) for s=w_2.
    d. Repeat (b) for s=w_3.
    e. Compare the complexity of the implementations for (b), (c), and (d).

3. (10 points) Repeat the previous problem for $f(a, b, c) = (ab) \oplus (ac)$.

4. (15 points) Large multiplexers can be designed using a hierarchy of smaller multiplexers.
    a. Use a single 4:1 multiplexer and as many 2:1 multiplexers as needed to make an 8:1 multiplexer. Draw the circuit for it using block graphical symbols for the 4:1 and 2:1 multiplexers. Explicitly label all inputs and outputs of each multiplexer.
        i. Show all the multiplexer outputs in terms of the MUX data inputs for $s_2\ s_1\ s_0 = 1\ 1\ 0$.
        ii. Show all the multiplexer outputs in terms of the MUX data inputs for $s_2\ s_1\ s_0 = 0\ 1\ 1$.
    b. Repeat (a) using two 4:1 multiplexers and as many 2:1 multiplexers as needed.
    c. Compare the implementations in parts (a) and (b).

5. (15 points) Large decoders can be designed using a hierarchy of smaller decoders.
    a. Write the truth table for a 1:2 decoder with an enable input, and draw the circuit for it using AND, OR, and NOT gates as needed.
    b. Use 1:2 decoders with enable inputs to make a 2:4 decoder with an enable input. Draw the circuit for it using block graphical symbols for the decoders rather than individual AND, OR, and NOT gates. Explicitly label all inputs and outputs of each 1:2 decoder
        i. How many 1:2 decoders are needed?
        ii. Can the circuit be designed using only 1:2 decoders and no other logic components?
    c. Use a single 2:4 decoder and as many 1:2 decoders as needed to make a 3:8 decoder. Draw the circuit for it using block graphical symbols for the decoders. Explicitly label all inputs and outputs of each decoder
        i. Show all the decoder outputs for $w_2\ w_1\ w_0 = 1\ 1\ 0$.
        ii. Show all the decoder outputs for $w_2\ w_1\ w_0 = 0\ 1\ 1$.

6. (10 points) Interpret the binary values below as unsigned integers and convert them to decimal values.
    a. $(101011)_2$ b. $(0101011)_2$ c. $(0011111)_2$ d. $(111100)_2$ e. $(111110)_2$

7. (10 points) Interpret the binary values in the previous problem as signed integers in 2's complement form and convert them to decimal values.