Homework 9

1a. 1024 bits $n = 16$

$\frac{1024 \text{ bits}}{16 \text{ bits per word}} = 64 \text{ words}$ 6:64 decoder needed

6 bits in address

1b. 1024 bits $n = 8$

$\frac{1024 \text{ bit}}{8 \text{ bits per word}} = 128 \text{ words}$ 7:128 decoder needed

7 bits in address

1c. 1024 bits $n = 64$

$\frac{1024 \text{ bits}}{64 \text{ bits per word}} = 16 \text{ words}$ 4:16 decoder needed

4 bits in address

2. Initial:

Data = 001010, R1 = 010110, R2 = 111000, R3 = 000001

Clk Signal 1

$S_1 S_0 = 11$

$R_1 = 000001$, $R_2 = 111000$, $R_3 = 000001$

Clk Signal 2

$S_1 S_0 = 10$

$R_1 = 000001$, $R_2 = 111000$, $R_3 = 111000$

Clk Signal 3

$S_1 S_0 = 01$

$R_1 = 000001$, $R_2 = 111000$, $R_3 = 111000$

Clk Signal 4

$S_1 S_0 = 00$

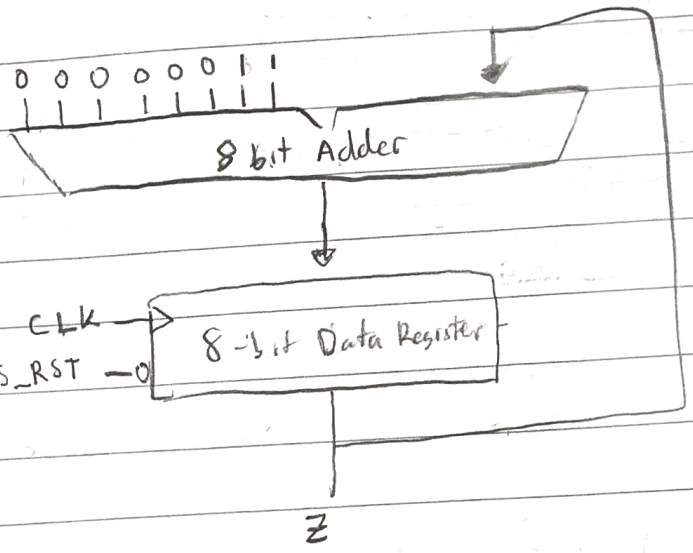
$R_1 = 000001$, $R_2 = 001010$, $R_3 = 111000$

Clk Signal 5

$S_1 S_0 = 11$

$R_1 = 000001$, $R_2 = 001010$, $R_3 = 111000$

3a.



3b. After first rising clock edge - Output is 3.

After second rising clock edge - output is 6

After third rising clock edge - output is 9

After 85th rising clock edge - Output is 255

After 86th rising clock edge - Output is 2.

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  1111 1111
  0000 0011
1 0000 0010
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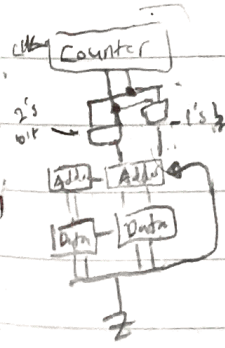
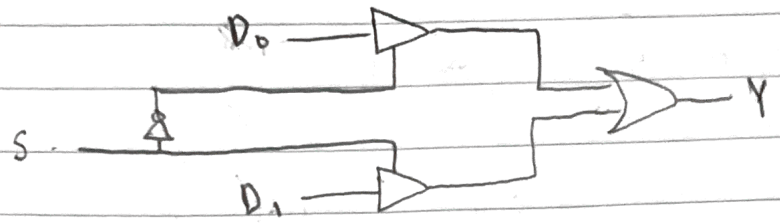
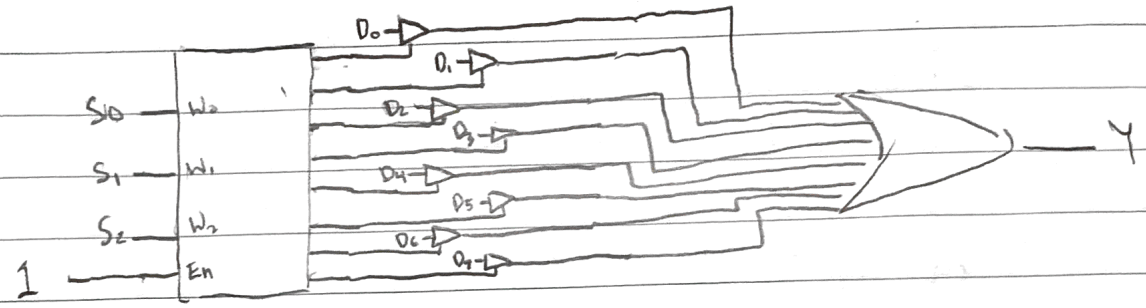
3c If I had a simple binary up counter with a smaller adder and smaller data storage register, I would have a two bit up counter and however many smaller adders and smaller data storage registers connected together to make one 8 bit adder and 8 bit data storage. The carry out one adder would be the carry in for another adder, The Q_n of data register with be the input for another register. The adders will only add when



4. 2:1 MUX using tri state driver



8:1 MUX using 3:8 decoder and tri-state drivers



5a. 1001 0011 Even number of 1's, so no error

5b. 1001 1110 Odd number of 1's (5 1's)
Therefore there is a bit error.

All possible words

- 1001 1100
- 1000 1110
- 1011 1110
- 1001 1010
- 0001 1110
- 1101 1110
- 1001 0110
- 1001 1111
- 1011 1110

5c. 0010 1100 Odder number of 1's (3 1's)
Therefore there is a bit error

Possible Words

- 0010 1101
- 0010 0100
- 0110 1100
- 0010 1110
- 0011 1100
- 1010 1100
- 0010 1000
- 0000 1100

5d. 01010101 Even number of 1's, so no error

6. 1100 1100 PT D3 D2 D1 P4 D0 P2 P1

C1: P1 ⊕ D0 ⊕ D1 ⊕ D3 = 0 ⊕ 1 ⊕ 0 ⊕ 1 = 0

C2: P2 ⊕ D0 ⊕ P2 ⊕ D3 = D ⊕ 1 ⊕ 0 ⊕ 1 = 0

C4: P4 ⊕ D1 ⊕ D2 ⊕ D3 = 1 ⊕ 0 ⊕ 0 ⊕ 1 = 0

CT: PT ⊕ D3 ⊕ D2 ⊕ D1 ⊕ P4 ⊕ D0 ⊕ P2 ⊕ P1 =

= 1 ⊕ 1 ⊕ 0 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 ⊕ 0 = 0

CT = 0

C4 C2 C1 = 000

Number of bit errors = 0

Correct 8-bit word = 1100 1100

Correct 4 bit data word = 1001

0011 0010 PT D3 D2 D1 P4 D0 P2 P1

C1: 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1

C2: 1 ⊕ 0 ⊕ 1 ⊕ 0 = 0

C4: 0 ⊕ 1 ⊕ 1 ⊕ 0 = 0

CT: 0 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1

CT = 1

C4 C2 C1 = 001

Number of bit errors = 1

Correct 8 bit word = 0011 0011

Correct 4 bit word = 0110

1011 1010 PT D3 D2 D1 P4 D0 P2 P1

$C1 = P_1 \oplus D_0 \oplus D_1 \oplus D_3 = 0 \oplus 0 \oplus 1 \oplus 0 = 1$

$C2 = P_2 \oplus D_0 \oplus D_2 \oplus D_3 = 1 \oplus 0 \oplus 1 \oplus 0 = 0$

$C4 = P_4 \oplus D_1 \oplus D_2 \oplus D_3 = 1 \oplus 1 \oplus 1 \oplus 0 = 1$

$CT = PT \oplus D_3 \oplus D_2 \oplus D_1 \oplus P_4 \oplus D_0 \oplus P_2 \oplus P_1 = 1$

CT = 1

C4C2C1 = 101

Number of bit errors = 1

Correct 8 bit word = 10101010

Correct 4 bit word = 1010

0010 0010 PT D3 D2 D1 P4 D0 P2 P1

$C1 = 0 \oplus 0 \oplus 0 \oplus 0 = 0$

$C2 = 1 \oplus 0 \oplus 1 \oplus 0 = 0$

$C4 = 0 \oplus 0 \oplus 1 \oplus 0 = 1$

$CT = 0 \oplus 0 \oplus 1 \oplus 0 \oplus 0 \oplus 0 \oplus 1 \oplus 0 = 0$

CT = 0

C4C2C1 = 100

Number of bit errors = 2

Correct 8 bit word = ——— Don't know since we don't know where the 2 bit errors are.

Correct 4 bit word = ———