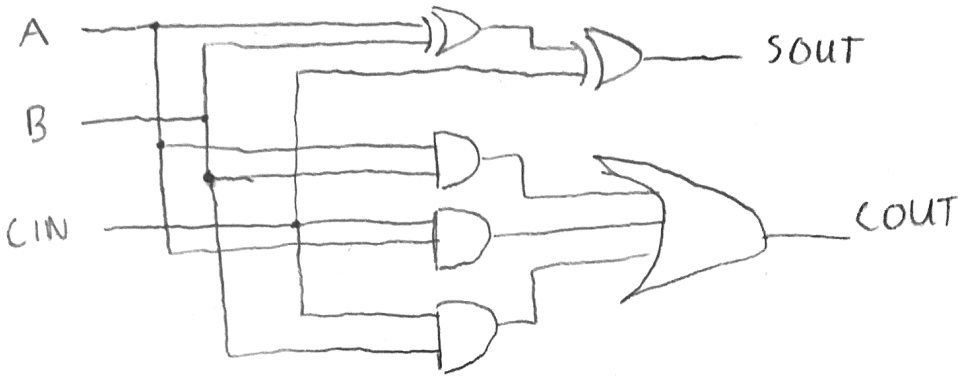
Pre-Lab 5

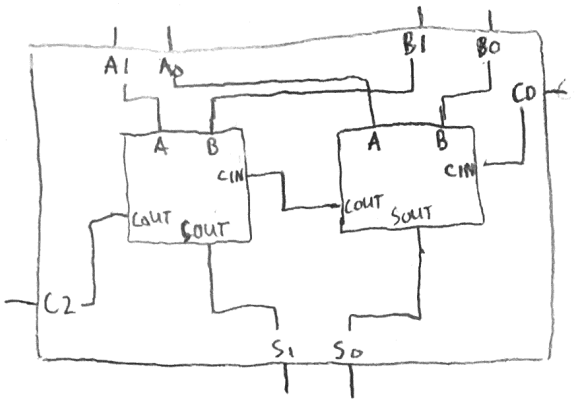
1) $SOUT = (A \oplus B) \oplus CIN$

$COUT = AB + ACIN + BCIN$

2)



3)



From inputs A1, A0, B1, B0 and CO to output C2, there are 8 gates.

4)

```
module myfulladd (A,B,CIN, SOUT, COUT);
        input A, B, CIN;
        output SOUT, COUT;
        assign SOUT = (A^B)^CIN;
        assign COUT = (A&B) | (A&CIN) | (B&CIN);
endmodule;
```

5)

```
module myadder2 (A1, A0, B1, B0, C0, S1, S0, C2);
        input A1, A0, B1, B0, C0;
        output S1, S0, C2;
        wire C1;
        myfulladd f1 (A0, B0, C0, S0, C1);
        myfulladd f2 (A1, B1, C1, S1, C2);
endmodule;
```

6) In order to test the 2-bit adder, I would first test all of the inputs' connections to make sure that they are properly connected to right single full adder component.

- Test each input connection by having that input be 1 and the rest is 0. We know what the outcome should be.
  - * First test A_0 and B_0.
  - * Then C_0
  - * Next C_1
  - * Then A_1 and B_1
  - * Then test C_2 by have A_1 and B_1 be 1.

- If all inputs are set to 0, the outputs should also all be 0.
- If for each input is set to 1 and all other inputs are 0...

$C_{IN}=1 \Rightarrow S_0=1, S_1=0, C_2=0$

$A_0=1 \Rightarrow S_0=1, S_1=0, C_2=0$

$B_0=1 \Rightarrow S_0=1, S_1=0, C_2=0$

$A_1=1 \Rightarrow S_0=0, S_1=1, C_2=0$

$B_1=1 \Rightarrow S_0=0, S_1=1, C_2=0$

- To test individual internal carry connection...

$A_0=1, B_0=1 \Rightarrow C_1=1 \therefore S_1=1 \;\&\; S_0=0$

$A_1=1, B_1=1 \Rightarrow C_2=1 \therefore S_1=0 \;\&\; S_0=0$

$C_{IN}=1, A_0=0, B_0=0 \Rightarrow C_1=0 \;\&\; S_0=1$