ELEN 21, COEN 21: Logic Design Winter 2021

Homework 4

due Wednesday 3 February 2021

1. A circuit uses four full adder blocks for a ripple carry adder in the manner shown in Figure 3.5.
    a. Draw the circuit using the four full adder circuit blocks connected so that they will add X=$(9)_{10}$ and Y= $(5)_{10}$ to produce a four bit sum and a carry out. Do NOT draw the circuitry inside the full adder block, but show all wired connections to input values and between full adder components. Label all inputs and outputs.
    b. Find the logic values of all the outputs of the full adder blocks for the X and Y inputs specified. What is the decimal value of the 4-bit sum? What is the carry_out?
    c. Repeat (a) and (b) using X=$(13)_{10}$ and Y= $(10)_{10}$. Is the sum correct? Explain.
    d. Assume that the time delay for a logic gate output to change in response to a change in a gate input is ΔT. What is the total delay time to a stable output level for each of the outputs of a full adder component if X and Y inputs change at $= t_0$? What is the total delay time to a stable output level for each of the five outputs of your 4-bit ripple carry adder if X and Y inputs change at $= t_0$?

2. A two-level circuit to add multi-bit binary values would be faster than a ripple carry adder using full adder circuits, but it would require more gates. Design a three-level circuit using three 4:1 Multiplexers to add two 2- bit binary values, a1 a0 and b1 b0. There is no carry-in for this adder. (To avoid possible confusion from using s for MUX selects and s for sum bits, we will call the adder output R, not S, for this problem.) The three 4:1 multiplexers will create the three outputs c2, r1, and r0. For the select inputs to each MUX, use a1 and b1. (There will be two logic levels in the MUX and one level in some of the logic for the MUX inputs.)

    a. For a full adder, write the equations for the outputs r0 and c1 in terms of the full adder inputs a0, b0,and c0. Since there is no carry in for this adder, set c0 to zero and rewrite the equations in terms of a0 and b0.
    b. For a full adder, write the equations for the outputs r1 and c2 in terms of the full adder inputs a1, b1,and c1. Substitute the expression for c1 from part (a) into these equations.
    c. For each of the three multiplexers, write its four data inputs assuming that the MUX select inputs are connected to a1 and b1.

3. An n-bit subtractor circuit to compute A-B can be created from an n-bit adder by connecting the A bits to the A adder inputs and connecting the bitwise complement of the B bits to the B adder inputs. The carry_in should be connected to 1.
    a. For n=4, find the subtractor outputs A-B and the carry_out for the following operand pairs. Find the decimal value of the result interpreted as a signed integer in 2's complement form.

        i. A=7, B=7 ii. A=7, B=0 iii. A = 0, B = 7 iv. A=0, B=0

    b. Repeat (a) for n =3. Explain any difference between these results and the results of part (a).

4. Design a 3-bit ALU with two select inputs s1 s0 that will output one of four logical functions of inputs A and B. Use 4:1 MUXes and other components as needed.

s1 s0	operation	output
0 0	OR	Ri = Ai + Bi
0 1	AND	Ri = Ai ·Bi
1 0	NAND	Ri = (Ai ·Bi)'
1 1	XOR	Ri = Ai ⊕Bi

5. Convert the following unsigned hexadecimal values to binary and to decimal values.
    a. $(A6)_{16}$ b. $(14B)_{16}$ c. $(20D)_{16}$

6. Find the values for C (carry out) ,V (overflow for signed addition), Z (the result is zero) , and N (the result is negative) as well as the 4-bit result when the following pairs of X and Y values are added using a 4-bit adder. Assume results are interpreted as signed integers in 2's complement form.

$X=(2)_{10}$, $Y=(5)_{10}$	$X=(4)_{10}$, $Y=(-4)_{10}$	$X=(6)_{10}$, $Y=(7)_{10}$	$X=(-6)_{10}$, $Y=(-7)_{10}$