ELEN 21, COEN 21: Logic Design Winter 2021

Homework 7

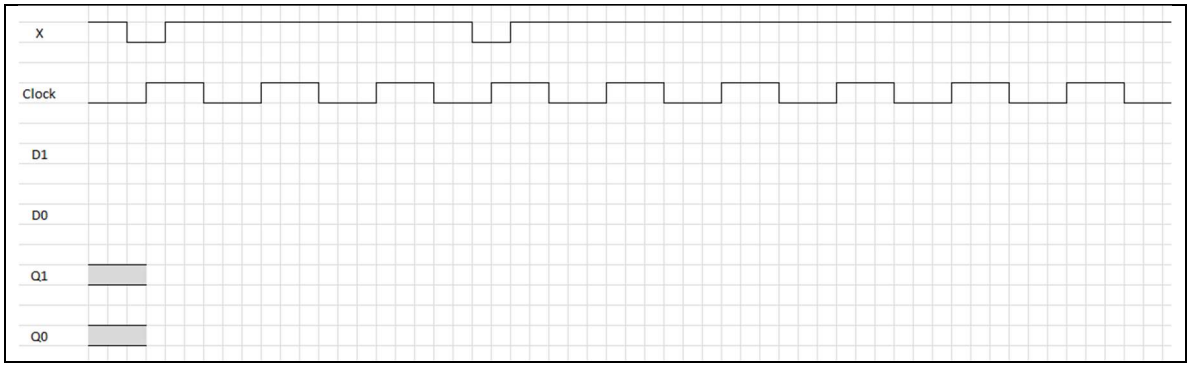
due Wednesday 24 February 2021

All problems are 15 points

1. Use the ring counter shift register circuit in Figure 5.28 with four flip-flops. Note that Q of the fourth flip-flop is connected to D of the first flip-flop, so there is no external serial input to this shift register
    a. Assume that **Start** goes to 1 so that that $Q_0\ Q_1\ Q_2\ Q_3 = 1\ 0\ 0\ 0$ and after that it remains 0. Then 16 clock cycles are applied to the circuit. List the sequence of outputs for $Q_0\ Q_1\ Q_2\ Q_3$ for the 16 clock cycles.
    b. How many different 4-bit values for $Q_0\ Q_1\ Q_2\ Q_3$ are in the output list in (a)?
    c. How many flip-flops can have an output of 1 at the same time?
    d. How many flip-flops change value on a single active clock edge?
    e. Assume that due to a wiring error, **Start** causes the flip-flops to initially be set to $Q_0\ Q_1\ Q_2\ Q_3 = 1\ 1\ 0\ 0$ instead of 1 0 0 0, and then 16 clock cycles are applied to the circuit. Write the sequence of outputs for $Q_0\ Q_1\ Q_2\ Q_3$.
    f. Assume that due to a wiring error, **Start** causes the flip-flops to initially be set to $Q_0\ Q_1\ Q_2\ Q_3 = 1\ 0\ 1\ 0$ instead of 1 0 0 0, and then 16 clock cycles are applied to the circuit. Write the sequence of outputs for $Q_0\ Q_1\ Q_2\ Q_3$.

2. Use the twisted ring counter shift register circuit in Figure 5.29 with four flip-flops. Note that Q' of the fourth flip-flop is connected to D of the first flip-flop, so there is no external serial input to this shift register
    a. Assume that **Reset_n** goes to 0 so that that $Q_0\ Q_1\ Q_2\ Q_3 = 0\ 0\ 0\ 0$ and after that it remains 1. Then 16 clock cycles are applied to the circuit. List the sequence of outputs for $Q_0\ Q_1\ Q_2\ Q_3$ for the 16 clock cycles.
    b. How many different 4-bit values for $Q_0\ Q_1\ Q_2\ Q_3$ are in the output list in (a)?
    c. How many flip-flops change value on a single active clock edge?
    d. Assume that due to a broken wire, **Reset_n** causes the flip-flops to be set to $Q_0\ Q_1\ Q_2\ Q_3 = 0\ 1\ 0\ 0$ instead of 0 0 0 0, and then 16 clock cycles are applied to the circuit. Write the sequence of outputs for $Q_0\ Q_1\ Q_2\ Q_3$.

3. A circuit has two positive edge-triggered D-type flip-flops which have a common clock signal. The two D inputs are $D_0 = X \cdot (Q_1 + Q_0')$ and $D_1 = X \cdot (Q_1 + Q_0)$ where X is an external input signal. Based on the operation of D-type flip-flops, complete the timing diagram below for the D's and Qs by stepping one clock cycle at a time to first evaluate the Ds before each active clock edge, and then set the value of the Qs after the clock edge until the following active cock edge. Assume that set-up and hold time requirements have been met. Do not explicitly show propagation delays through the flip-flops.



4. For the circuit in the previous problem, add a circuit output Z which is $Z = Q_1 \cdot Q_0$. Analyze this circuit operation for all inputs with a next state table and a state transition diagram instead of doing a simple timing diagram for one specific input sequence.
    a. Show the next state table for this circuit in the style of Figure 6.6 with present state Q1 Q0 in place of y2 y1 and input X instead of w. For the next state, evaluate D2 D1, which will be the next state since it will be the value of the flip-flop outputs after the active clock edge.
    b. Draw the state transition diagram in the style of Figure 6.3. Use the actual state values of Q_1, Q_0 rather than A, B, C, and D.
    c. What does this circuit do? When is the output 1?
    d. Create the timing diagram from the previous problem directly from the state table for the specific input sequence given and make sure that they are the same.

5. A 4-bit shift register with outputs Q_0, Q_1, Q_2, Q_3 has serial input $D_0 = Q_0 \oplus Q_3$. Note that there is no external input to this shift register. However, the shift register will have a synchronous load capability so that its starting state can be specified.
    a. Show the next state table for this shift register in the style of Figure 6.6. Use Q_0, Q_1, Q_2, Q_3 to define the states.
    b. Draw the state transition diagram for the case where the shift register is initialized to 0000.
    c. Draw the state transition diagram for the case where the shift register is initialized to 1000.