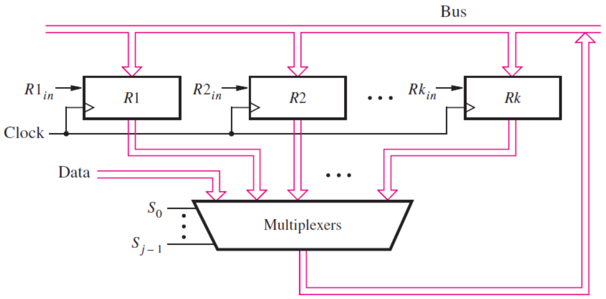
ELEN 21, COEN 21: Logic Design Winter 2021

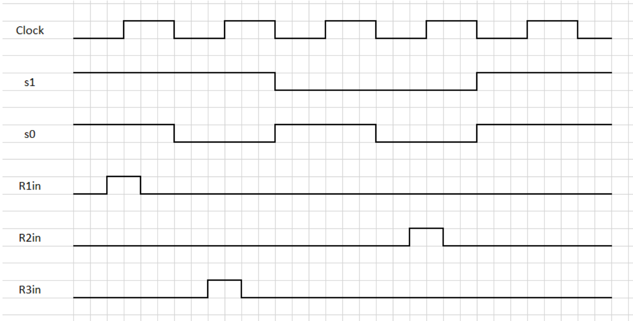
Homework 9

due Thursday 11 March 2021

1. A memory with 1024 bits is organized to access n-bit words. For each value of n, find the number of words in the memory, the size of the decoder needed to select an individual word, and the number of bits in the address needed to specify an individual word in the memory.
   a. n=16
   b. n=8
   c. n=64

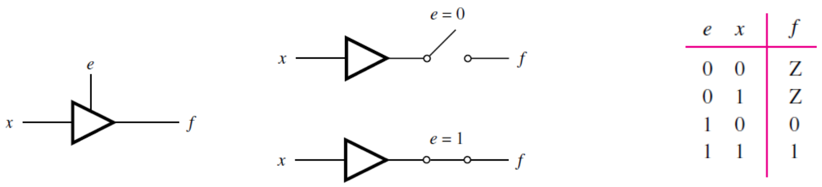
2. The data bus shown below is 6 bits wide. It has three 6-bit registers and a 6-bit data source connected to it through a MUX. The MUX selects, s1 s0, select data, R1, R2, or R3 in that order. Initially Data is 001010, R1 is 010110, R2 is 111000, and R3 is 000001. Register k will be loaded on the rising clock edge if Rk_{in} is high. Using the timing diagram below determine what value is in each register after each active clock edge.





3. An 8-bit counter that will count by 3s, i.e. it will count 0, 3, 6, 9, etc. is needed. Rather than design a custom Moore FSM for this, consider a design using only already available components, i.e.an 8-bit data storage register and an 8-bit adder. The data storage register has a clear input. When input SYS_RST is 1, the count by 3s counter output is reset to 0. When input SYS_RST is 0 and CLK input has a rising edge, the count by 3s counter output increases by three.
   a. Draw a schematic for your circuit with clearly labeled input and outputs.
   b. If the count by 3s counter is reset to zero and then SYS_RST is set to 0, what is the output after the first rising clock edge? After the second? After the third ? After the 85th? After the 86th ?
   c. If you also had access to simple binary up counters with a count enable input, how would you implement the count by 3s counter with a smaller adder and a smaller data storage register?

4. Show the circuit for a 2:1 MUX using noninverting tri-state drivers (shown below and in Figure B.62a). Show a circuit for an 8:1 MUX using a 3:8 decoder and tristate drivers as shown below.



e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

(a) A tri-state buffer

(b) Equivalent circuit

(c) Truth table

5. The four 8 bit words below each have seven bits of data with an even parity bit put in the leftmost position to make the 8 bit word have even parity. For each word determine if a bit error is detected. If a bit error is detected, list all the possible words that could be the correct value of the word if you assume only one bit error occurred.
   a. 1001 0011
   b. 1001 1110
   c. 0010 1100
   d. 0101 0101

6. The following 8bit words are formatted as discussed in class to have three parity bits and a total parity bit so that a single bit error can be corrected and two bit errors can be detected. Complete the table below for the four 8-bit words to show the value of the 4 parity error checks. Interpret the four parity error checks to determine if there are no errors, where the error is if there is one error, or if there are two errors.

	PT	**D3**	**D2**	**D1**	**P4**	**D0**	**P2**	**P1**
bit position:	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**

8-bit word formatted as shown above	CT	C4 C2 C1	Number of bit errors	Correct 8-bit word	Correct 4-bit data word D3 D2 D1 D0
1 1 0 0 1 1 0 0					
0 0 1 1 0 0 1 0					
1 0 1 1 1 0 1 0					
0 0 1 0 0 0 1 0					