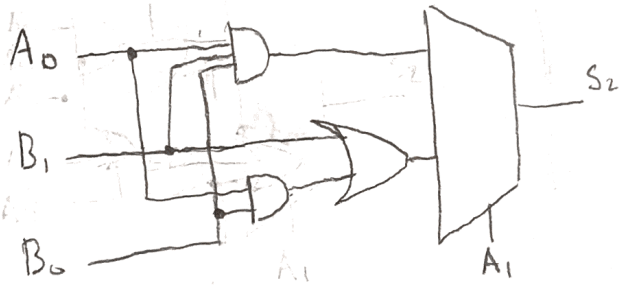
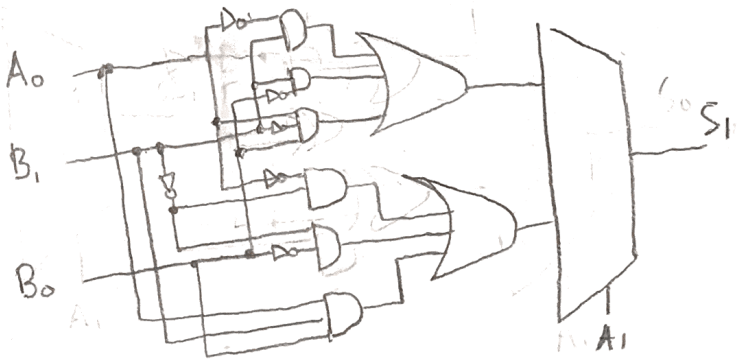
Pre-Lab 4

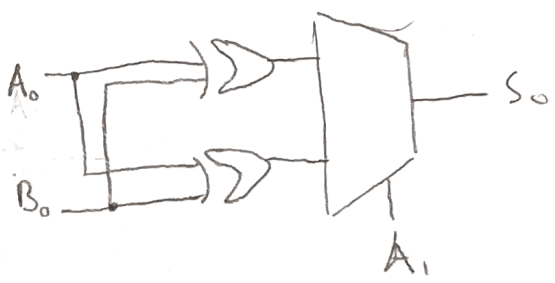
1)

	A1	A0	B1	B0	S_2	S_1	S_0
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	1	0
3	0	0	1	1	0	1	1
4	0	1	0	0	0	1	0
5	0	1	0	1	0	1	1
6	0	1	1	0	1	0	0
7	0	1	1	1	0	1	0
8	1	0	0	0	0	1	1
9	1	0	0	1	1	0	0
10	1	0	1	0	1	0	1
11	1	0	1	1	0	1	1
12	1	1	0	0	1	0	0
13	1	1	0	1	1	0	1
14	1	1	1	0	1	1	0
15	1	1	1	1			

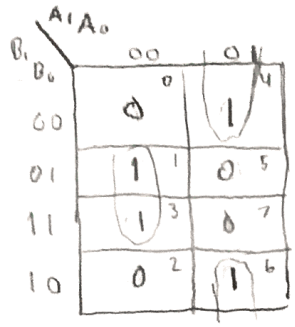
2a)

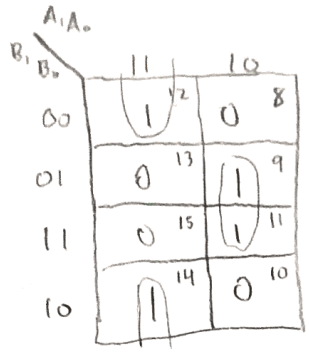






2b)

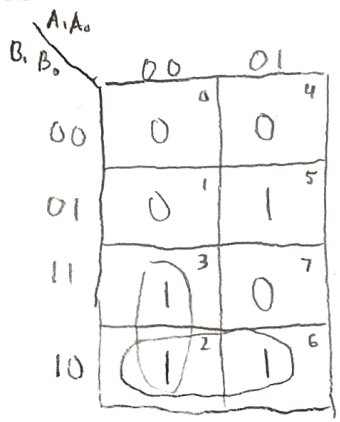


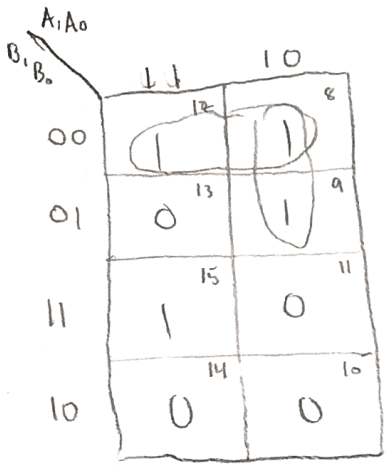


$f_{S_0}(0, A_0, B_1, B_0) = A_1' A_0 B_0' + A_1' A_0' B_0$

$f_{S_0}(1, A_0, B_1, B_0) = A_1 A_0' B_0 + A_1 A_0 B_0'$

2c) S1

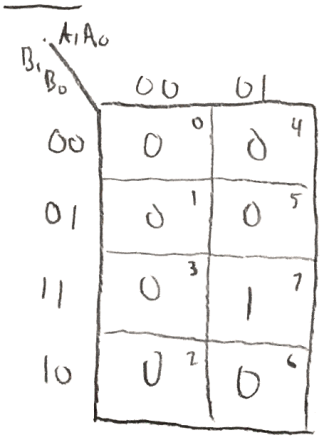


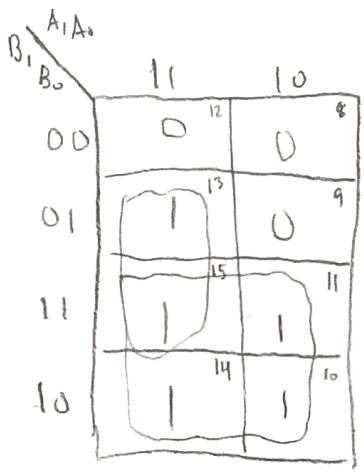


$f_{S_1}(0, A_0, B_1, B_0) = A_1' A_0' B_1 + A_1' B_1 B_0' + A_1' A_0 B_1' B_0$

$f_{S_1}(1, A_0, B_1, B_0) = A_1 A_0' B_1' + A_1 B_1' B_0' + A_1 A_0 B_1 B_0$

S2

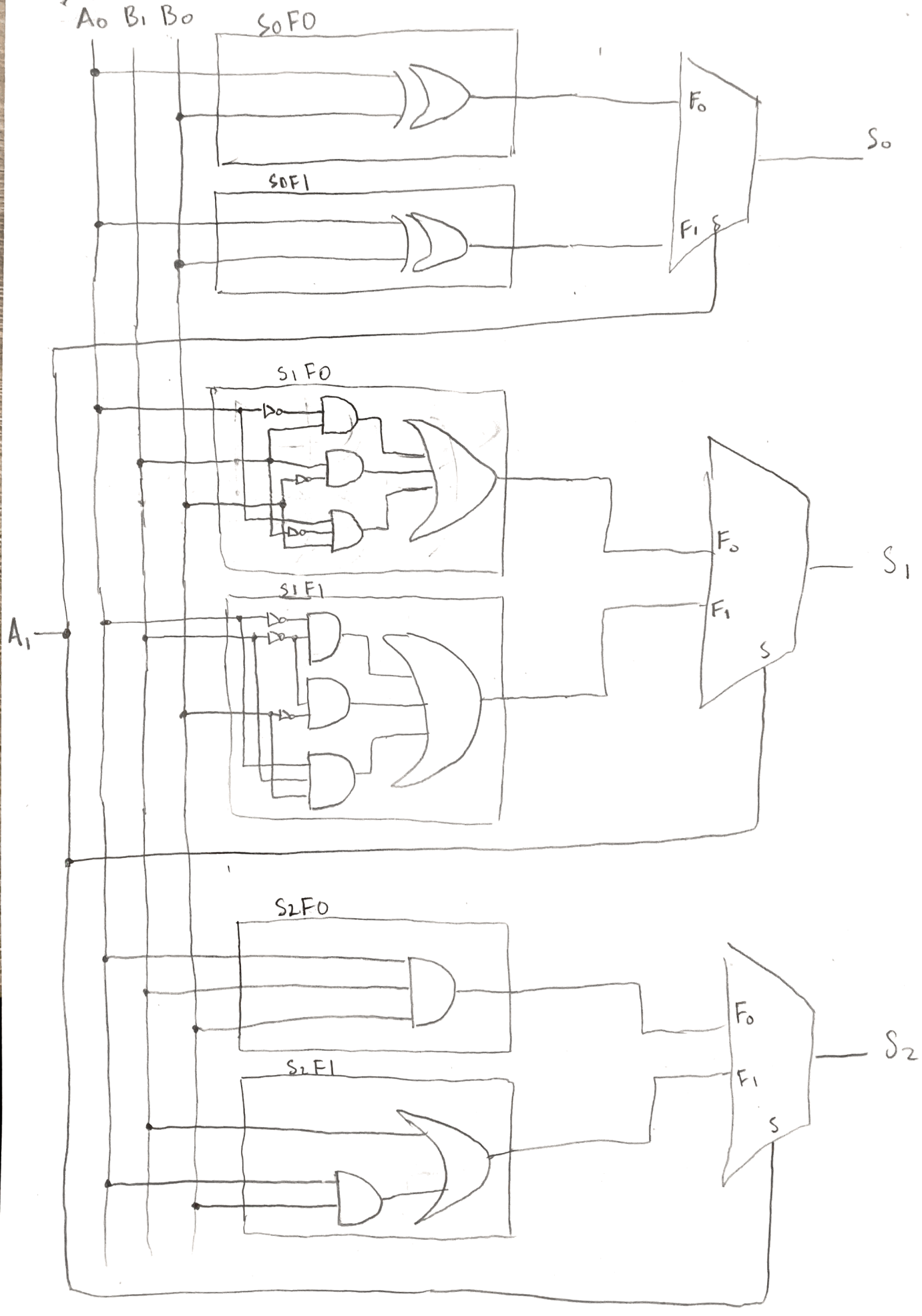




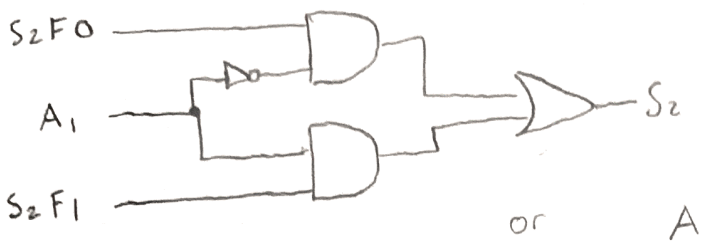
$f_{S_2}(0, A_0, B_1, B_0) = A_1' A_0 B_1 B_0$

$f_{S_2}(1, A_0, B_1, B_0) = A_1 B_1 + A_1 A_0 B_0$

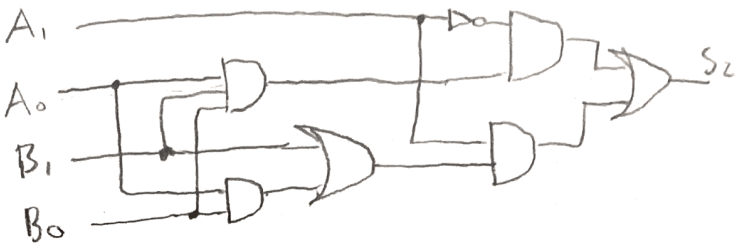
3)



4a)



or



4b)

```
wire w0, w1, w2, w3, w4, w5, w6, w7, w8, w9, w10, w11, w12;
module fulladder_s2 (a1, a0, b1, b0, s1);
    input a1, a0, b1, b0;
    output s1;
    not (w, a1);
    not (w0, a0);
    not (w1, b1);
    not (w2, b0);
    and (w3, w0, b1);
    and (w4, b1, w2);
    and (w5, a0, w1, b0);
    and (w6, w0, w1);
    and (w7, w1, w2);
    and (w8, a0, b1, b0);
    or (w9, w3, w4, w5);
    or (w10, w6, w7, w8);
    and (w11, w, w9);
    and (w12, a1, w10);
    or (s1, w11, w12);
endmodule
```

4c)

```
module fulladder_s0 (a1, a0, b1, b0, s0);
    input a1, a0, b1, b0;
    output s0;
    assign f = (~a1 &((a0 &~b0)|(~a0&b0))) | (a1 &((a0&~b0)|(~a0&b0)));
endmodule
```