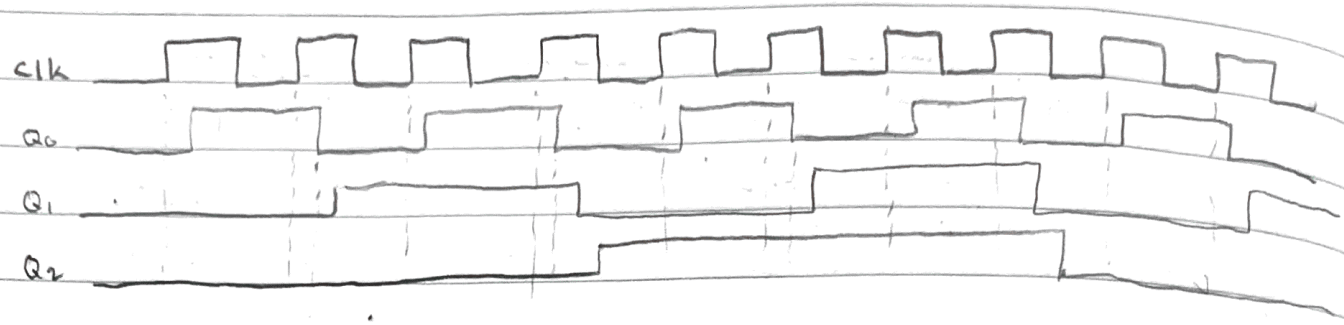
Homework 6

1a.

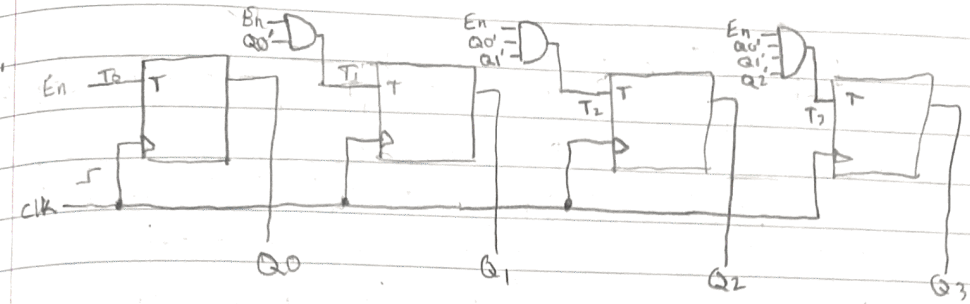


b. You can obtain the needed frequencies by scaling down our current counter. So $\frac{16}{64} = 0.25$, therefore to design a 16 MHz clock from a 64 MHz clock it needs to be scaled down by 0.25x. So everything will be a fourths of what it was when it was 64 MHz. For 2 MHz, it would be scaled down to $\frac{1}{32}$ of the 64 MHz So the minimum time between the clock oscillating is 62.5ns for 16 MHz and 500ns for 2 MHz

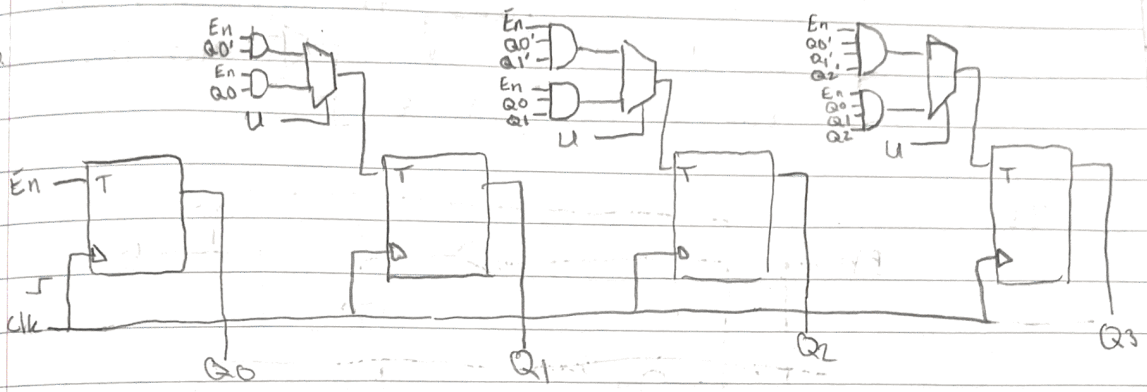
c. The lowest frequency clock signal is 1 MHz, because the max nanoseconds is 1000ns and to get frequency it is $\frac{1000ns}{x\,ns}$ so $\frac{1000ns}{1000ns} = 1\,MHz$.

d. Yes. You could obtain the needed clock frequencies in part b, using a down counter, because it the same amount of bits and there is a change the least significant bits every time, only difference is that Q_0, Q_1, Q_2 start at 1 rather than 0.

2 a.



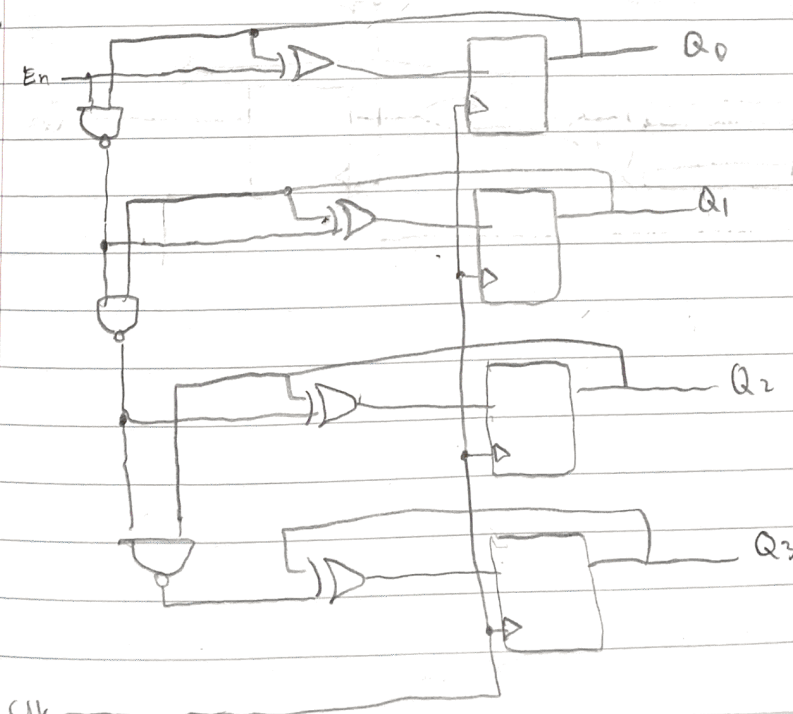
b.



T0: Down - En T1: Down - En · Q0' T2: Down - En · Q0' · Q1' T3: Down - En · Q0' · Q1' · Q2'

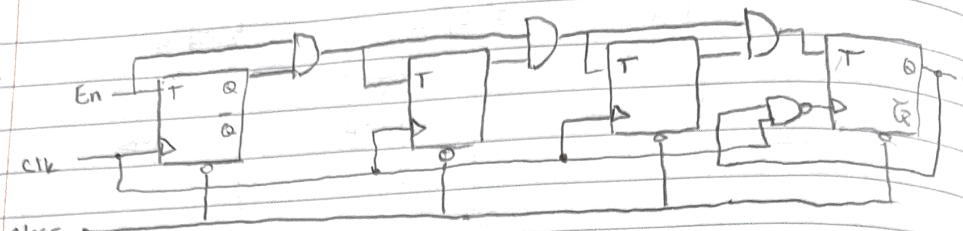
Up - En Up - En · Q0 Up - En · Q0 · Q1 Up - En · Q0 · Q1 · Q2

3a.



3b is on the next page after 4.

4.



Using an nand gate, the clock will stop flip-flops for Q_3 when $Q_3 = 1$. This prevents Q_3 from changing when the counter hits 8.

3b.