

# 1. Description

# 1.1. Project

Project Name	Label_Feader
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	08/31/2022

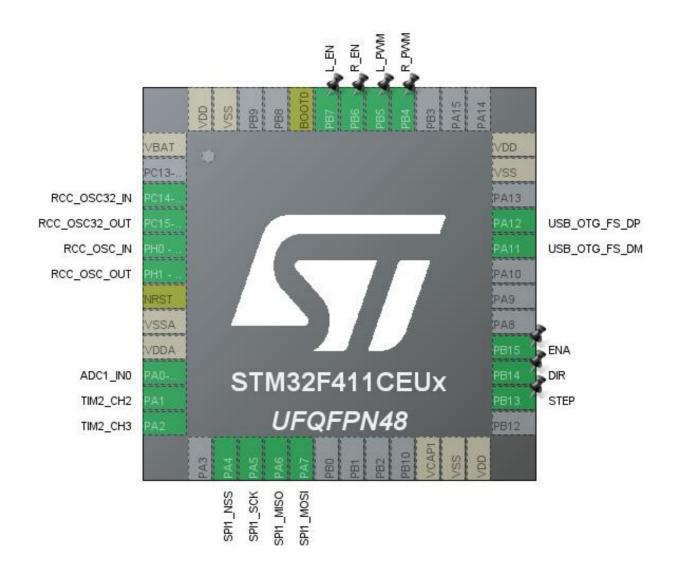
## 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

# 1.3. Core(s) information

Core(s)	Arm Cortex-M4

# 2. Pinout Configuration

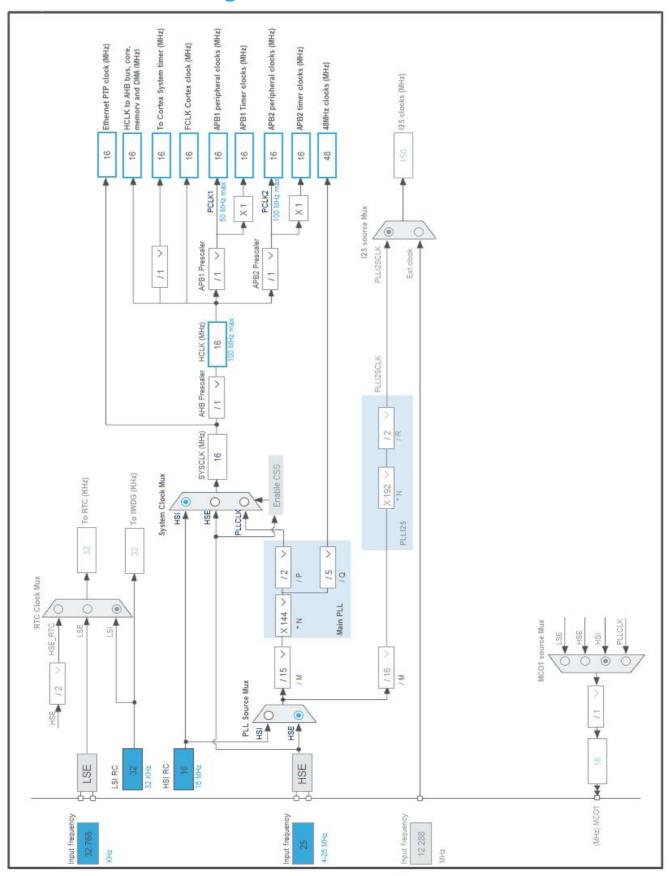


# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
UFQFPN48	(function after		Function(s)	
	reset)		` ,	
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
11	PA1	I/O	TIM2_CH2	
12	PA2	I/O	TIM2_CH3	
14	PA4	I/O	SPI1_NSS	
15	PA5	I/O	SPI1_SCK	
16	PA6	I/O	SPI1_MISO	
17	PA7	I/O	SPI1_MOSI	
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
26	PB13 *	I/O	GPIO_Output	STEP
27	PB14 *	I/O	GPIO_Output	DIR
28	PB15 *	I/O	GPIO_Output	ENA
32	PA11	I/O	USB_OTG_FS_DM	
33	PA12	I/O	USB_OTG_FS_DP	
35	VSS	Power		
36	VDD	Power		
40	PB4 *	I/O	GPIO_Analog	R_PWM
41	PB5 *	I/O	GPIO_Analog	L_PWM
42	PB6 *	I/O	GPIO_Output	R_EN
43	PB7 *	I/O	GPIO_Output	L_EN
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

Name	Value	
Project Name	Label_Feader	
Project Folder	C:\Users\mprzybyl\STM32CubelDE\workspace_1.10.1\Label_Feader	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_SPI1_Init	SPI1
6	MX_USB_DEVICE_Init	USB_DEVICE
7	MX_TIM2_Init	TIM2

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEUx
Datasheet	DS10314_Rev6

### 6.2. Parameter Selection

Temperature	25
Vdd	1.7

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

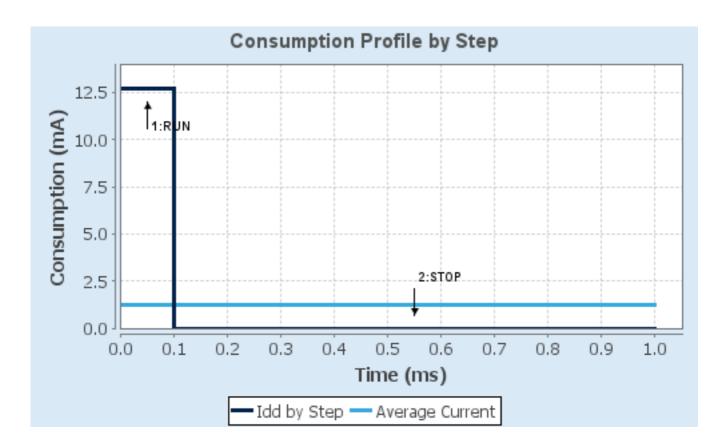
## 6.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-
		PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 µA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	104.31	105
Category	In DS Table	In DS Table

## 6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

## 6.6. Chart



# 7. Peripherals and Middlewares Configuration

# 7.1. ADC1 mode: IN0

#### 7.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 0
Sampling Time 3 Cycles

ADC\_Injected\_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

**System Parameters:** 

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.3. SPI1

**Mode: Full-Duplex Master** 

Hardware NSS Signal: Hardware NSS Output Signal

7.3.1. Parameter Settings:

**Basic Parameters:** 

Frame Format Motorola

Data Size 16 Bits \*

First Bit MSB First

**Clock Parameters:** 

Prescaler (for Baud Rate) 8 \*

Baud Rate 2.0 MBits/s \*

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

**Advanced Parameters:** 

CRC Calculation Disabled

NSS Signal Type Output Hardware

7.4. TIM2

Clock Source: Internal Clock
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3

7.4.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 15 \*
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value ) 127 \*

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

**PWM Generation Channel 3:** 

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

#### 7.5. USB\_OTG\_FS

#### Mode: Device\_Only

#### 7.5.1. Parameter Settings:

Speed Device Full Speed 12MBit/s

Low powerDisabledLink Power ManagementDisabledVBUS sensingDisabledSignal start of frameDisabled

#### 7.6. USB\_DEVICE

#### Class For FS IP: Communication Device Class (Virtual Port Com)

#### 7.6.1. Parameter Settings:

#### **Basic Parameters:**

USBD\_MAX\_NUM\_INTERFACES (Maximum number of supported interfaces)

1
USBD\_MAX\_NUM\_CONFIGURATION (Maximum number of supported configuration)

1
USBD\_MAX\_STR\_DESC\_SIZ (Maximum size for the string descriptors)

512
USBD\_SELF\_POWERED (Enabled self power)

Enabled

USBD\_DEBUG\_LEVEL (USBD Debug Level) 0: No debug message

**Class Parameters:** 

USB CDC Rx Buffer Size 64 \*

USB CDC Tx Buffer Size 64 \*

### 7.6.2. Device Descriptor:

**Device Descriptor:** 

VID (Vendor IDentifier) 1155

LANGID\_STRING (Language Identifier)

English(United States)

MANUFACTURER\_STRING (Manufacturer Identifier)

Aplisens S.A. \*

**Device Descriptor FS:** 

PID (Product IDentifier) 22336

PRODUCT\_STRING (Product Identifier) STM32 Label Feader V0.1 \*

CONFIGURATION\_STRING (Configuration Identifier)

INTERFACE\_STRING (Interface Identifier)

CDC Interface

CDC Interface

<sup>\*</sup> User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	STEP
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	DIR
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENA
	PB4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	R_PWM
	PB5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	L_PWM
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R_EN
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	L_EN

### 8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA2_Stream2	Memory To Peripheral	Low
SPI1_RX	DMA2_Stream0	Peripheral To Memory	Low

### SPI1\_TX: DMA2\_Stream2 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Half Word
Memory Data Width: Half Word

# SPI1\_RX: DMA2\_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Half Word
Memory Data Width: Half Word

# 8.3. NVIC configuration

# 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA2 stream0 global interrupt	true	0	0	
DMA2 stream2 global interrupt	true	0	0	
USB On The Go FS global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 global interrupt	unused			
TIM2 global interrupt	unused			
SPI1 global interrupt	unused			
FPU global interrupt	unused			

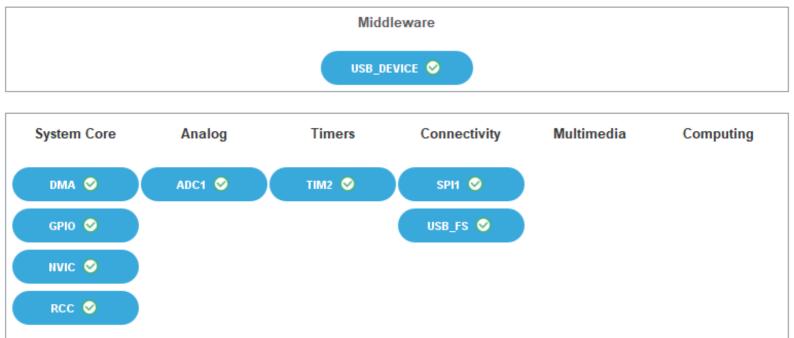
# 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true

\* User modified value

# 9. System Views

- 9.1. Category view
- 9.1.1. Current



## 10. Docs & Resources

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stm8\_embedded\_software\_solutions.pdf

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