EEE3096S
BRMKEA001, CLLSTE009
PRAC 5

Below in figure 1 are the results after using ADD, ROR, LTH and MAC with an initial ACC value of 0b00000101.

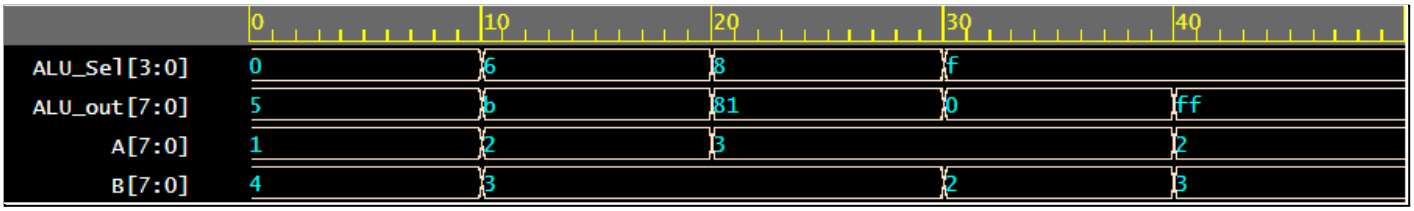

Figure 1 - waveform output

In figure 2 below is the console output.

A	B	ALU_Sel	ALU_Out
00000001	00000100	0000	00000101
00000010	00000011	0110	00001011
00000011	00000011	1000	10000001
00000011	00000010	1111	00000000
00000010	00000011	1111	11111111

Figure 2 - Console output

The A and B values were changed for each test. Below in table 1 is the A, B and accumulator values, the test ran, the expected output and the measured output.

	A	B	Acc init	Expected Output	Measured Output
ADD (A+B)	1	4	0	5	5
MAC (Acc + A*B)	2	3	5	11	11
ROR (Acc rotated by 1)	3	3	11	81	81
LTH-T (Acc = 0xFF if A<B else 0)	3	2	81	0	0
LTH-F (Acc = 0xFF if A<B else 0)	2	3	0	ff	ff

Table 1 - Test outputs

The testbench code used is attached below in appendix A

Appendix A

```
module tb_alu2;
//Inputs
 reg clk;
 reg[7:0] A,B;
 reg[3:0] ALU_Sel;

//Outputs
  reg[7:0] ALU_out;


 // Verilog code for ALU
  integer i;
  reg[7:0] expected;
 ALU test_unit(
   .clk(clk),
   .A(A),.B(B),  // ALU 8-bit Inputs
   .ALU_Sel(ALU_Sel),// ALU Selection
   .ALU_out(ALU_out) // ALU 8-bit Output
  );

  initial begin
    $dumpfile("dump.vcd"); $dumpvars;
    $display("A         B         ALU_Sel  ALU_Out");
    $monitor("%b  %b  %b     %b",A,B,ALU_Sel, ALU_out);


    // ADD
    A = 8'b0001;
    B = 8'b0100;
    ALU_Sel = 4'b0000;
    clk=1'b1;
    #5;
    expected = A + B;
    clk=1'b0;
    #5;

    // MAC
    A = 8'b0010;
    B = 8'b0011;
    ALU_Sel = 4'b0110;
    clk=1'b1;
    #5;
    expected = 8'b0101 + (A * B);
    clk=1'b0;
    #5;

    // ROR
    A = 8'b0011;
    ALU_Sel = 4'b1000;
    clk=1'b1;
    #5;
    expected = 8'b10000001;
    clk=1'b0;
    #5;

    // LTH - T
    A = 8'b0011;
    B = 8'b0010;
    ALU_Sel = 4'b1111;
    clk=1'b1;
```

```
    #5;
    expected = 8'h0;
    clk=1'b0;
    #5;

    // LTH - F
    B = 8'b0011;
    A = 8'b0010;
    ALU_Sel = 4'b1111;
    clk=1'b1;
    #5;
    expected = 8'hFF;
    clk=1'b0;
    #5;


  end

endmodule
```