



# FIR Filter

Verilog Hardware Design







### Design Flow





Getting Started with FIR Filter Concept



System Modeling Using MATLAB



FIR Filter Architecture (Block Diagram)



Hardware Design Using Verilog



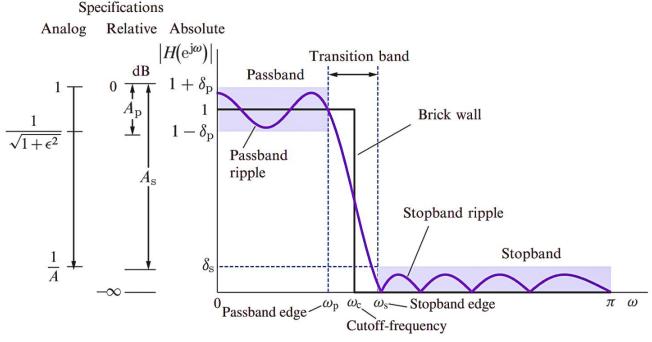
Testbench and Simulation Using Vivado



.WAV File Filtering Using Simulink

## What is FIR Filter?

Finite Impulse Response (FIR) Filter is a digital LTI system with an impulse response that settles to a zero value over a certain period of time, thus making it finite. It passes a set of desired frequency components from a mixture of desired and undesired components.



Example of tolerance diagram for a lowpass filter - Applied digital signal processing - Dimitris G. Manolakis, Vinay K. Ingle.

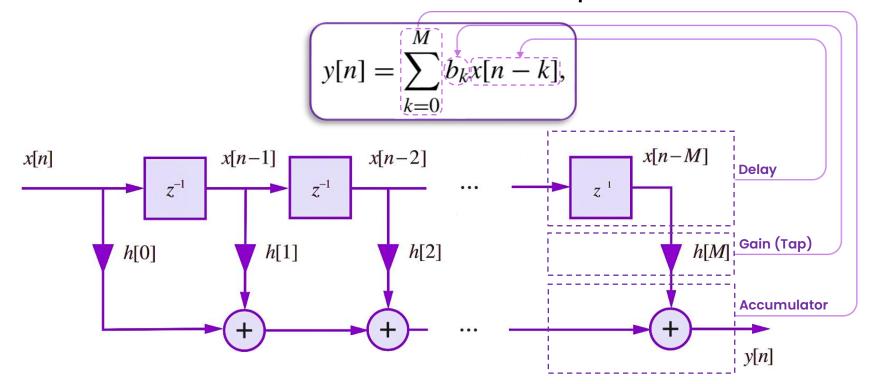
FIR Filter is featured by phase linearity and stability which make it suitable for systems that rely on the shape characteristics of a signal such as IoT devices and VUI systems where the shape of a voice signal should be preserved, and Neuron and cell monitoring devices. However, it requires higher order (more hardware) compared to IIR.

## What is FIR Filter?

We can generally describe discrete-time LTI systems through Linear Constant-Coefficient Difference Equation (LCCDE):

$$y[n] = -\sum_{k=1}^{N} a_k y[n-k] + \sum_{k=0}^{M} b_k x[n-k]$$
Feedback Feedforward Constant Coefficients

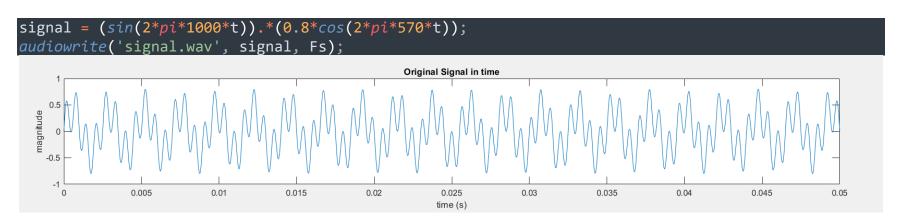
Since the feedback causes the impulse response depends on old outputs and consequentially its non-zero samples extend to infinity such as Infinite Impulse Response (IIR) Filters, FIR Filters have no feedback constant coefficient and can be expressed as follows:

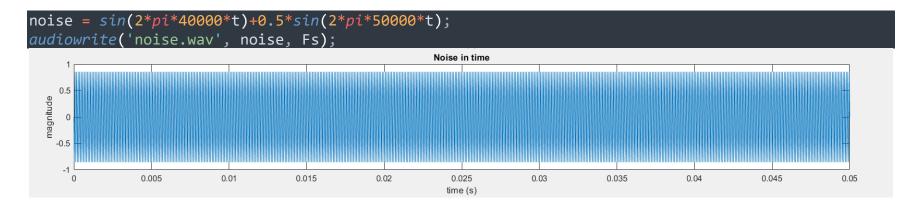


To determine our design requirements and filter specifications, let's assume we are dealing with audio signal from .wav file which has sampling rate 44.1 KHz.

Creating a simple multi-frequency signal with 570 Hz and 1KHz and another signal that represents noise with high frequencies +40KHz.

```
Fs=44100;
t = 0:1/50000:0.05;
```

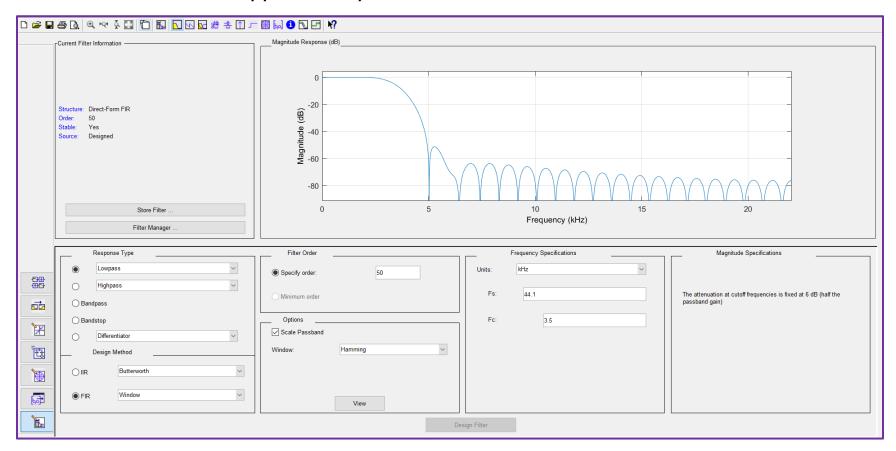




Now we can design our filter based on the previous ranges of frequencies using Filter Designer tool by the following command:

#### >> filterDesigner

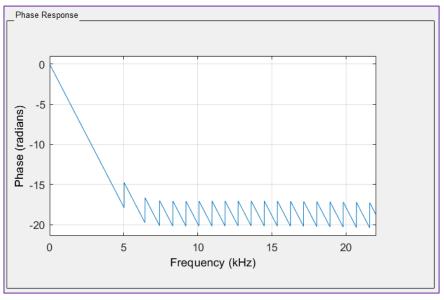
Note: This command is supported only in MATLAB newer versions than 2018 instead of fdatool

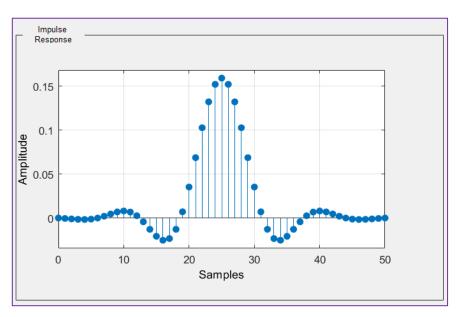


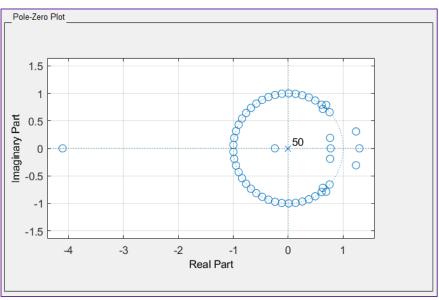
I designed a 50<sup>th</sup> order low-pass FIR filter with Hamming window for better side lobes reduction and 3.5KHz Cutoff Frequency which is suitable for filtering our IKHz from the applied +40KHz noise.

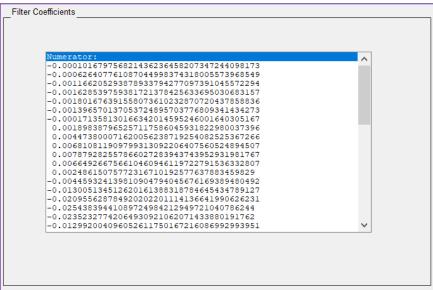


### From the toolbar, We can represent our filter from different aspects:







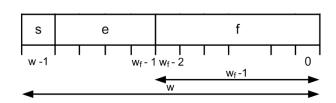


Now, the most critical step is to represent the Filter Coefficients shown above in our design.



### Getting our 51 coefficients From File>Export>Coefficient File (ASCII)

```
% Generated by MATLAB(R) 9.8 and Signal Processing Toolbox 8.4.
   % Generated on: 08-Feb-2023 03:24:28
   % Coefficient Format: Decimal
 5
   % Discrete-Time FIR Filter (real)
   % Filter Structure : Direct-Form FIR
   % Filter Length : 51
   % Stable : Yes
   % Linear Phase
                     : Yes (Type 1)
12
13
14 Numerator:
   -0.000101679756821436236458207347244098173
  -0.000626407761087044998374318005573968549
   -0.001166205293878933794277097391045572294
   -0.001628539759381721378425633695030683157
   -0.001801676391558073610232870720437858836
   -0.001396570137053724895703776809341434273
   -0.000171358130166342014595246001640305167
```



To represent floating number in binary we reserve the MSB as a sign bit, some bits for integer value (exponent), and other bits for the fraction (mantissa). So, let the tap (coefficient register) size is 16-bit including 1 bit for the sign, 0 bit for integer (all coefficients are less than 1) and the rest 15 bits represents the floating part.

```
To represent 15-bit fraction, multiply Coefficient * 2^15
if +ve --> round the result off
if -ve --> round the result off --> get 2's complement (1 + ~(rounded off result))
-0.0001016 --> 1111 1111 1111 1101
-0.0006264 --> 1111 1111 1110 1011
-0.0011662 --> 1111 1111 1101 1010
-0.0016285 --> 1111 1111 1100 1011
-0.0018016 --> 1111 1111 1100 0101
-0.0013965 --> 1111 1111 1101 0010
-0.0001713 --> 1111 1111 1111 1010

0.0018983 --> 0000 0000 0011 1110

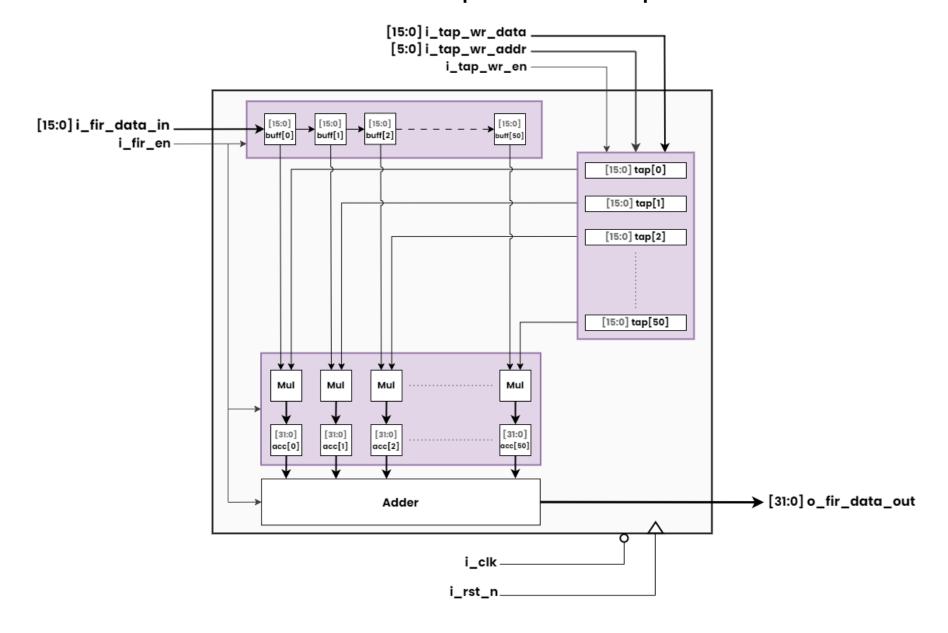
and so on ...
```

From the block diagram stated before, our main building blocks is:

Buffers act as a shift register that propagates each 16-bit sample.

**Taps** hold the *16-bit* filter coefficients (I treated it as a configurable RAM)

**Accumulators** hold the 16-bit samples × 16-bit taps *32-bit* results.



```
module fir filter
    #( parameter ORDER
                                = 50,
       parameter DATA IN WIDTH = 16,
       parameter DATA OUT WIDTH = 32,
       parameter TAP DATA WIDTH = 16,
       parameter TAP ADDR WIDTH = 6 )
                    signed [DATA IN WIDTH-1 : 0] i fir data in
        input wire
                                                   i fir en
        input wire
                                                   i tap wr en
        input wire
                           [TAP ADDR WIDTH-1 : 0] i tap wr addr
                           [TAP_DATA_WIDTH-1 : 0] i_tap_wr_data
        input wire
        input wire
                                                   i clk
        input wire
                                                   i rst n
       output req signed [DATA OUT WIDTH-1:0] o fir data out
    );
//internal registers declaration as 2D-arrays for optimized hardware description
reg signed [TAP DATA WIDTH-1 : 0] tap[ORDER : 0] ;
reg signed [DATA IN WIDTH-1 : 0] buffer[ORDER : 0];
req signed [DATA OUT WIDTH-1 : 0] accumulator[ORDER : 0] ;
integer i ;
//51-taps block logic
always @(posedge i clk or negedge i rst n) begin
   if (!i rst n)
       begin
       //50th order fir coefficients
            tap[0] <= 16'b 1111 1111 1111 1101;
            tap[1] <= 16'b 1111 1111 1110 1011;
            tap[2] <= 16'b 1111 1111 1101 1010;
```

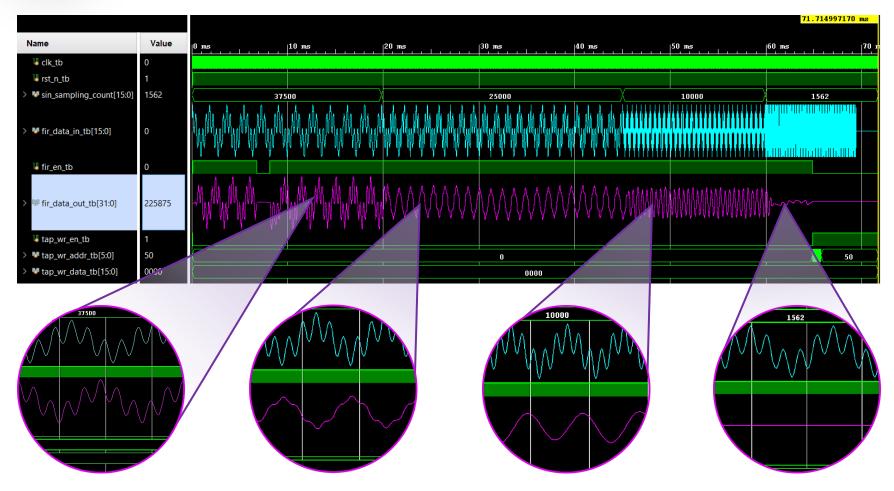
**Preview Full Code on GitHub** 

```
tap[49] <= 16'b 1111_1111_1110_1011 ;
            tap[50] <= 16'b 1111_1111_1111_1101;
        end
    else if(i_tap_wr_en && !i_fir_en) //preventing coeff change during the operation
        begin
            tap[i_tap_wr_addr] <= i_tap_wr_data ;
        end
end
//51-buffers block logic
always @(posedge i_clk or negedge i_rst_n) begin
    if (!i_rst_n)
        begin
            for (i=0; i \le ORDER; i=i+1)
                begin
                    buffer[i] <= 16'b0;
                end
        end
    else if (i_fir_en)
        begin
            buffer[0] <= i_fir_data_in ;</pre>
            for (i=0; i<ORDER; i=i+1)
                begin
                    buffer[i+1] <= buffer[i] ;</pre>
                end
        end
end
//51-accumulator block logic
always @(posedge i_clk or negedge i_rst_n) begin
    if (!i rst n)
            for (i=0; i<=ORDER; i=i+1)
```

**Preview Full Code on GitHub** 

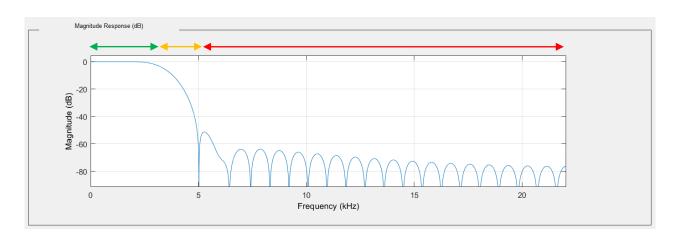
### RTL Verification

```
module fir filter tb();
    signed [15 : 0]
                      fir data in tb
reg
                       fir en tb
reg
                       tap wr en tb
reg
            [5 : 0]
                      tap wr addr tb
req
                       tap wr data tb
            [15:0]
reg
                       clk tb
req
                       rst n tb
reg
wire signed [31 : 0]
                      fir data out tb;
parameter CLK PERIOD = 22675.73696; //periodic time of 44.1KHz CLK
parameter SIN1 SAMP
                                    ; //sampling time for 550Hz + 3KHz
                      = 37500
                                                                           Sin Wave
parameter SIN2 SAMP
                                    ; //sampling time for 820Hz + 4.3KHz Sin Wave
                      = 25000
                                    ; //sampling time for 2.1KHz + 10.8KHz Sin Wave
parameter SIN3 SAMP
                      = 10000
                                    ; //sampling time for 13KHz + 70KHz
parameter SIN4 SAMP
                      = 1562
                                                                           Sin Wave
`include "fir filter tasks.v"
reg [15 : 0] sin sampling count;
integer i ;
//----DUT Instantiation
fir filter DUT (
    .i fir data in (fir data in tb)
                    (fir en tb)
    .i fir en
                    (tap wr en tb)
    .i tap wr en
    .i tap wr addr (tap wr addr tb)
    .i tap wr data (tap wr data tb)
    .i clk
                    (clk tb)
                    (rst n tb)
    .i rst n
    .o fir data out (fir data out tb)
```



550Hz: Passed 820Hz: Passed 2.1KHz: Passed 13KHz: Filtered

3KHz: Passed 4.3KHz: attenuated 10.8KHz: Filtered 70KHz: Filtered



# Simulink Testing

In the previous testbench, we covered several scenarios of filtering a multi-frequency signal in addition to testing control signals such as disabling *fir\_en* and resuming it again and finally writing new filter coefficients (clear all taps in our case).

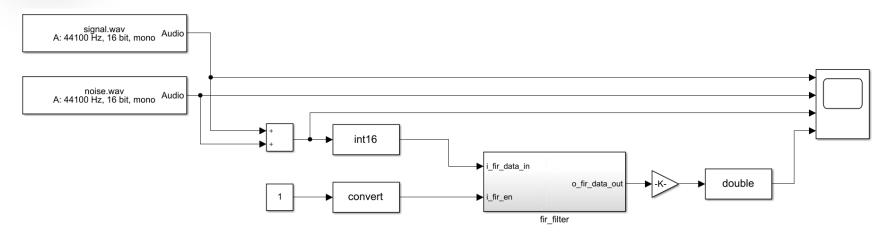
**But for more digging into practical applications,** we are going to import our verified RTL to Simulink and apply the more complex audio .wav files we created before and check the filter results.

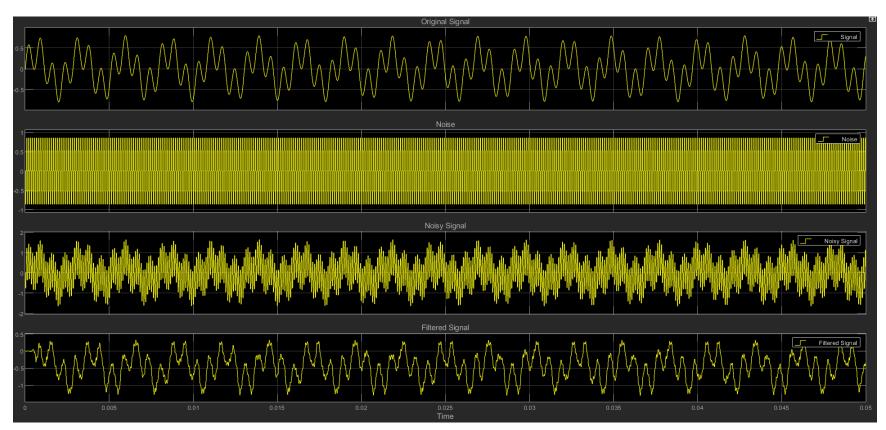
To import HDL code and generate Simulink model:

#### >> importhdl('fir\_filter.v')

Then, create your top Simulink model and get from Simulink Library Browser>DSP System Toolbox>Sources>From Multimedia File and import the .wav files and get other required blocks to construct our experiment system as shown in the following page.

# Simulink Testing





We can notice that the original signal is recovered successfully with an acceptable effect of noise in some values of the signal's amplitude.



### Thank You!

All code for this project can be found on my GitHub

