Computer Architecture
Computer Engineering Track
Tutorial 13

The Comparison of Memory Types: SRAM and DRAM

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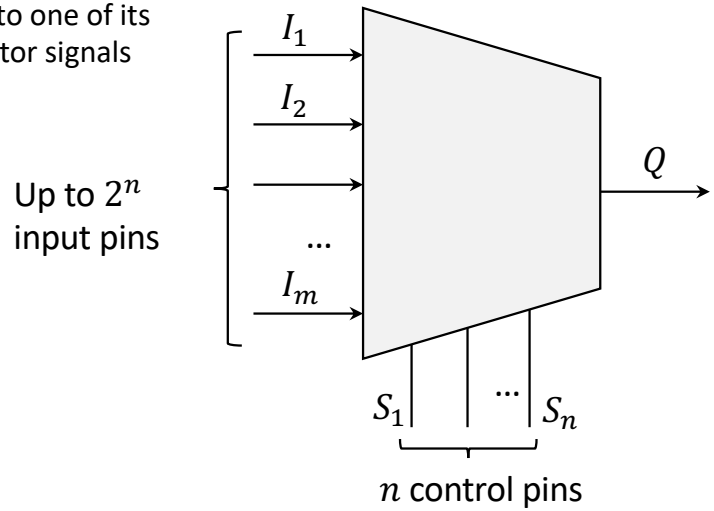
INNOPOLIS UNIVERSITY

Recap of Hardware Building Blocks

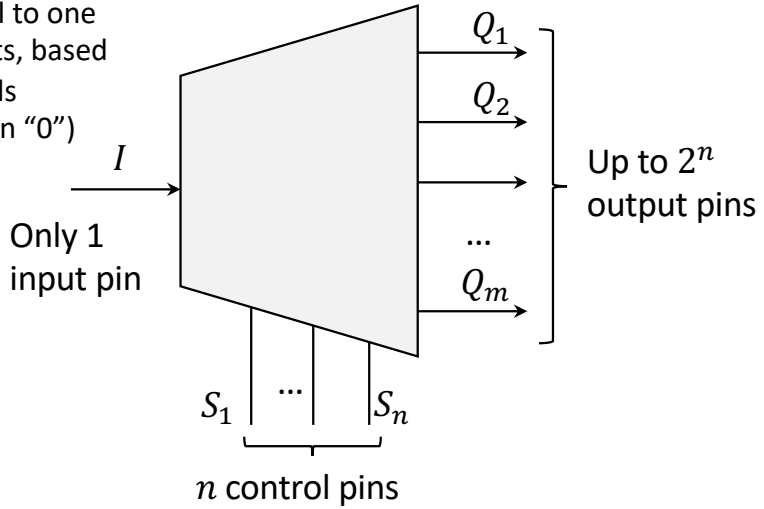
Multiplexor

Sets a specific output to one of its inputs, based on selector signals



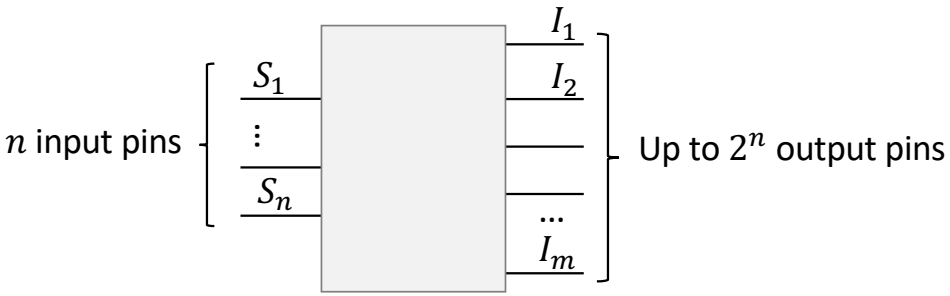
Demultiplexor

Forwards input signal to one of its multiple outputs, based on the selector signals (other outputs remain "0")



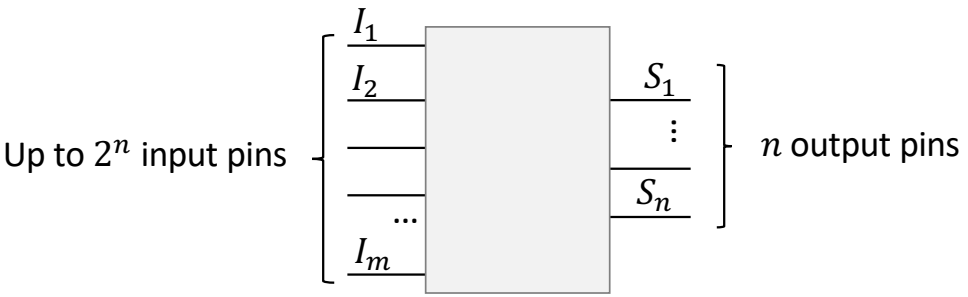
Decoder

Sets to "1" exactly one output pin, which corresponds to the signals of input pins; All other pins are set to "0"

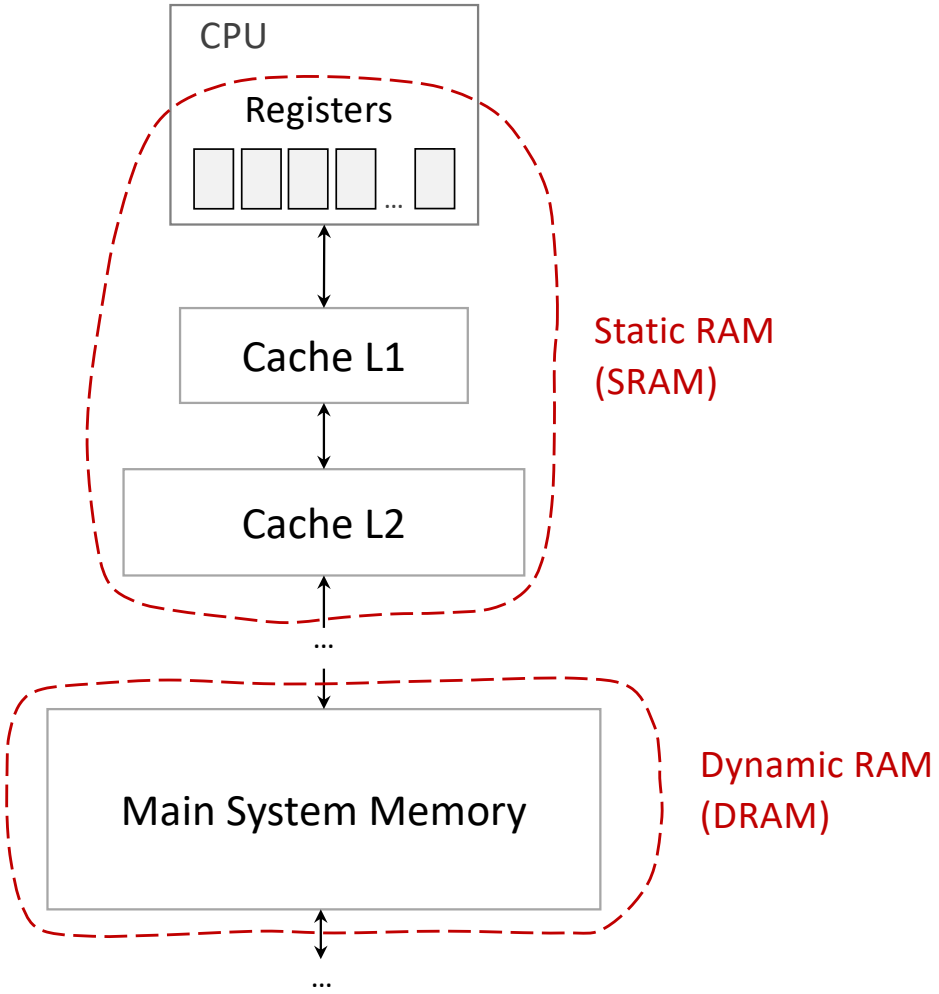


Encoder

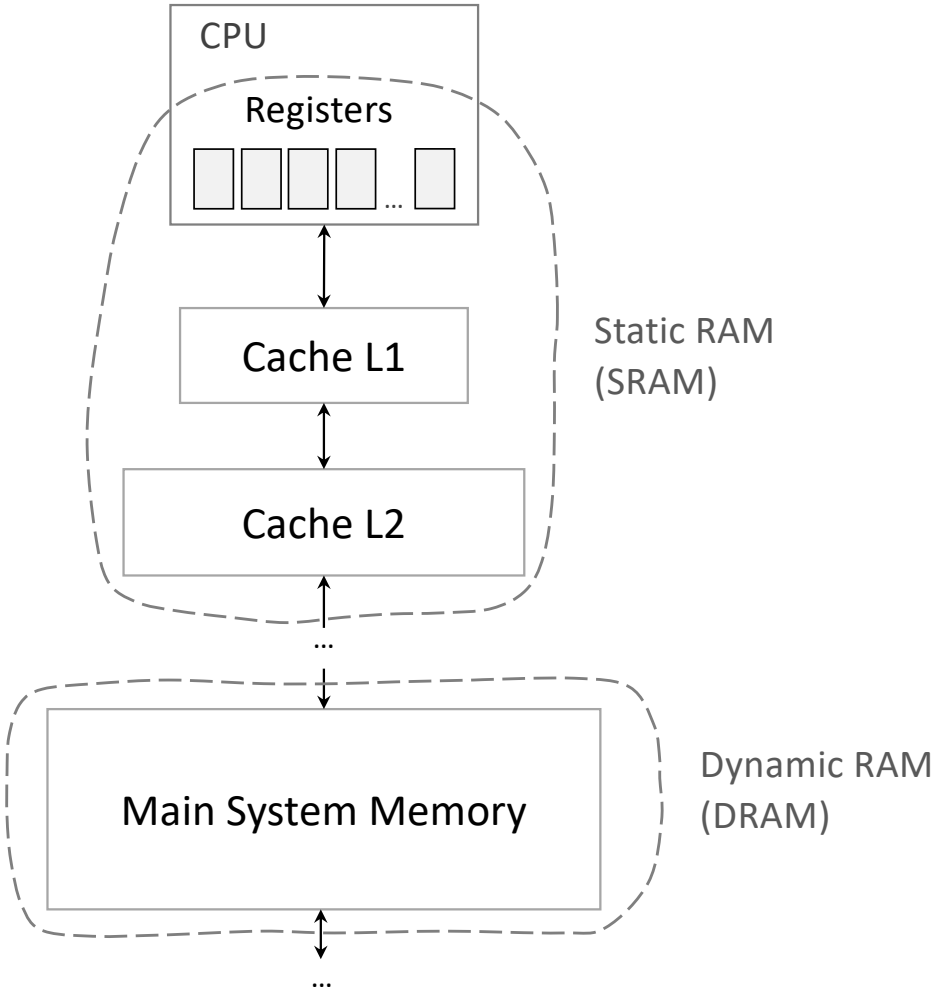
The opposite function of a decoder;
Only one input pin can be set to "1", while all others – "0"



Memory Hierarchy – the Fundamental Idea of Computer Architecture



The Comparison of DRAM and SRAM Memory Types



Characteristic	**SRAM**	**DRAM**
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
Storage Element	Flip-flop (Latch)	Capacitor
Usage	CPU cache, registers	System memory
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage	Not present	Significant
Chip Reliability	More reliable	Less reliable
Volatility	Both are volatile (require electrical power to keep data)	
Memory Cell Access	Each cell is accessed directly, unlike Sequential Access Memory (SAM)	

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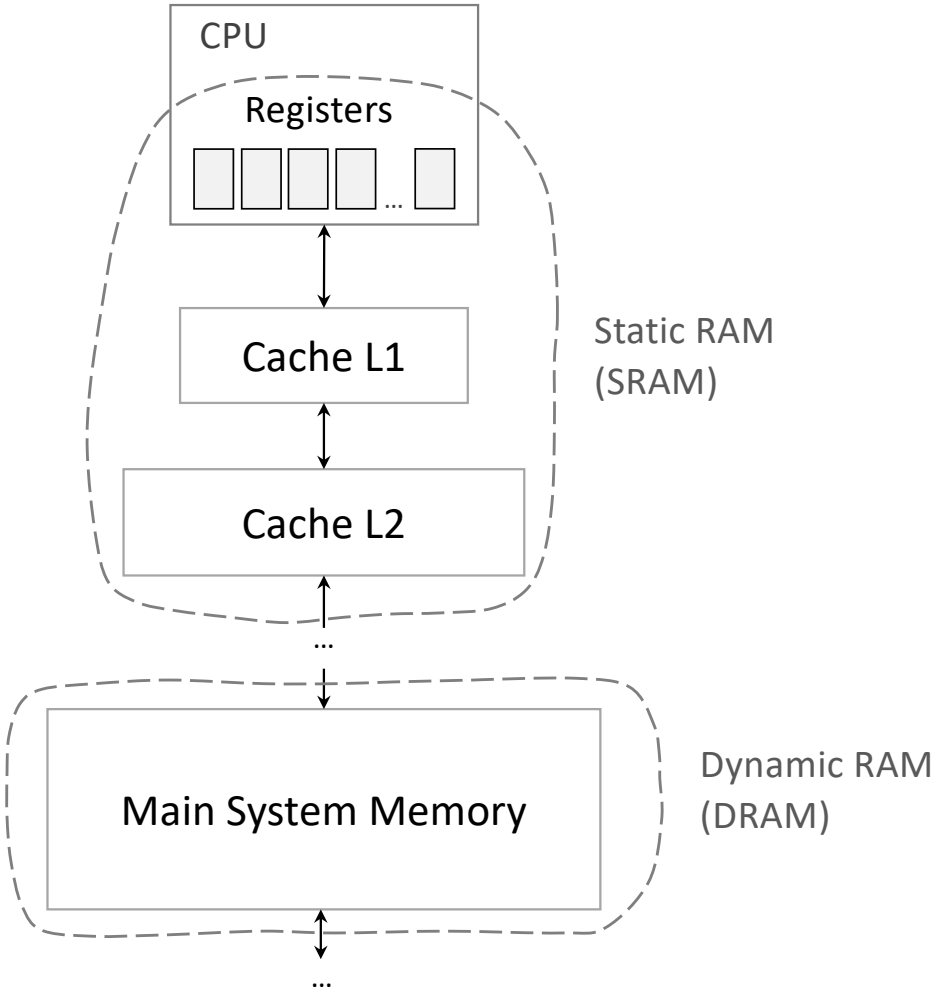

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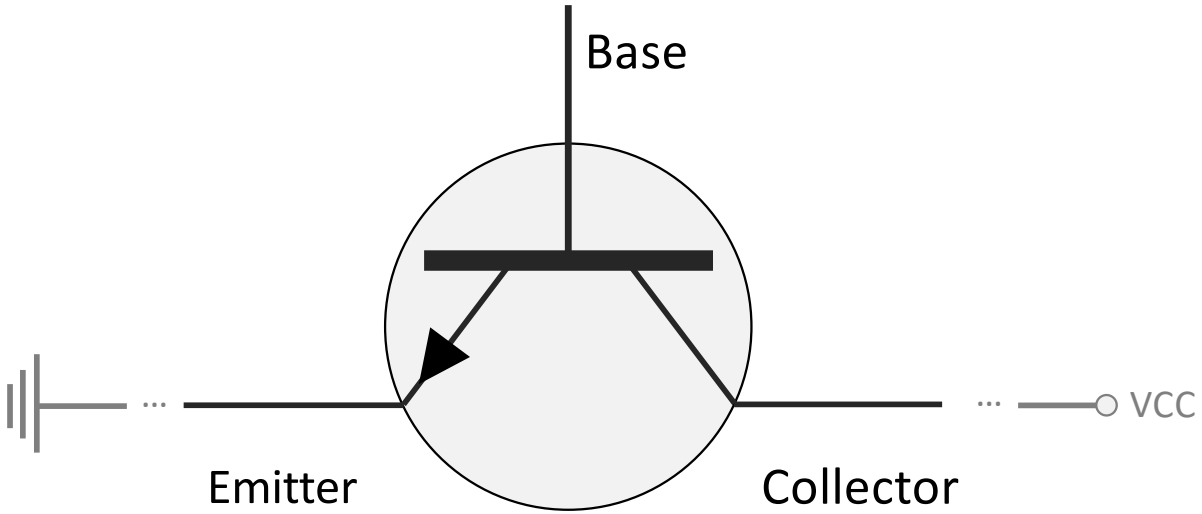
Transistor Recap

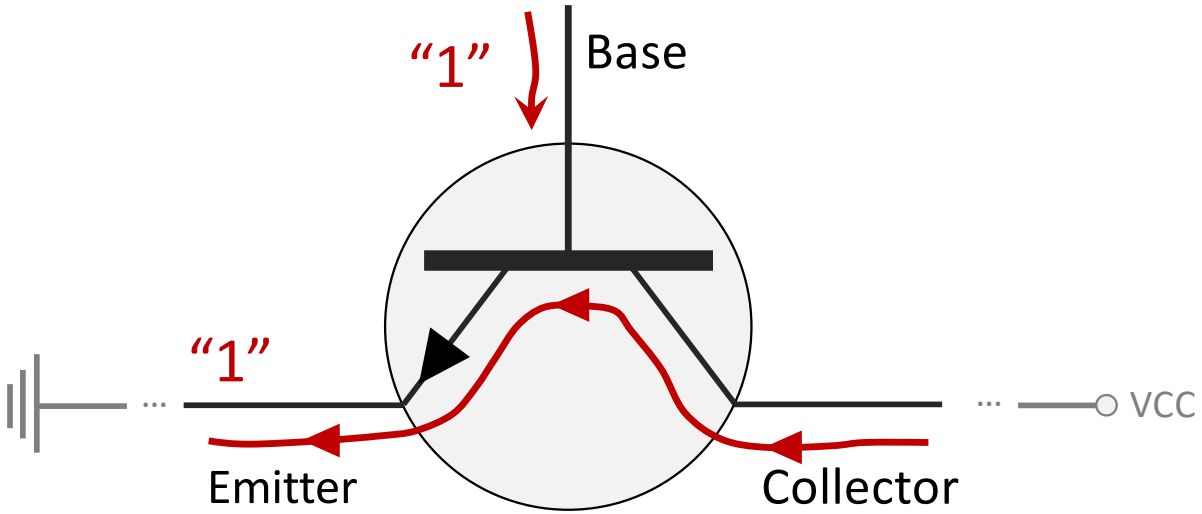


Transistor is a fast switch:

If there is voltage at the Base terminal (Base = “1”), then current flows between Emitter and Collector;

Otherwise (Base = “0”), there is no current

Transistor Recap



Note: Current direction depends on the transistor type (e.g. NPN or PNP)

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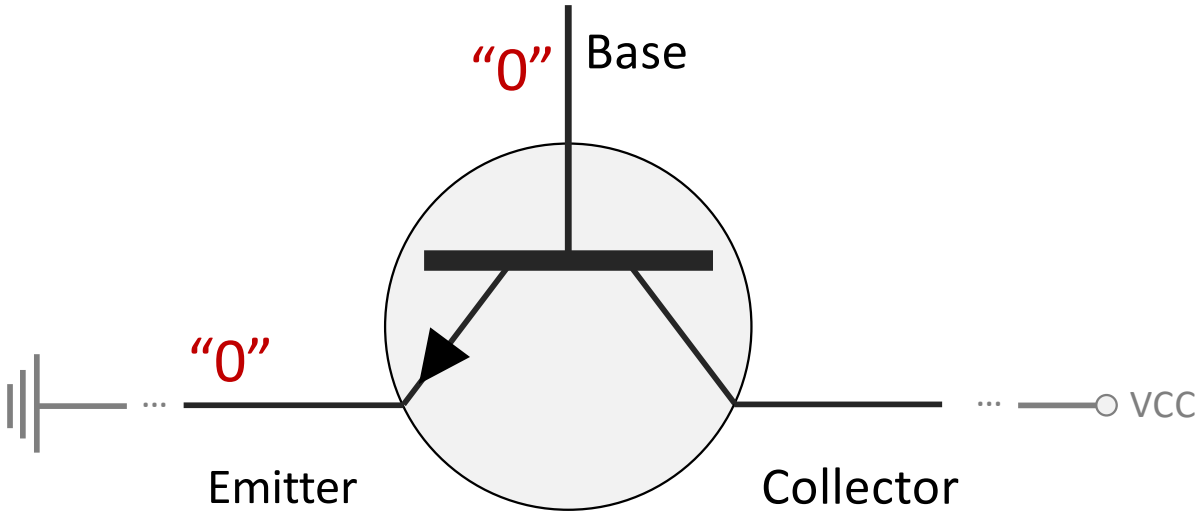

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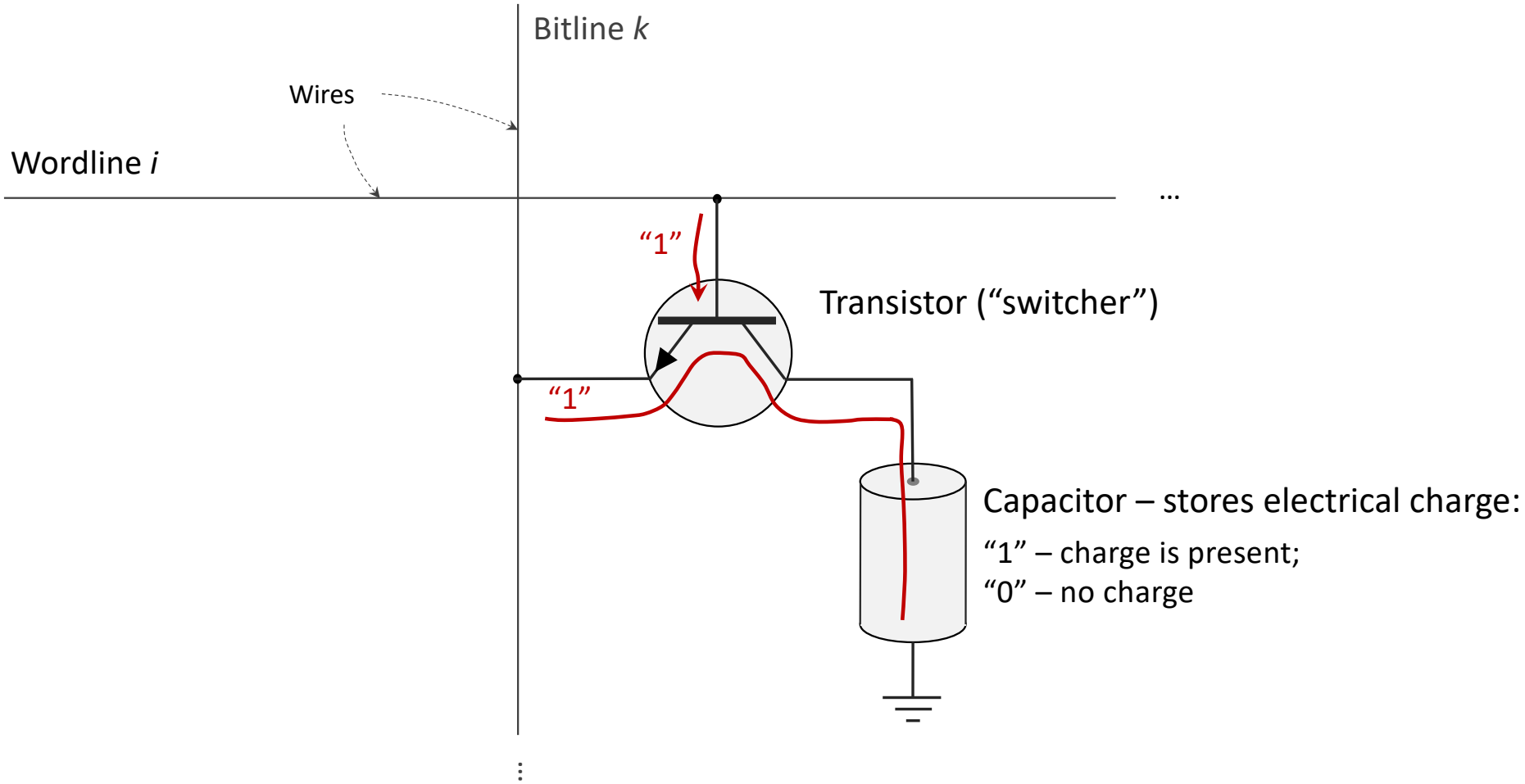
Capacitor: a physical device to store electrical charge

Image is taken from https://en.wikipedia.org/wiki/Capacitor

DRAM memory cell



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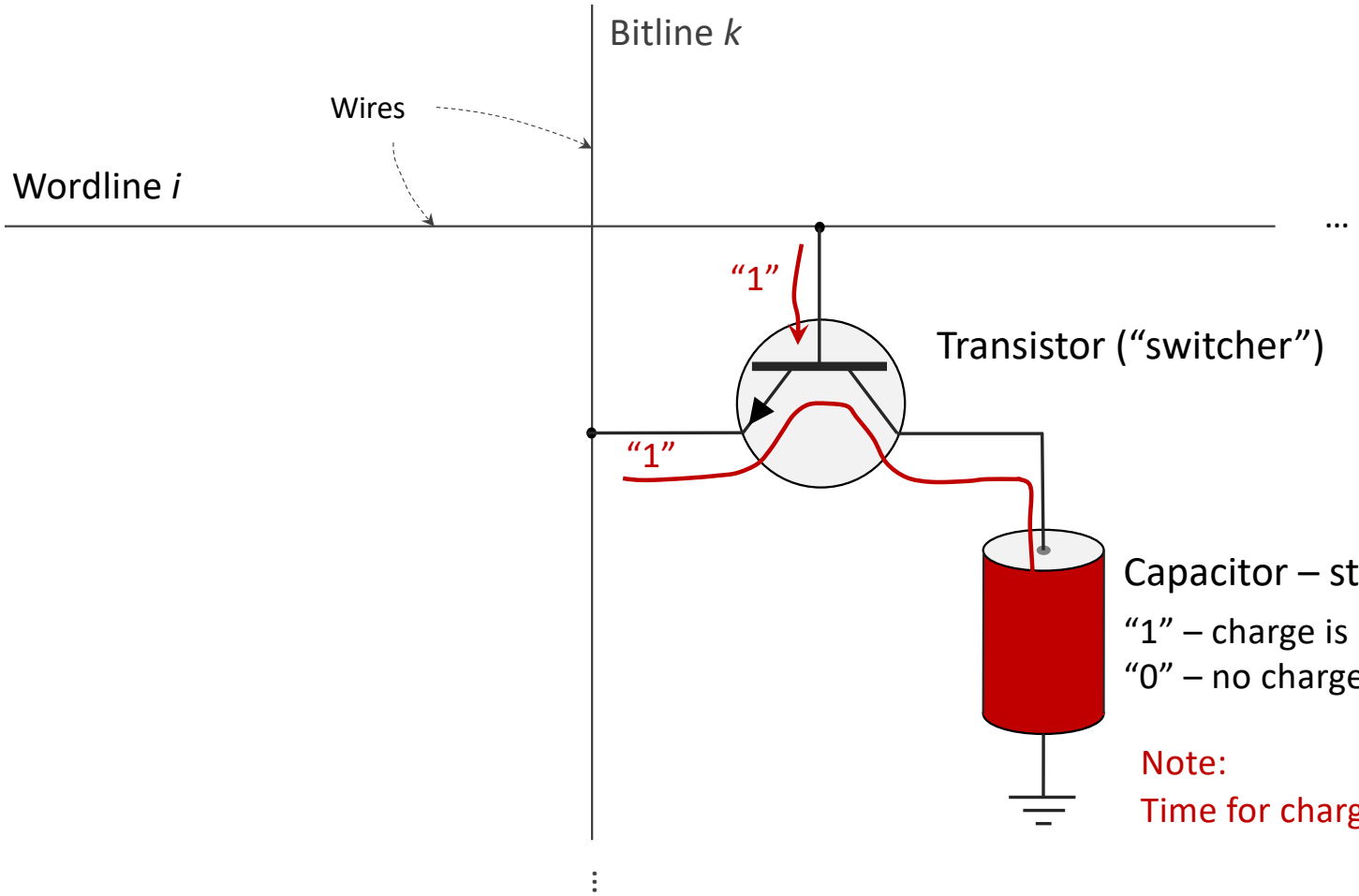

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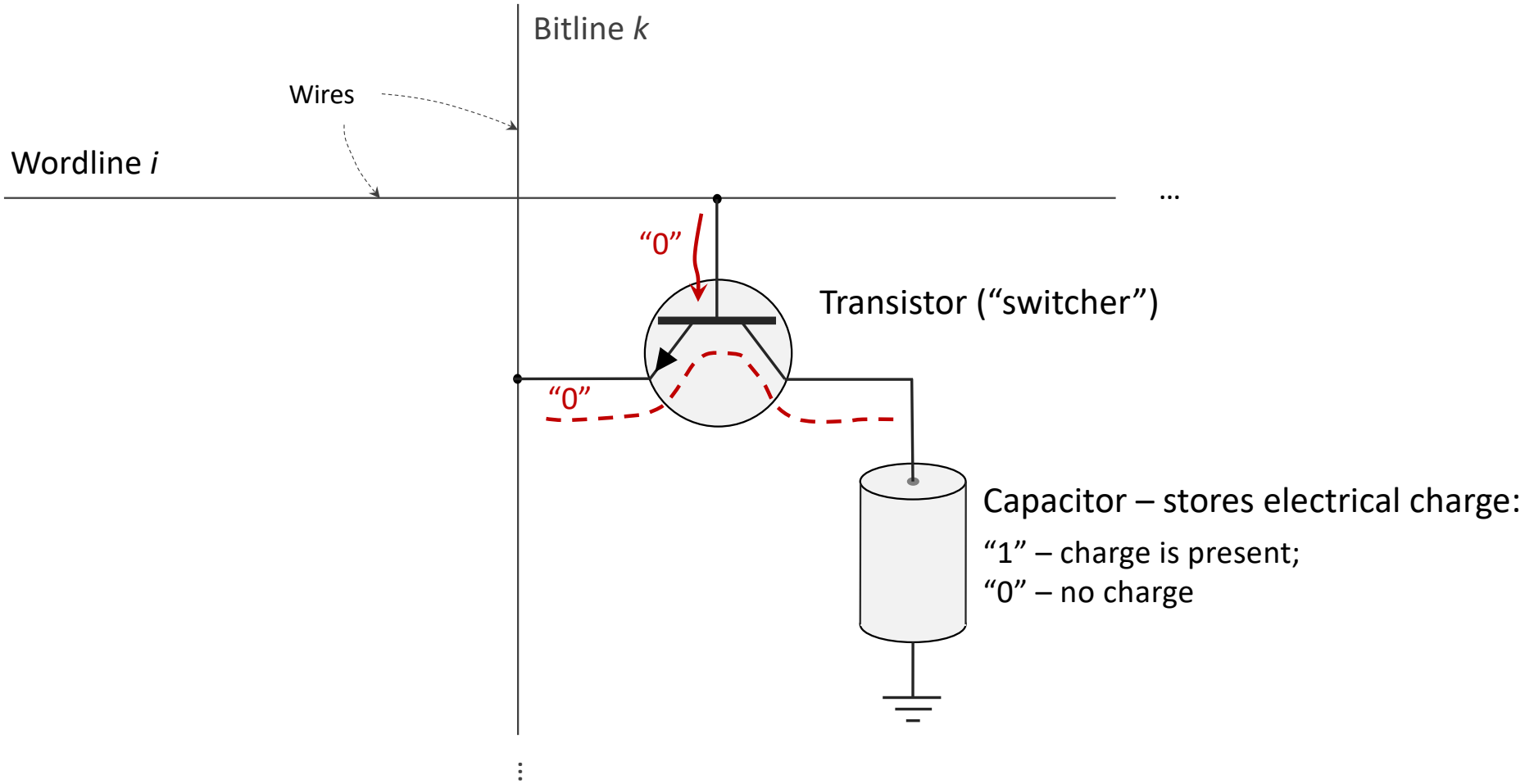

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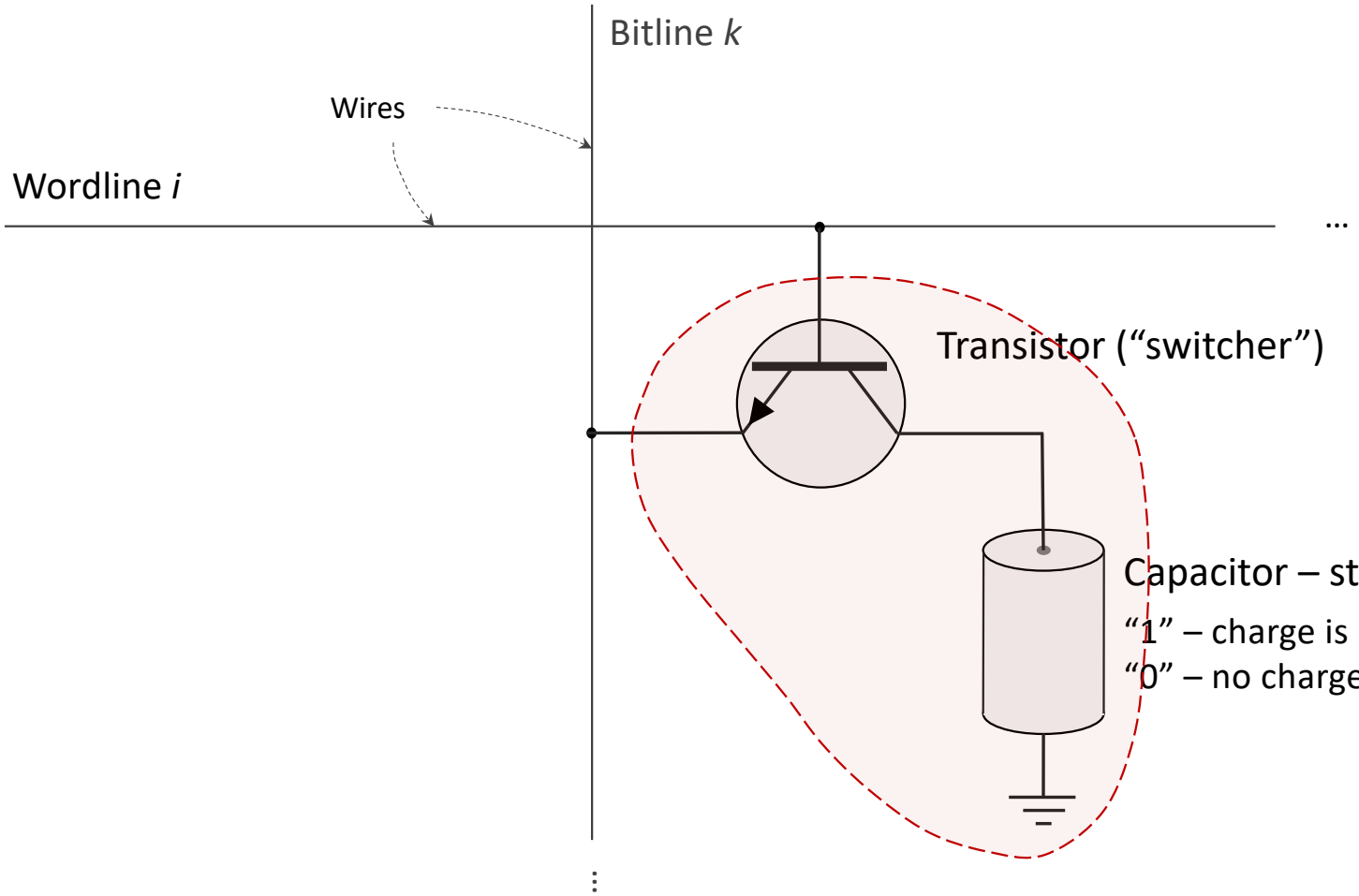
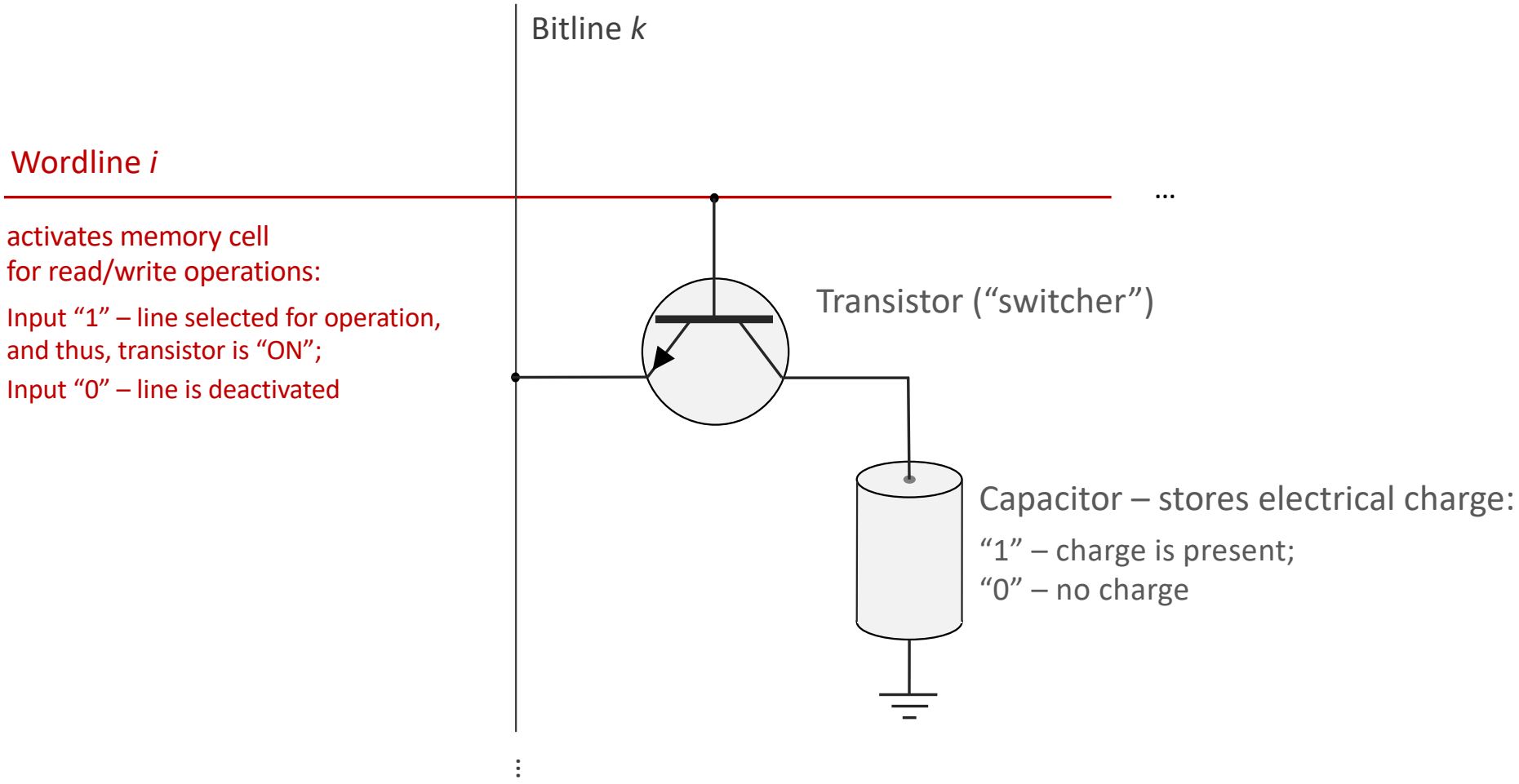


DRAM memory cell: capacitor + transistor

DRAM memory cell



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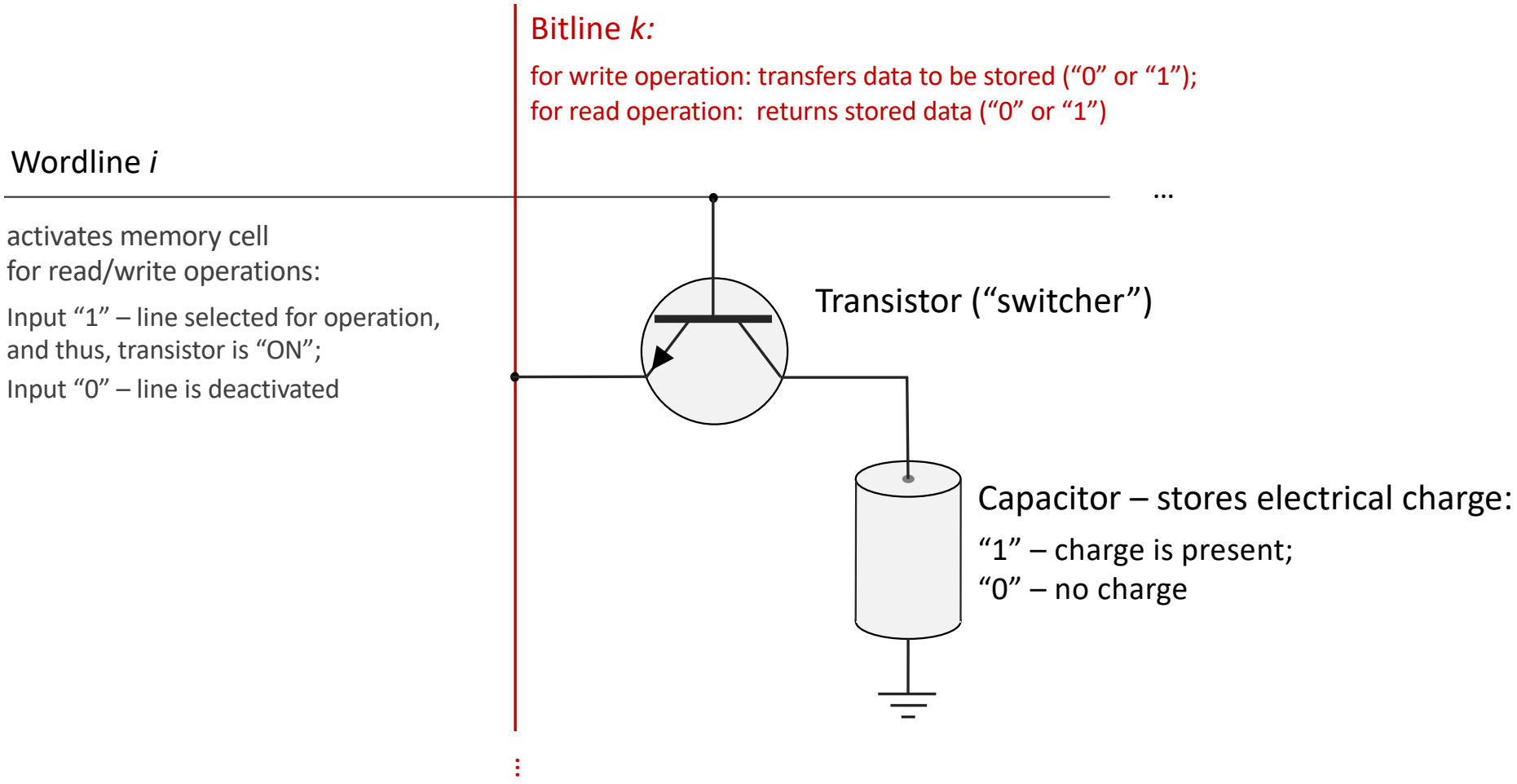
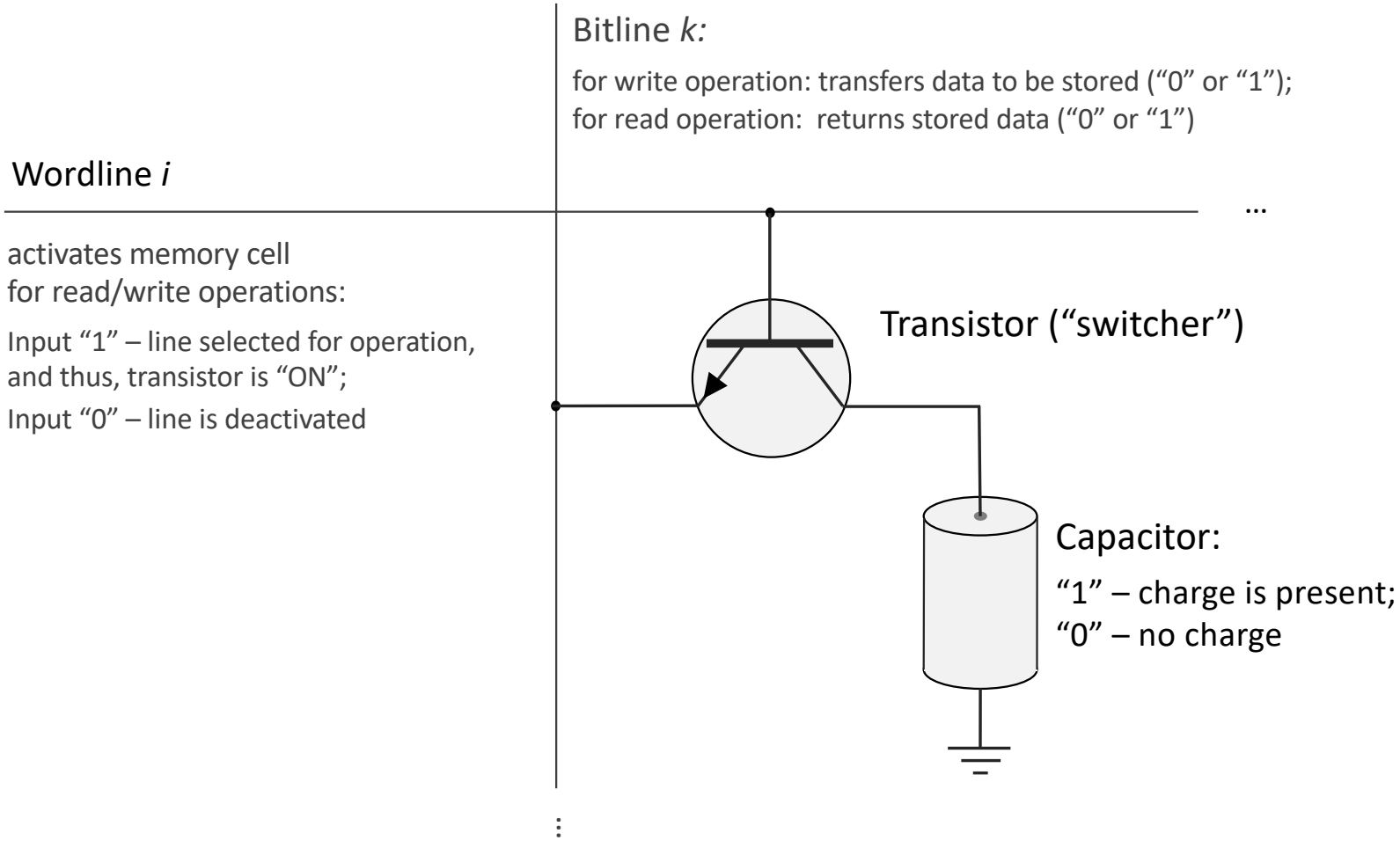
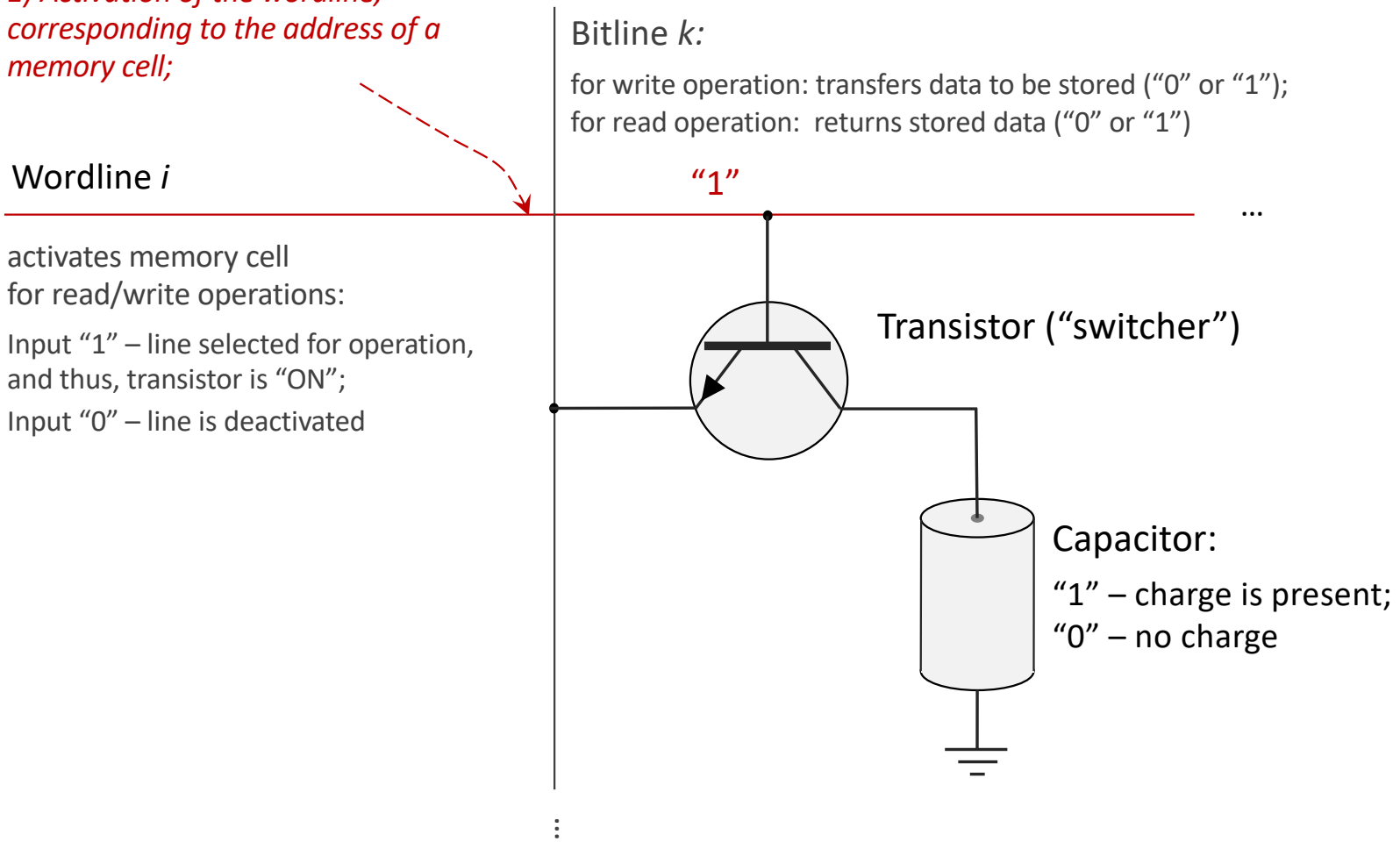


Writing into DRAM memory cell



Writing into DRAM memory cell

1) Activation of the wordline, corresponding to the address of a memory cell;



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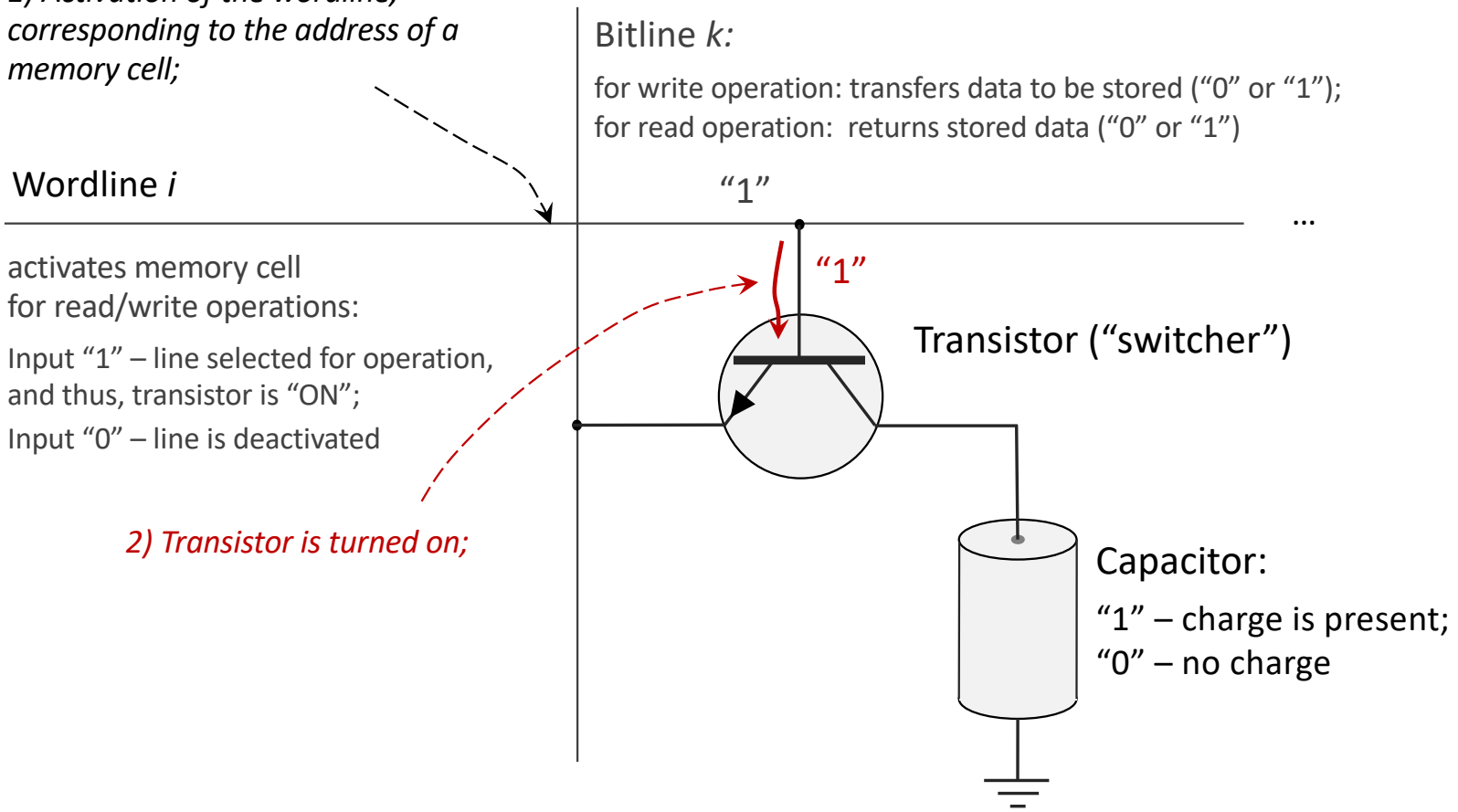

Writing into DRAM memory cell

1) Activation of the wordline, corresponding to the address of a memory cell;

Bitline *k:*

for write operation: transfers data to be stored (“0” or “1”);
for read operation: returns stored data (“0” or “1”)

Wordline *i*

“1”

…

activates memory cell
for read/write operations:

Input “1” – line selected for operation, and thus, transistor is “ON”;

Input “0” – line is deactivated

“1”

Transistor (“switcher”)

“1”

2) Transistor is turned on;

“1”

Capacitor:

“1” – charge is present;
“0” – no charge

3) Transfering data bit over the bitline, to be stored;

If “1” – capacitor gets charged (however, some time for charging is needed)

Writing into DRAM memory cell

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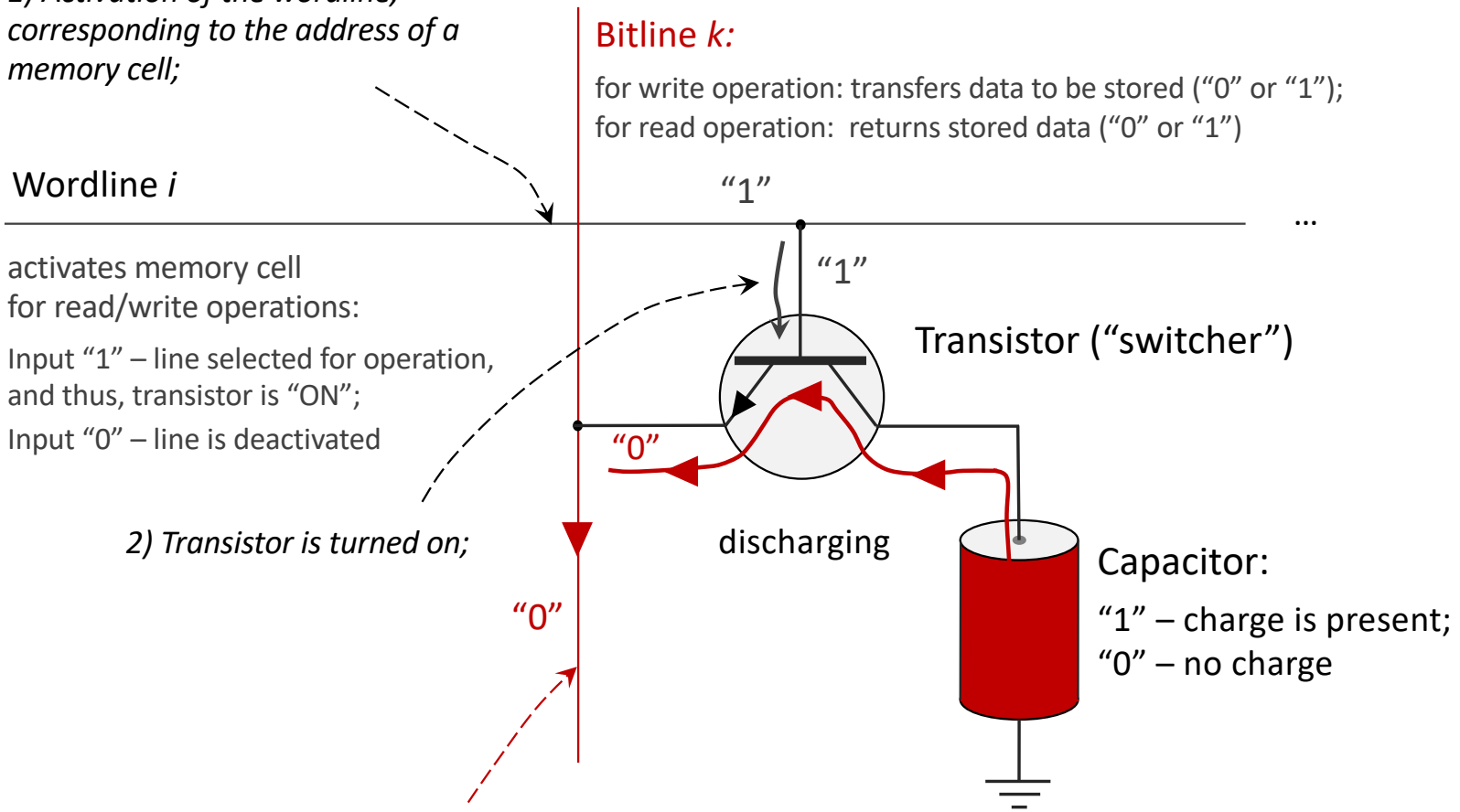

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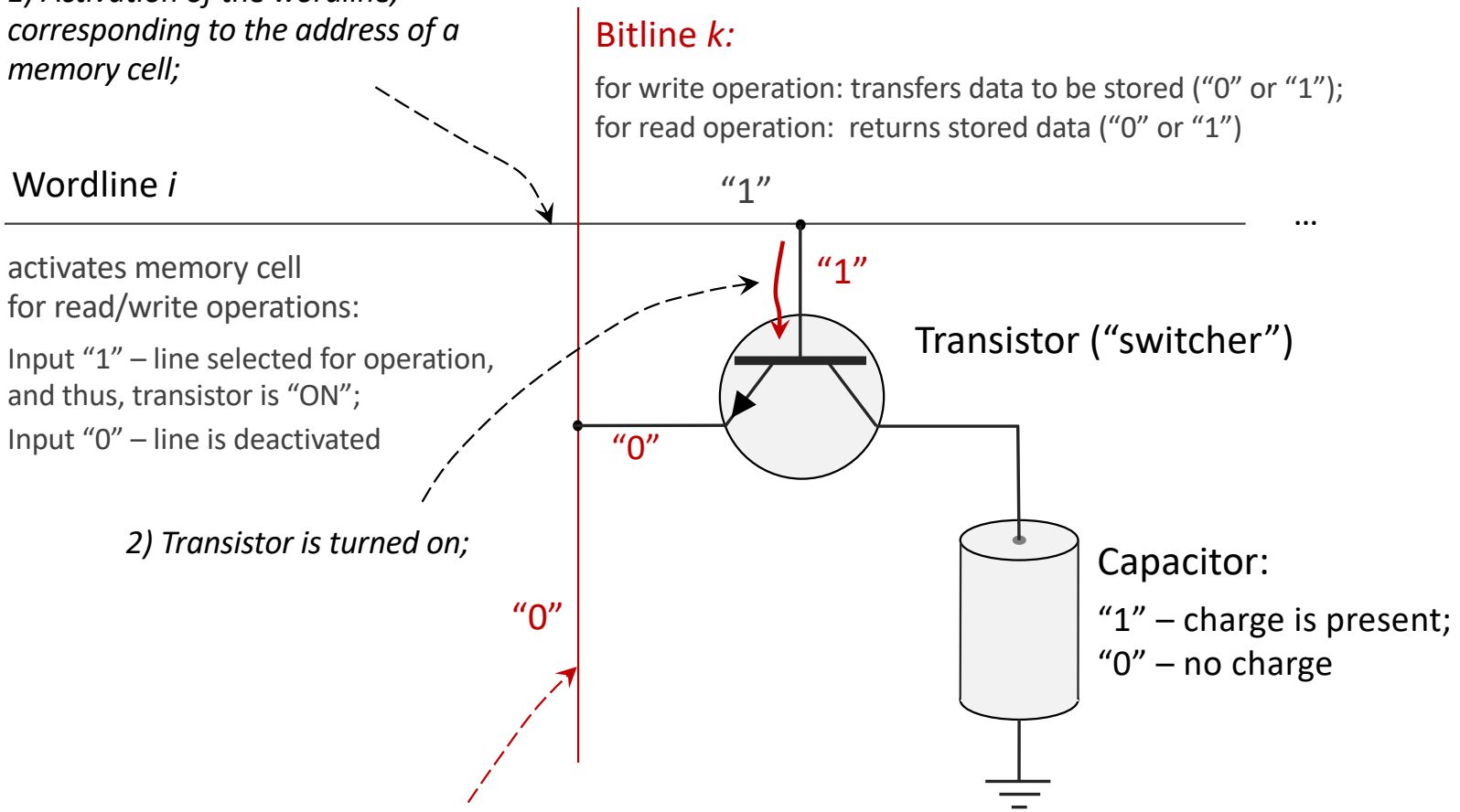

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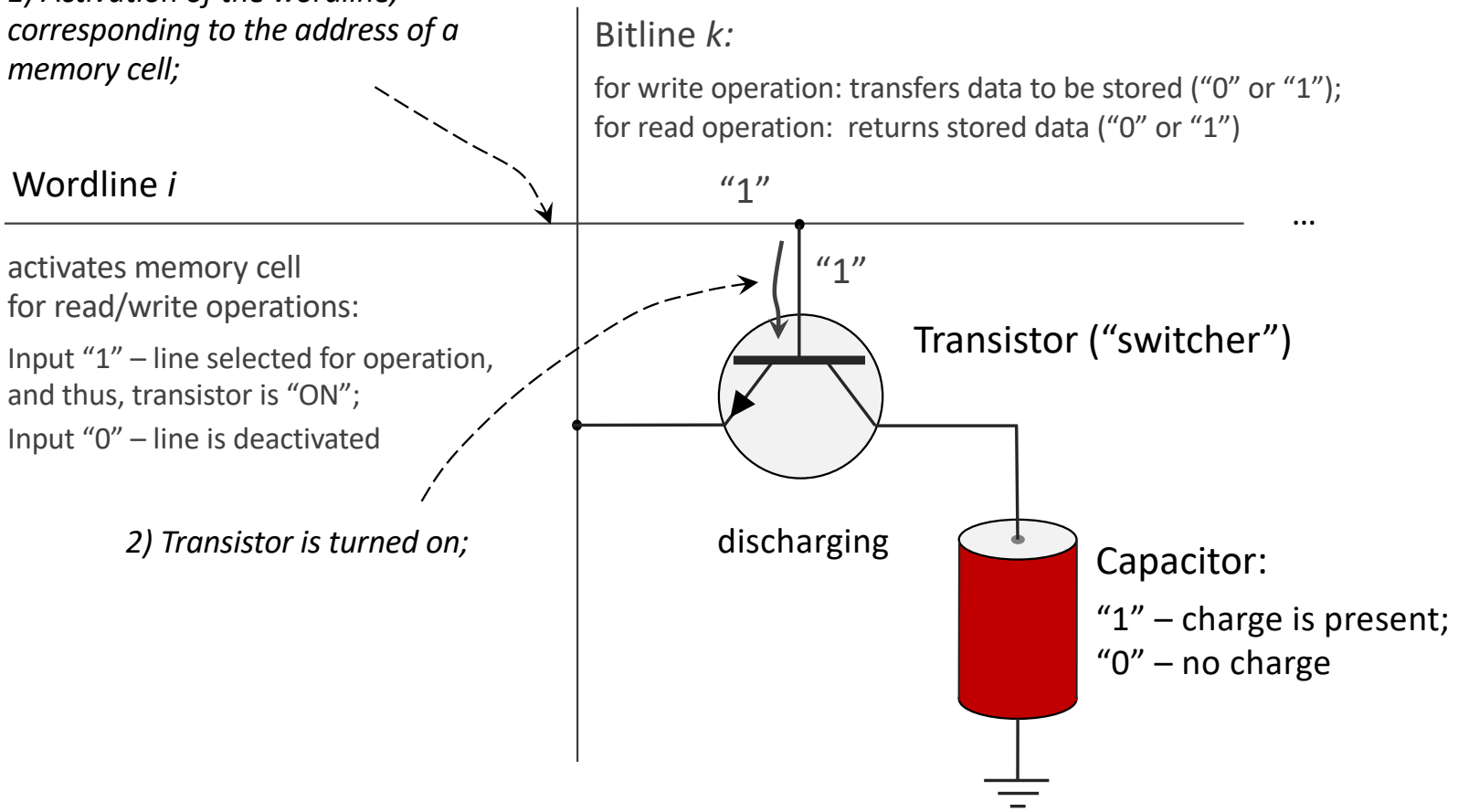

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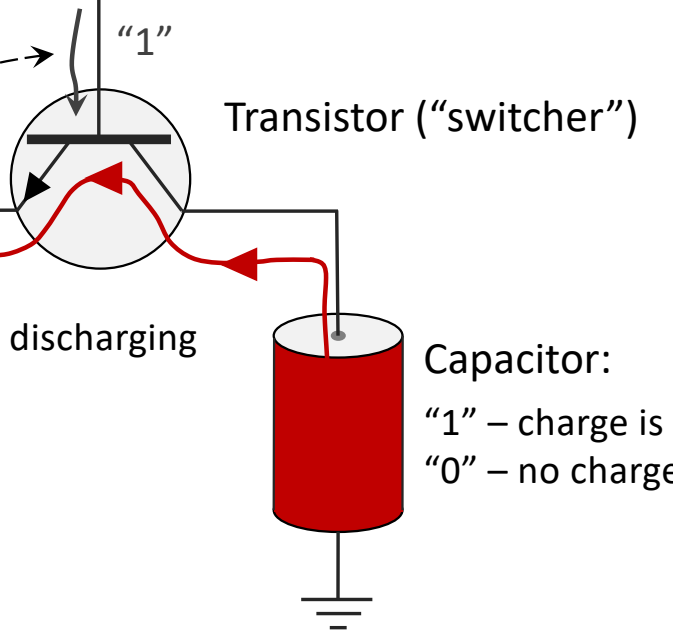
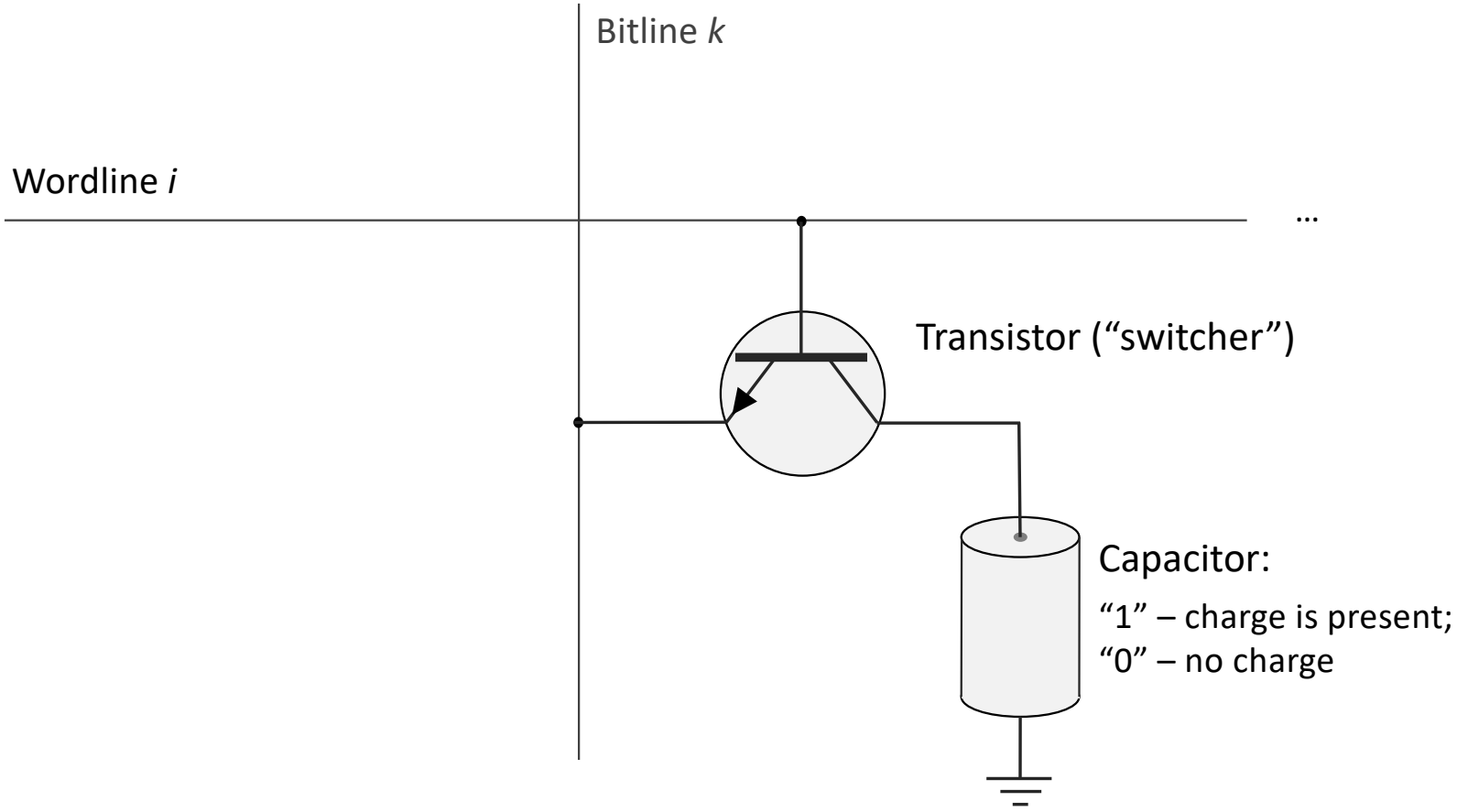


2) Transistor is turned on;

3) Transfering data bit from capacitor over the bitline

A More Compact Graphical Notation for Electrical Circuits



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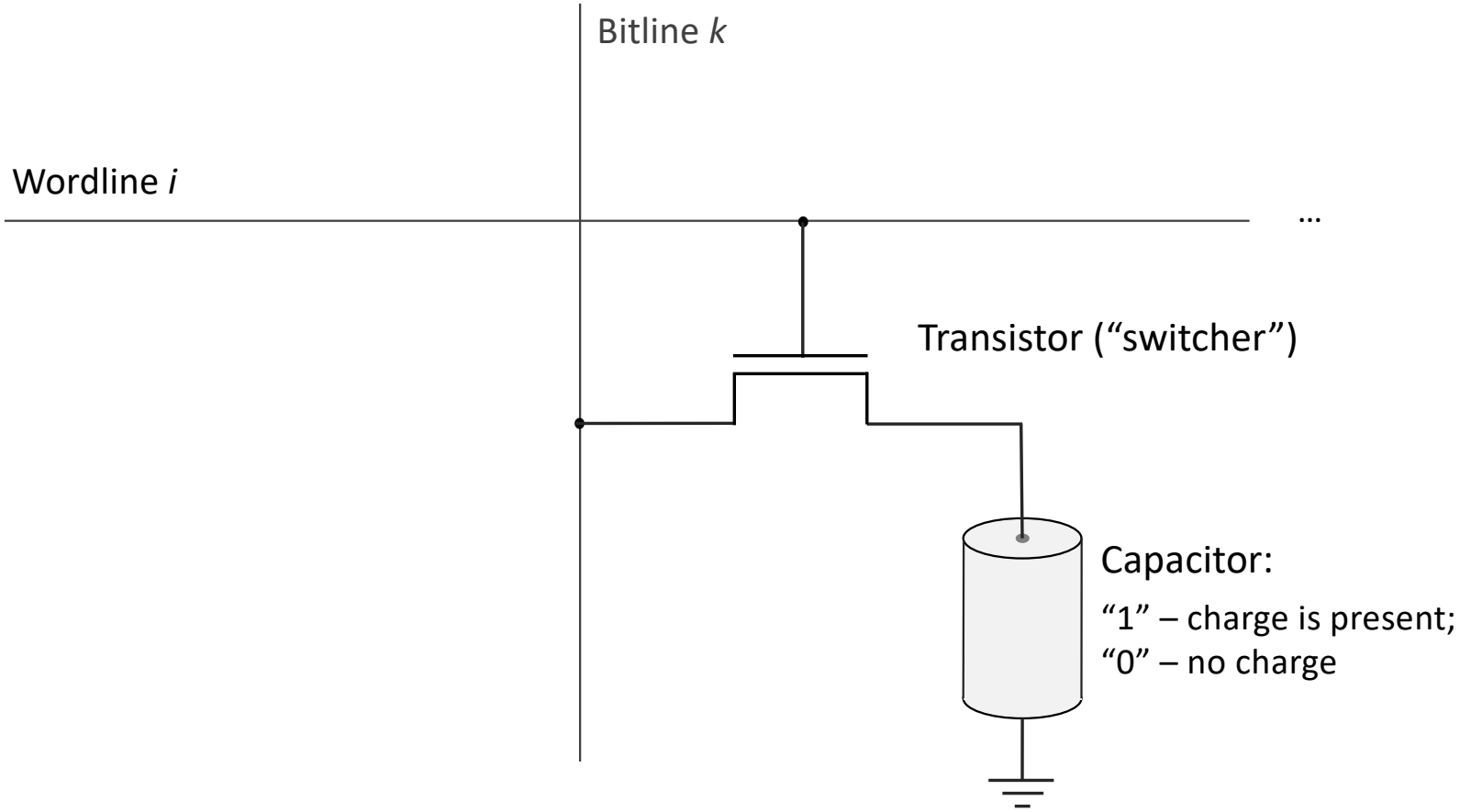

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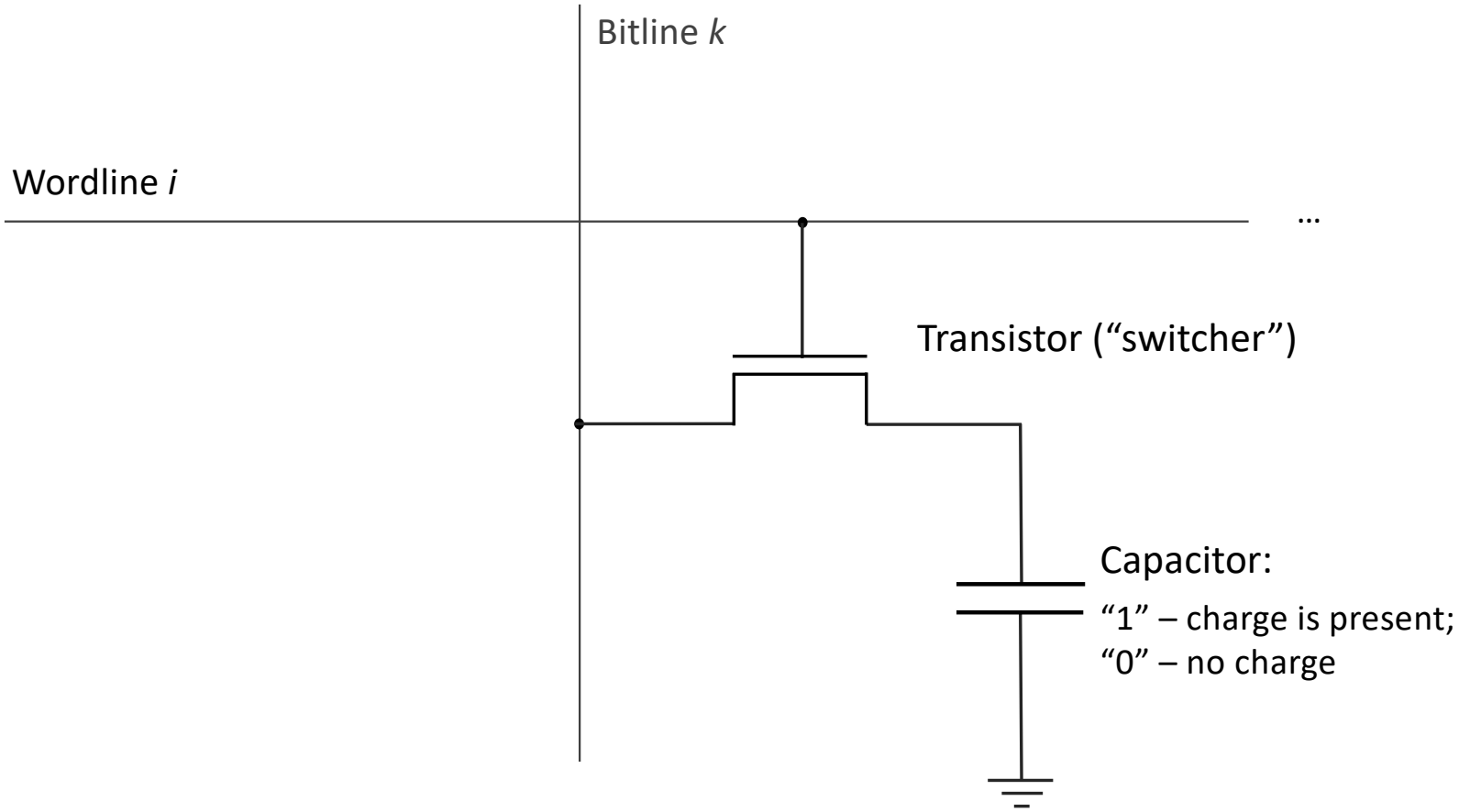
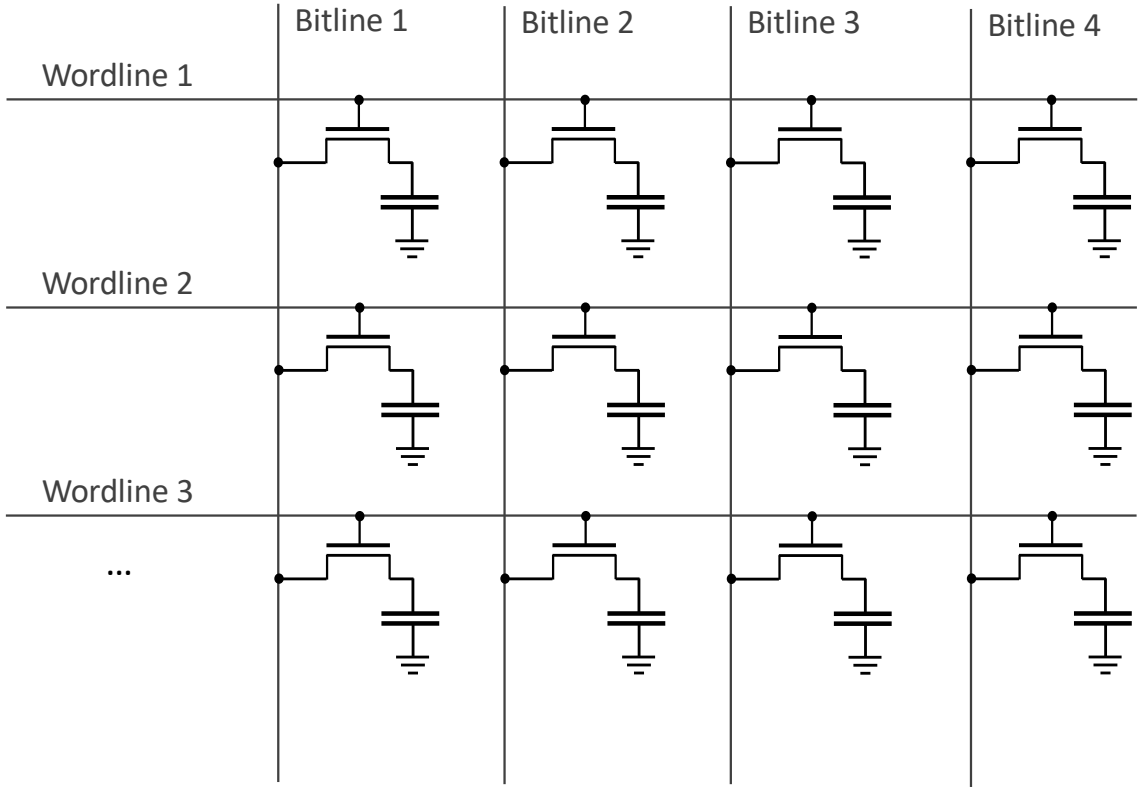


DRAM Memory: the Work Principle

DRAM memory – a set of memory cells
(each cell contains 1 bit of data)



DRAM Memory: the Work Principle

DRAM memory – a set of memory cells
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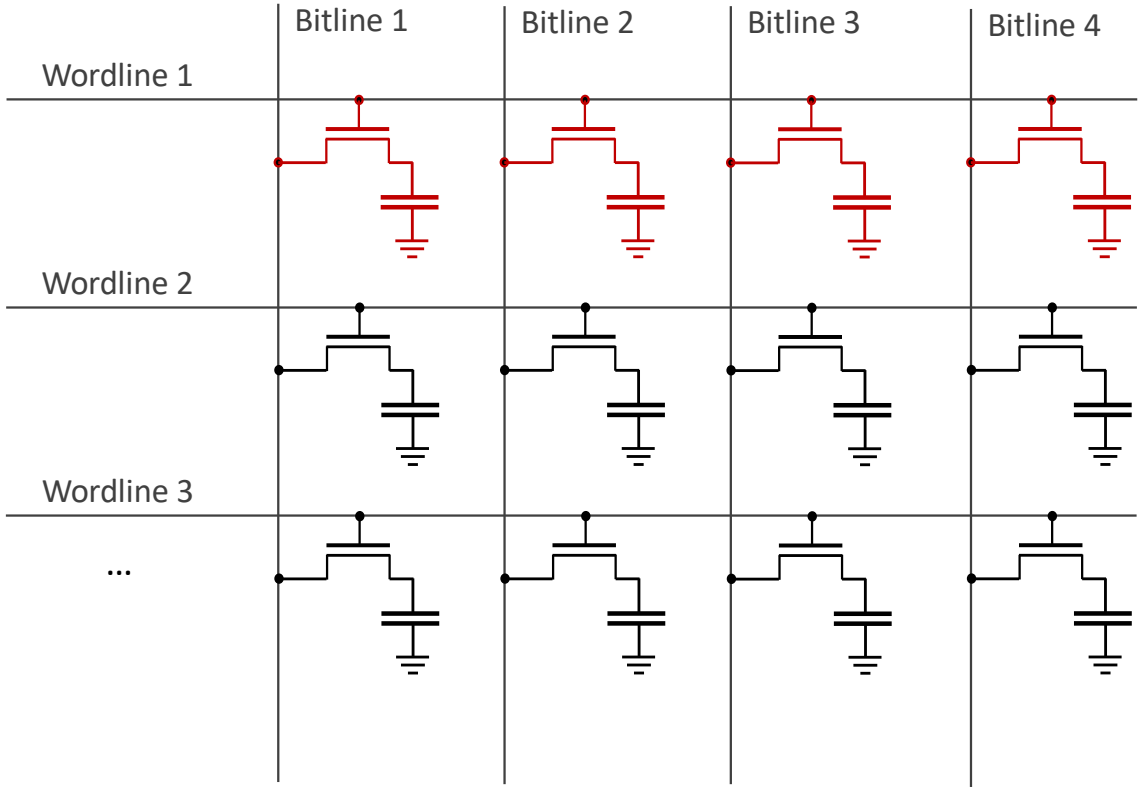
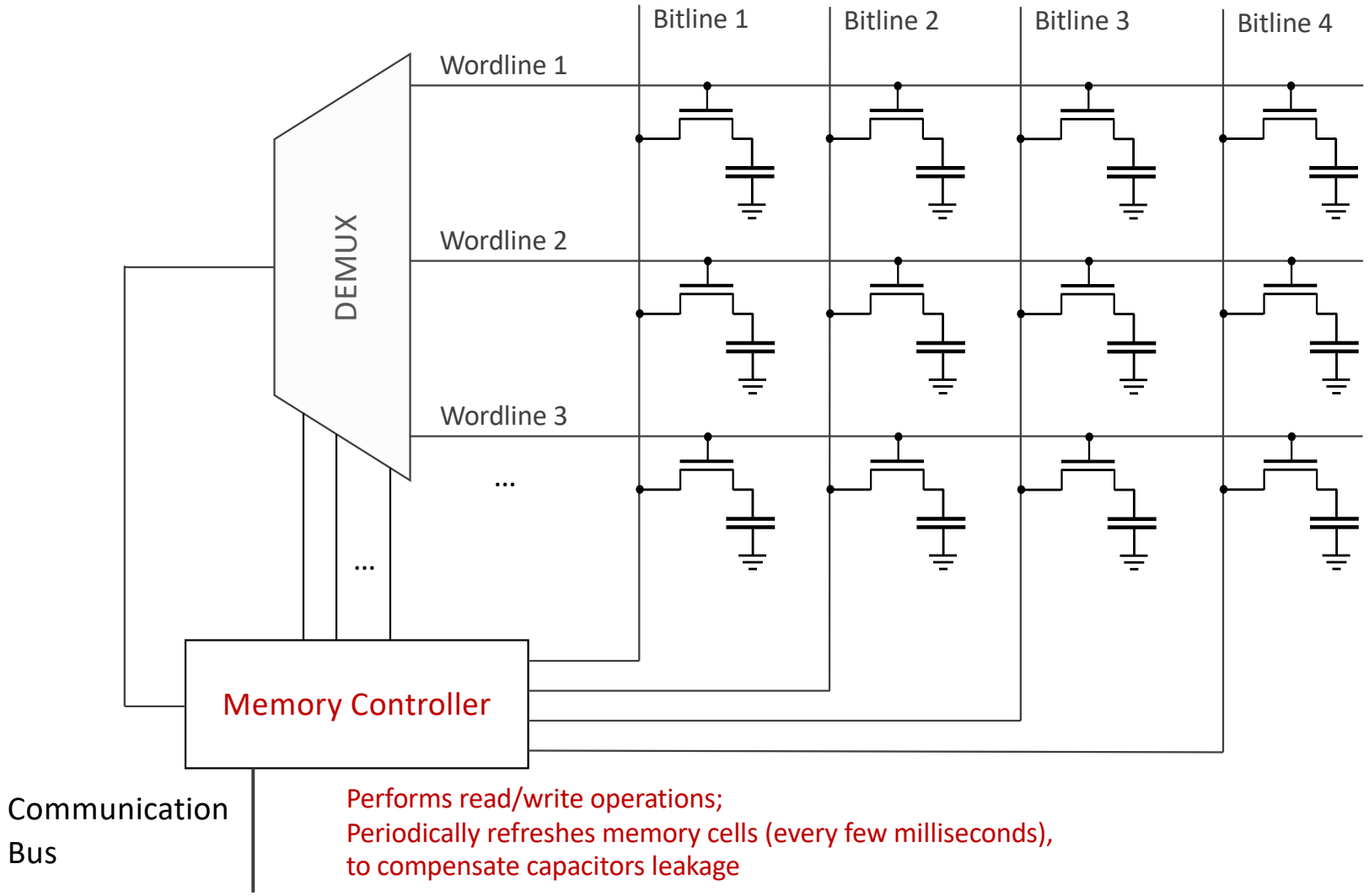
Several memory cells are connected to the same wordline



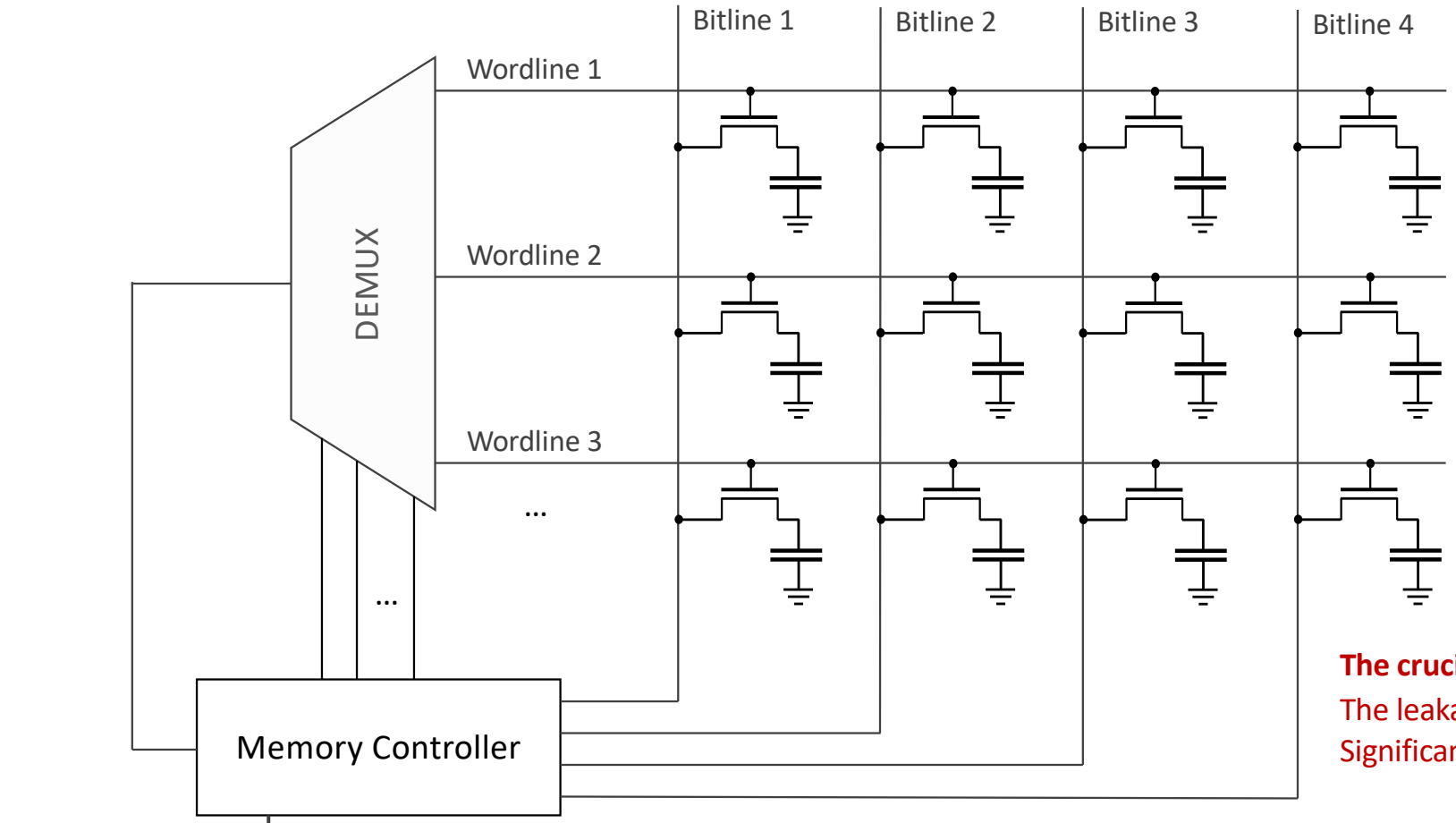
DRAM Memory: the Work Principle

Memory controller operates with memory cells,
by using demultiplexors, encoders, etc.



Performs read/write operations;
Periodically refreshes memory cells (every few milliseconds),
to compensate capacitors leakage

DRAM Memory: the Work Principle



The crucial problems:

The leakage of capacitors;

Significant time needed for charging

Performs read/write operations;

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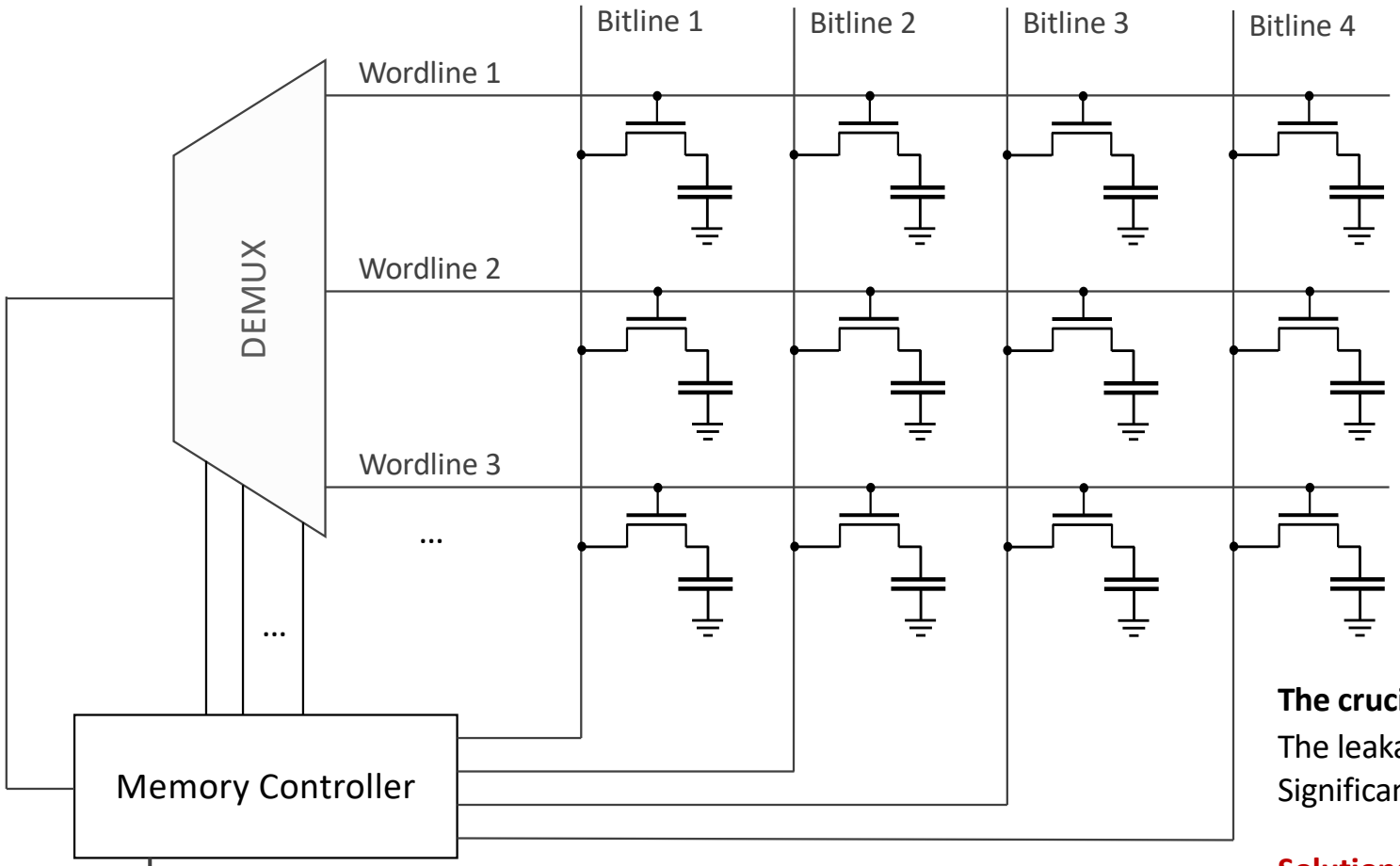

Performs read/write operations;
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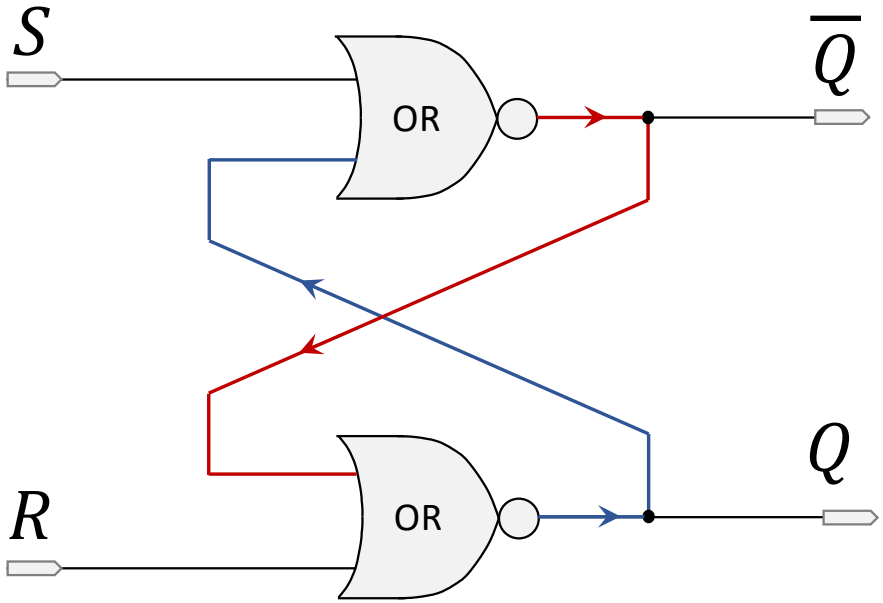
The crucial problems:

The leakage of capacitors;
Significant time needed for charging

Solution:

To use SRAM,
which relies on latches and flip-flops (different from capacitors)

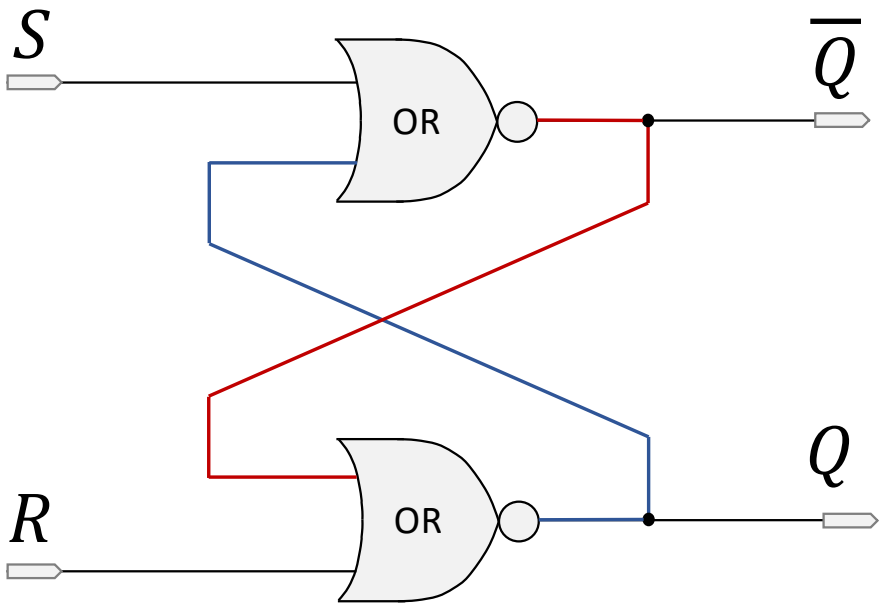
Latch Recap: an electronic circuit to store one bit of information



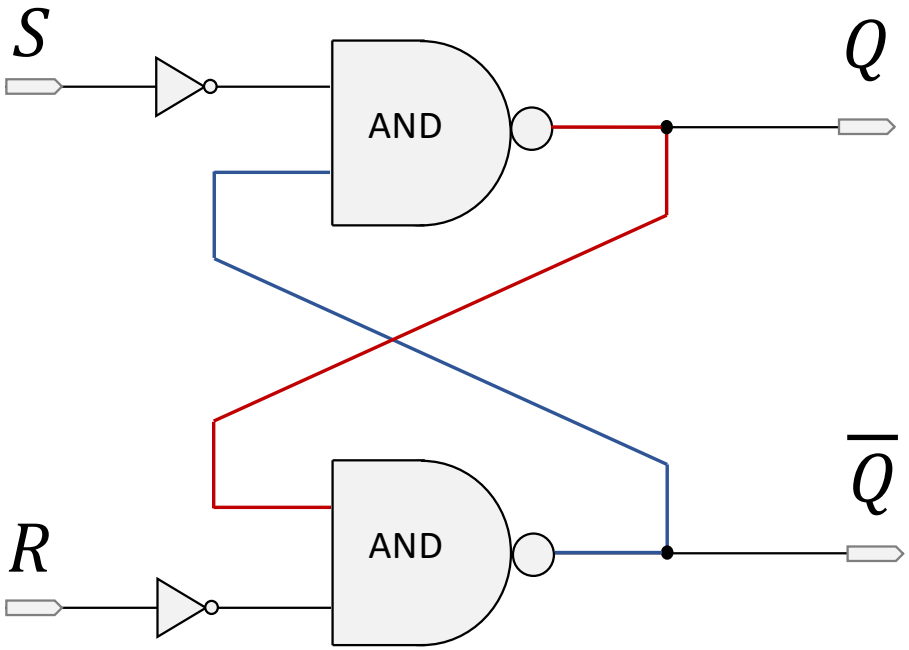
S	**R**	**Q**
1	0	1
0	1	0
0	0	Q^{prev}
1	1	Illegal inputs

Latch Recap: multiple logic implementations are available

1) Implementation by using NOR logic gates:

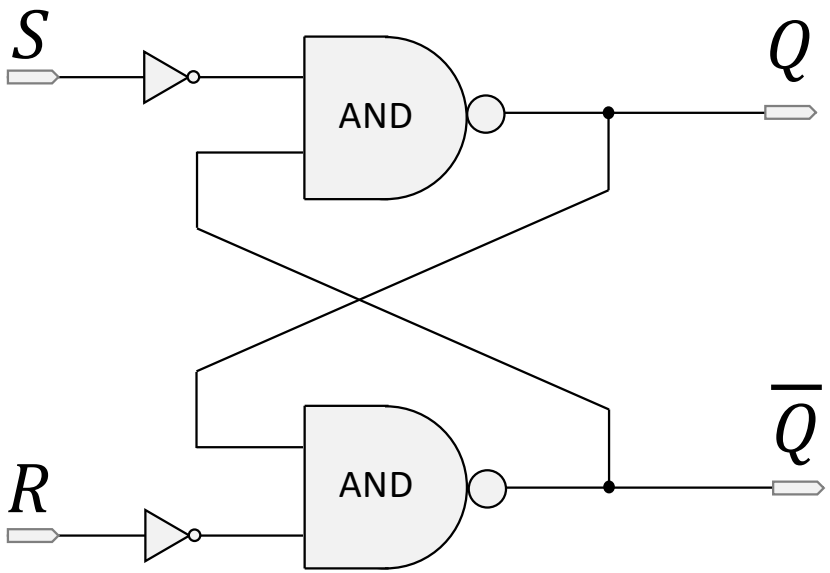


2) by using NAND logic gates:



These representations are logical oversimplified representations, hiding many implementation details

Latch Logical representation:



Before usage, latch is initialized by one of these input combinations:

either R = 1 & S = 0, or S = 1 & R = 0;

Latch hardware implementation should be such, that one of these input combinations results into Q and $\overline{Q}$ according to a latch specification

Electrical circuit implementation (one of many):

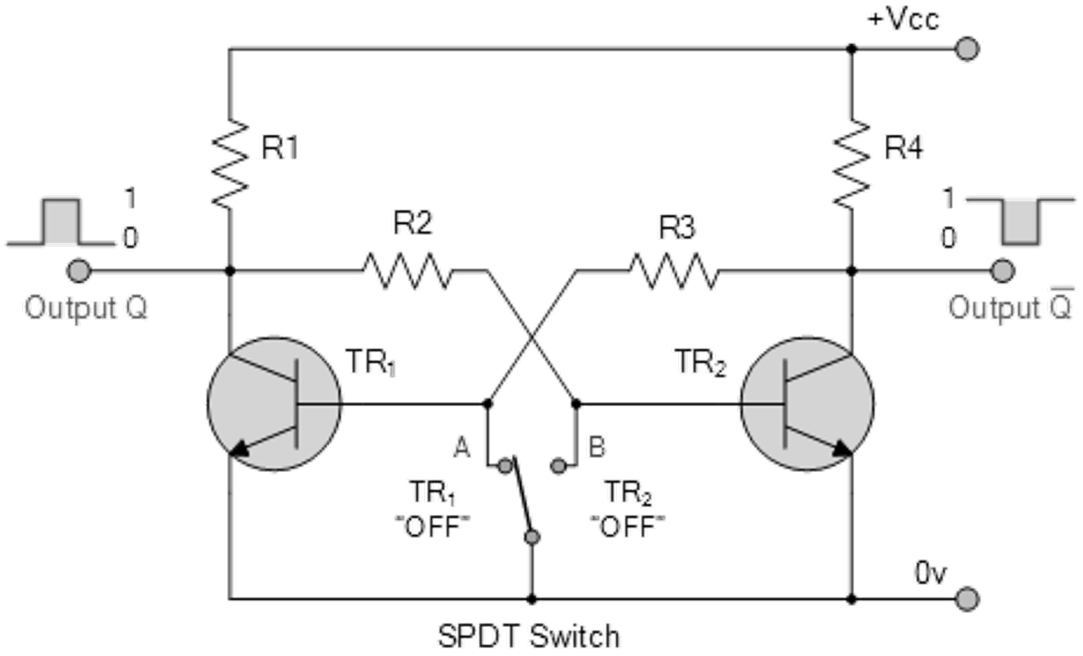


Image is taken from https://www.electronics-tutorials.ws/waveforms/bistable.html

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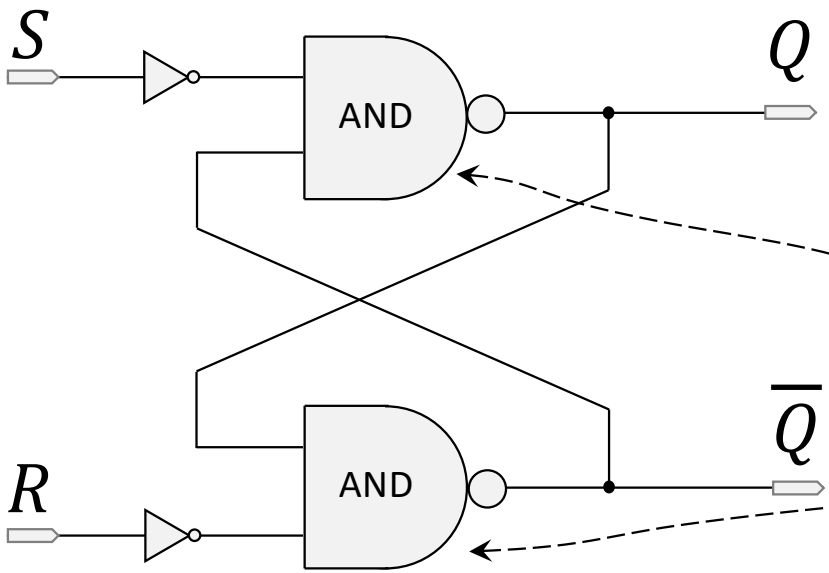

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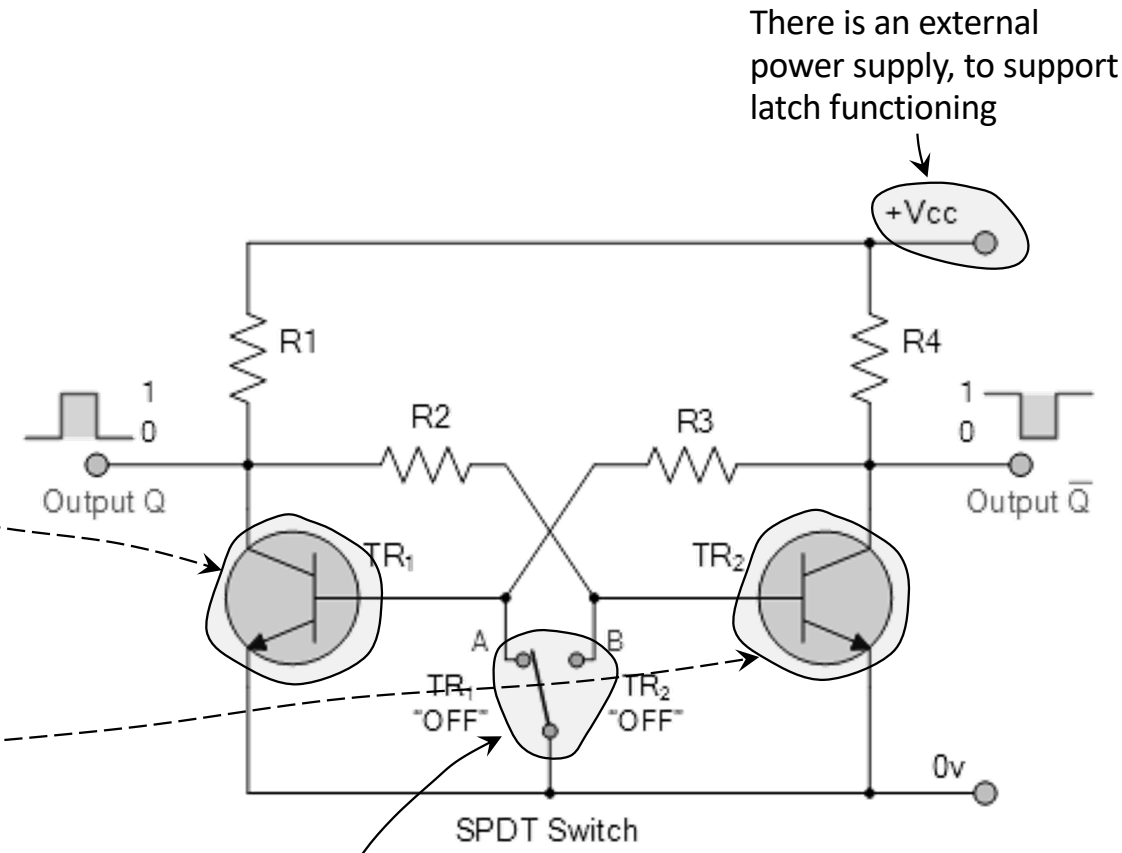

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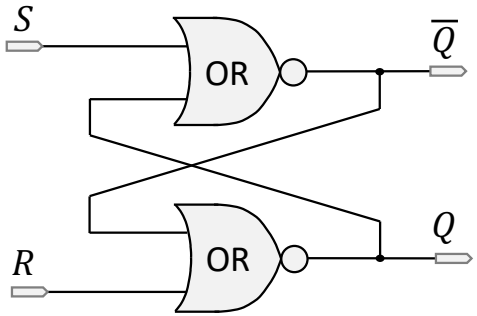
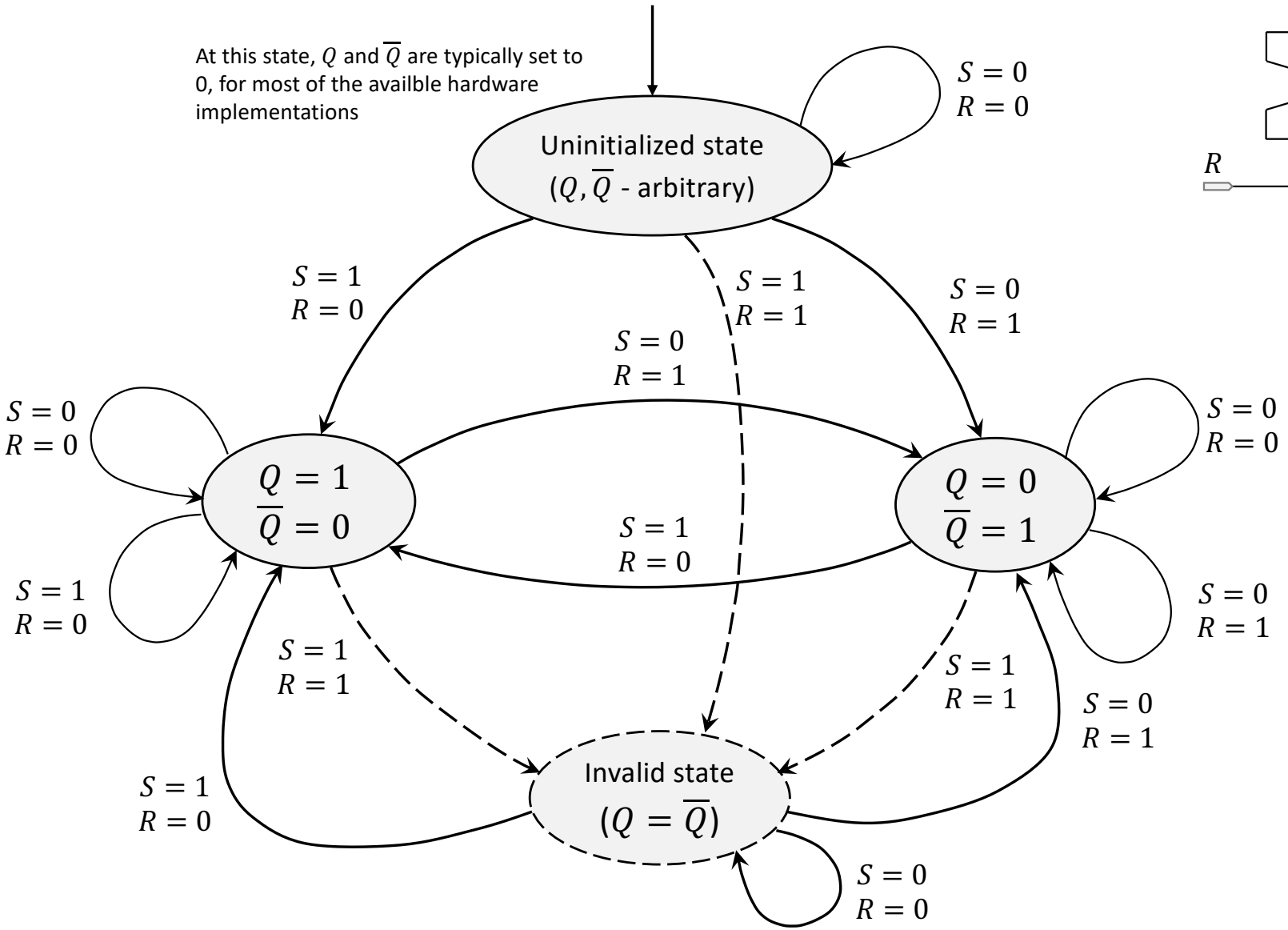
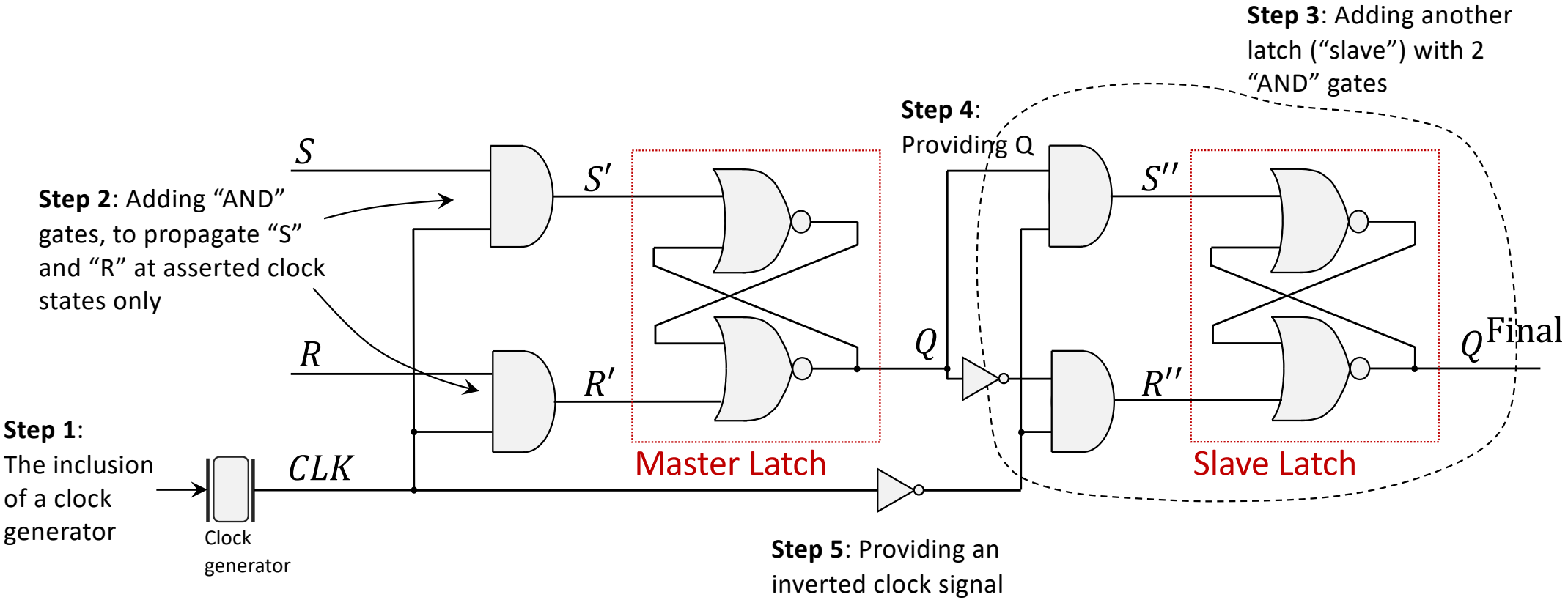
State Transition Diagram for a Latch





Recap: A Synchronous Flip-Flop Constructed of S/R Latches



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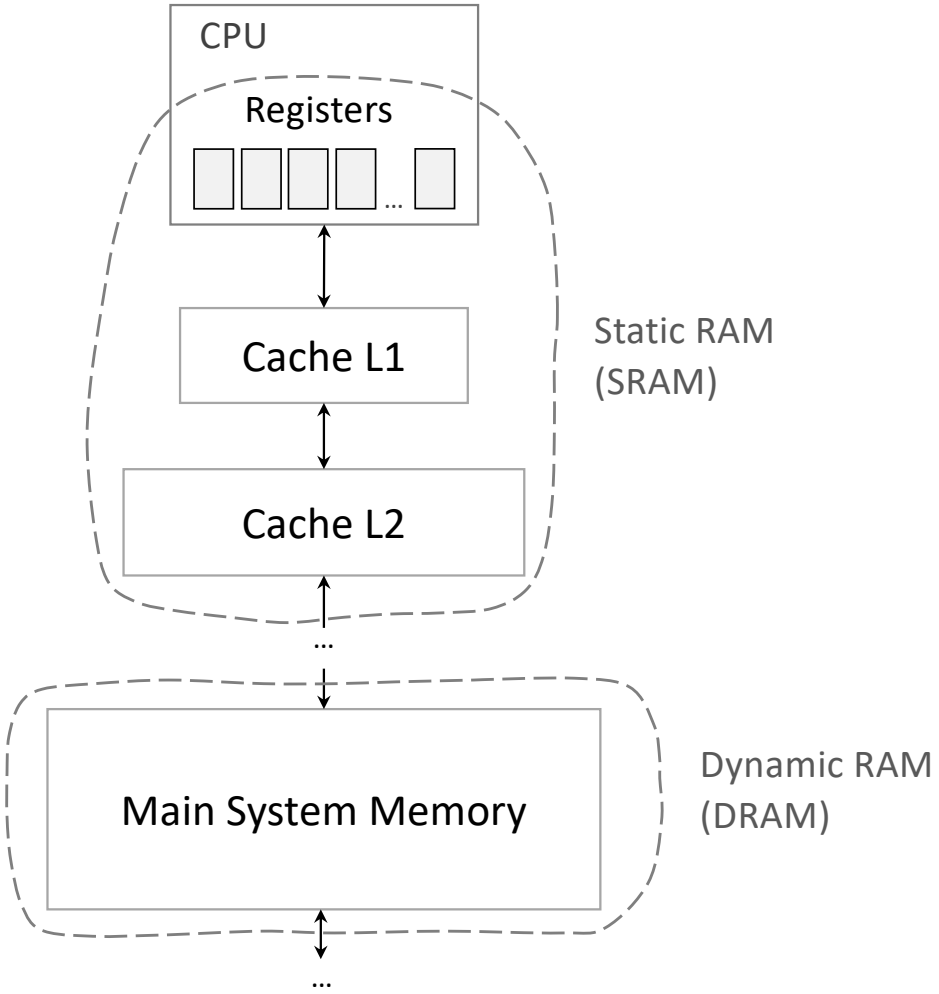

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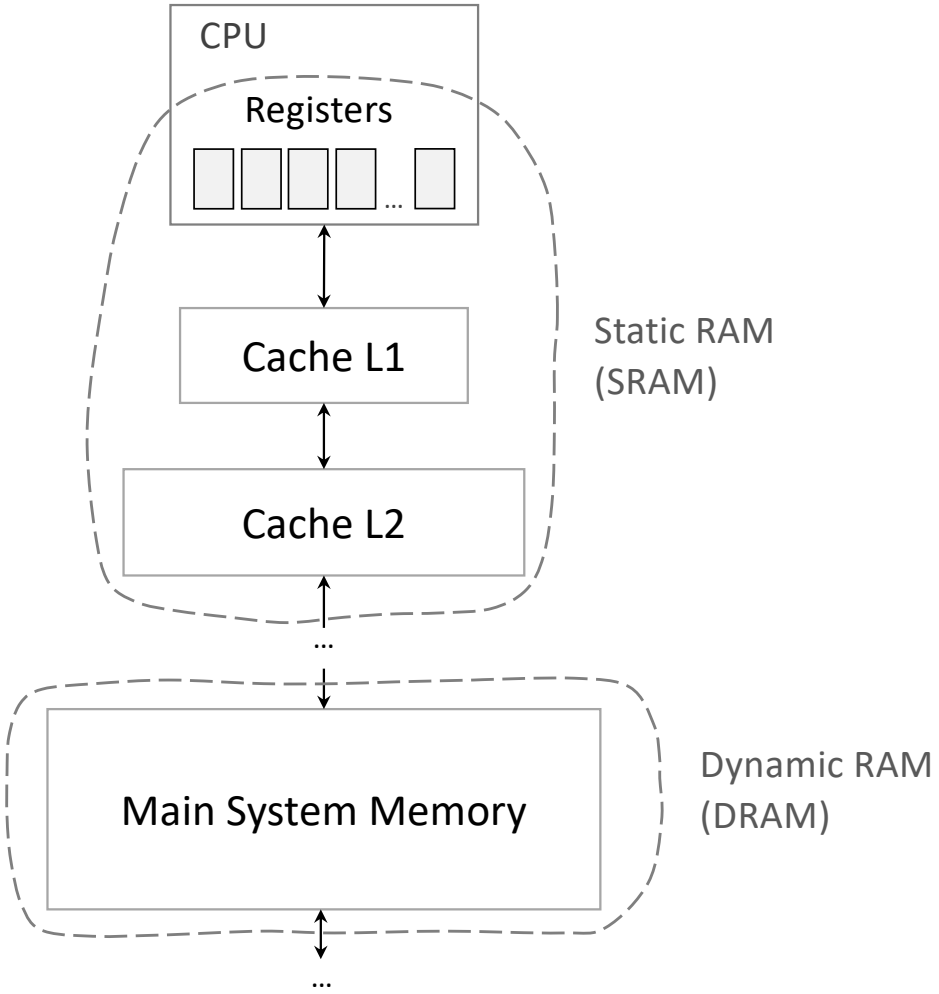
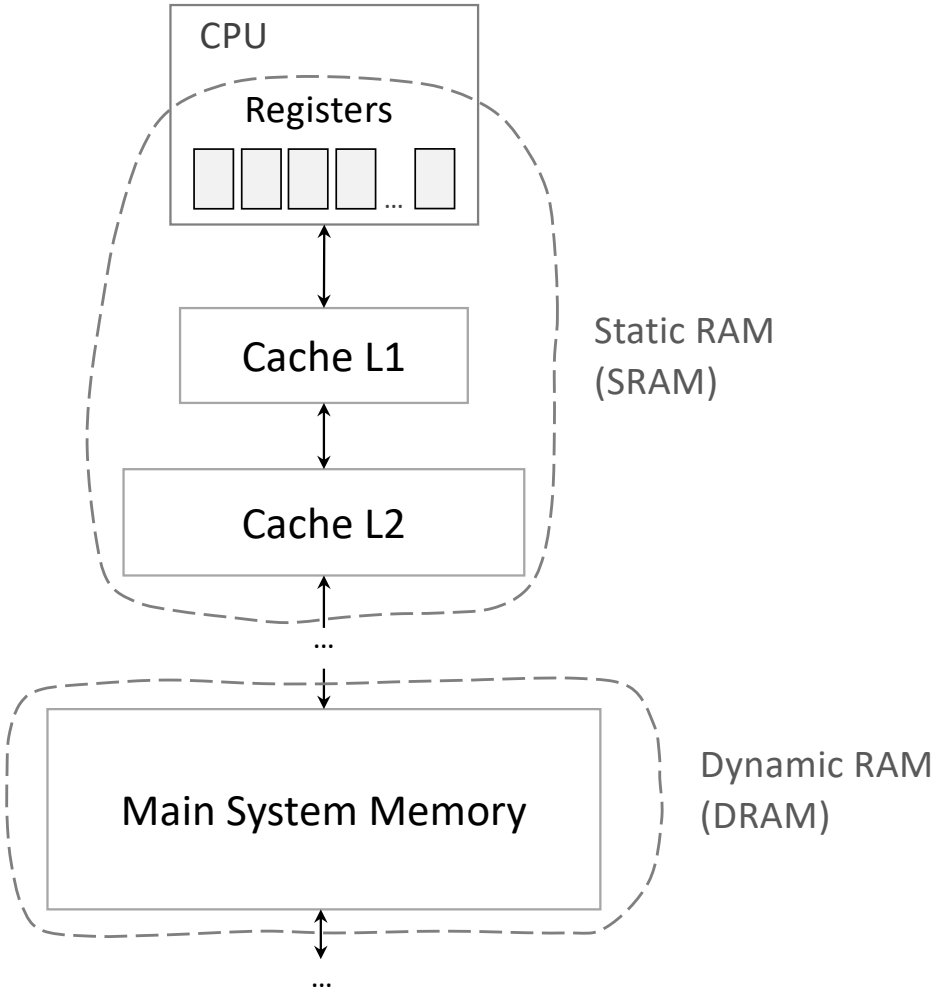


Characteristic	SRAM	DRAM
Access Speed	Faster	Slower
Storage Capacity		
Storage Element		
Usage		
Cost		
Power Consumption		
Organisation		
Power Leakage		
Chip Reliability		
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
Storage Element		
Usage		
Cost		
Power Consumption		
Organisation		
Power Leakage		
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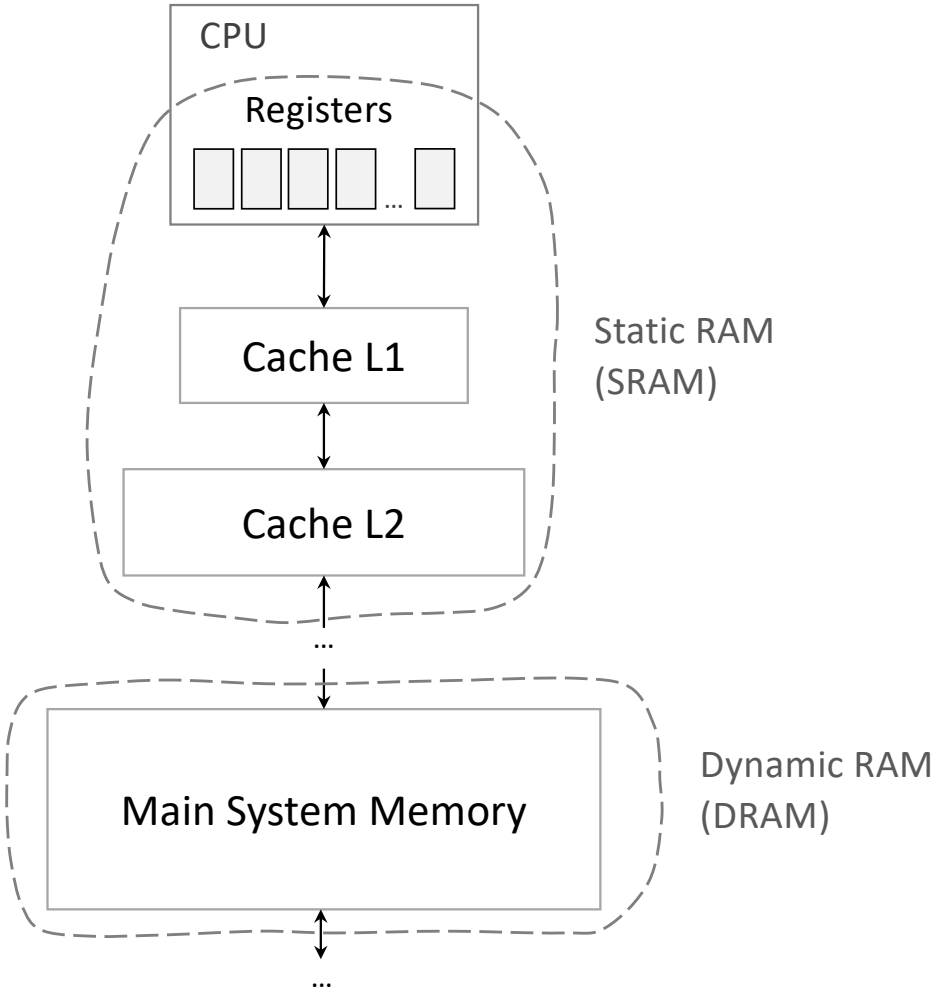
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
Storage Element	Flip-flop	Capacitor
Usage		
Cost		
Power Consumption		
Organisation		
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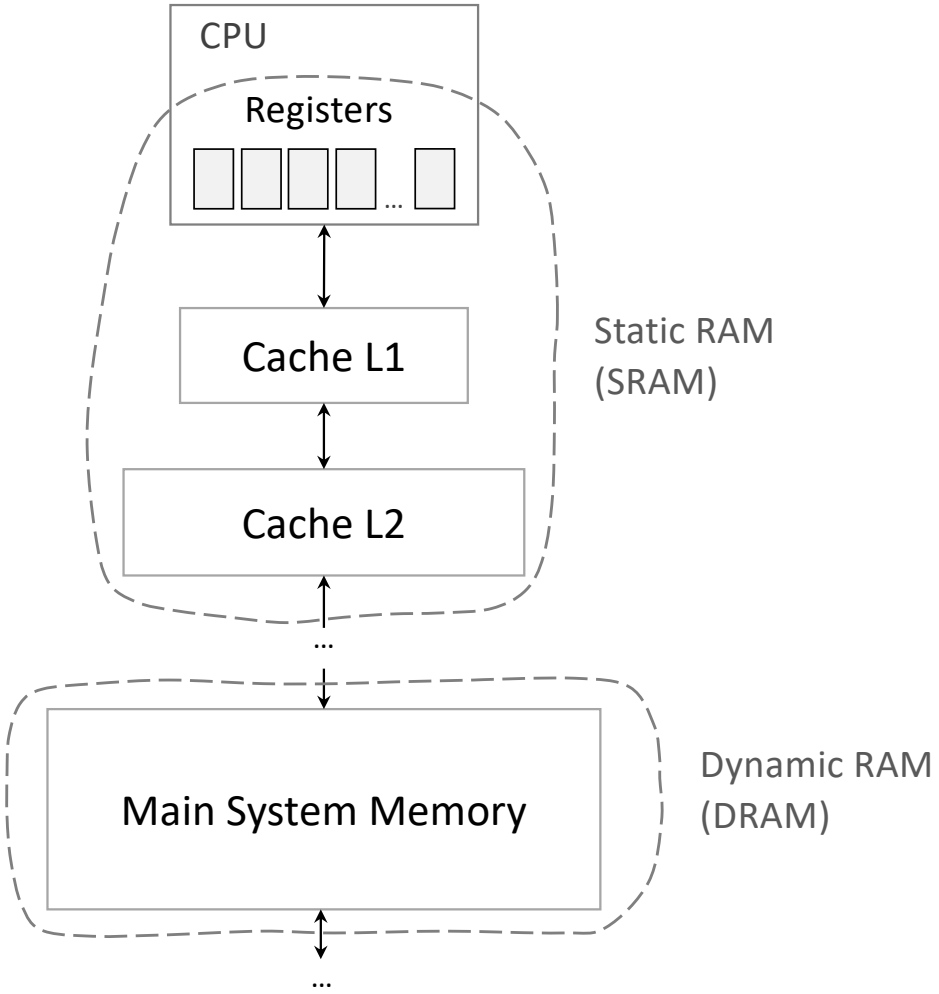
Chip Reliability		
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
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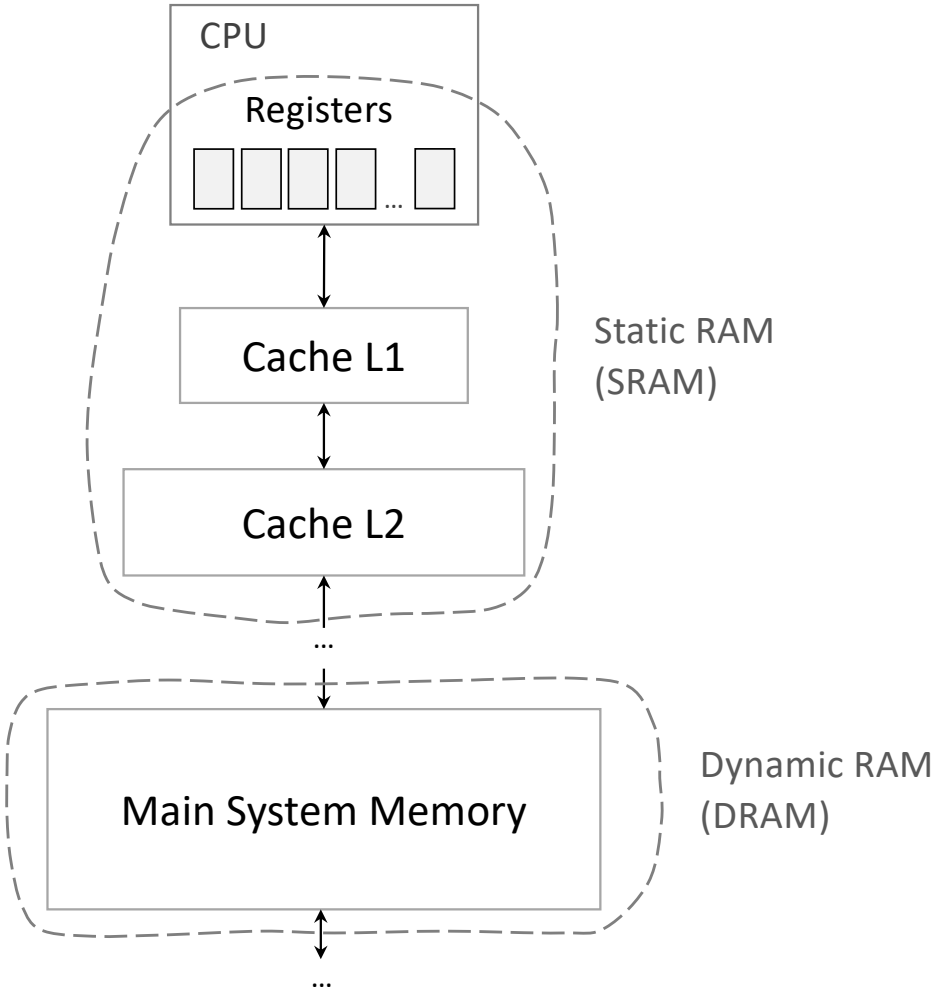
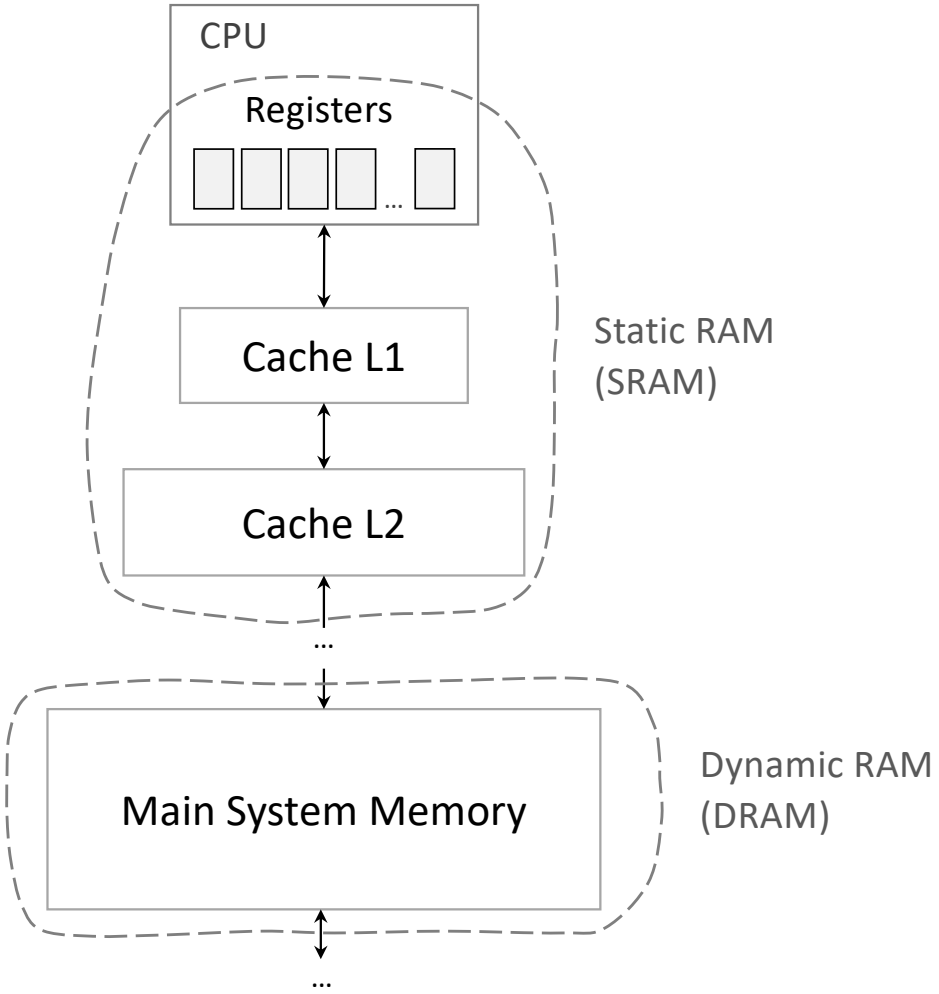
The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
Storage Element	Flip-flop	Capacitor
Usage	CPU cache, registers	System memory
Cost	Expensive	Cheaper
Power Consumption		
Organisation		
Power Leakage		
Chip Reliability		
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



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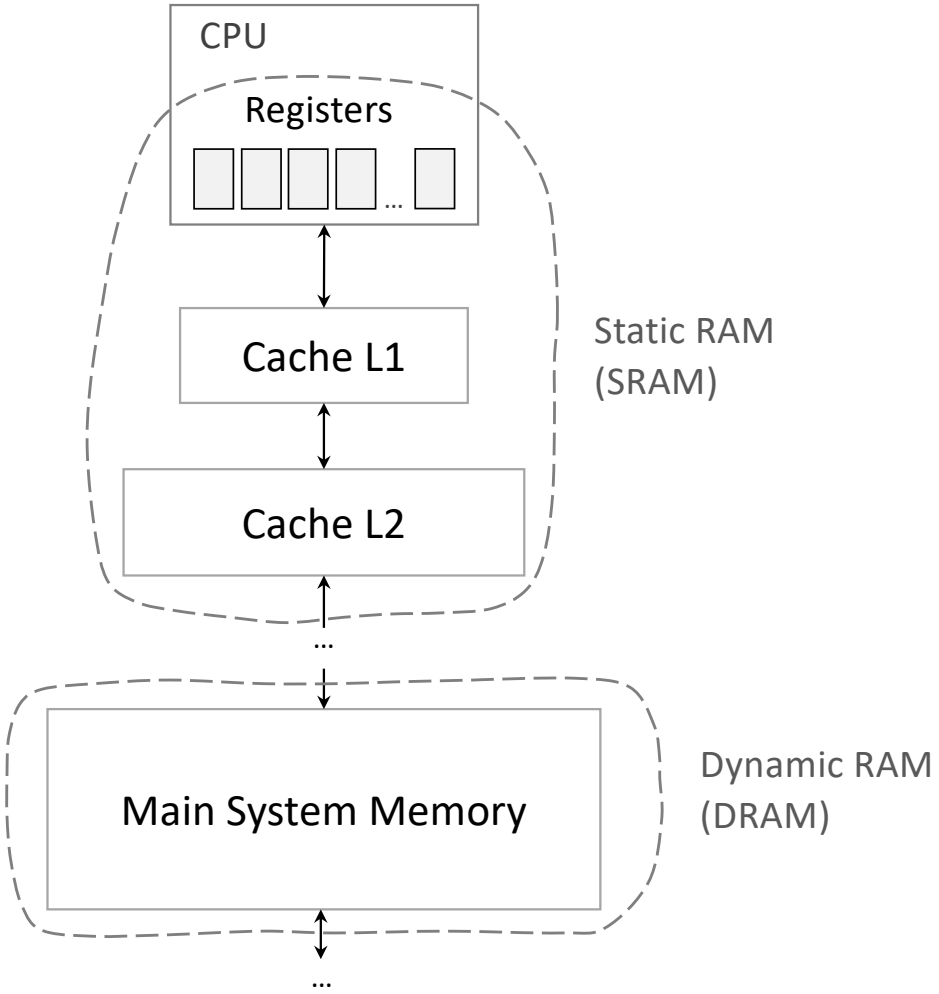
The Comparison of DRAM and SRAM Memory Types



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Storage Capacity	Smaller	Larger
Storage Element	Flip-flop	Capacitor
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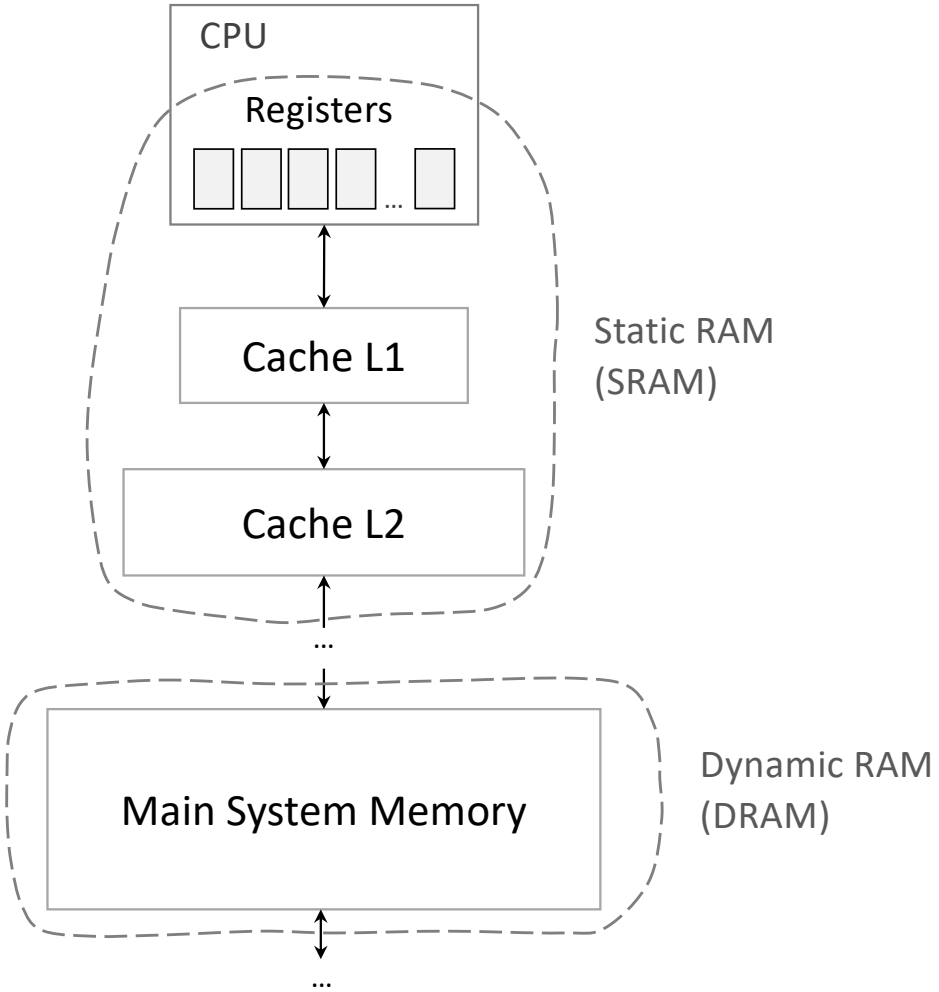
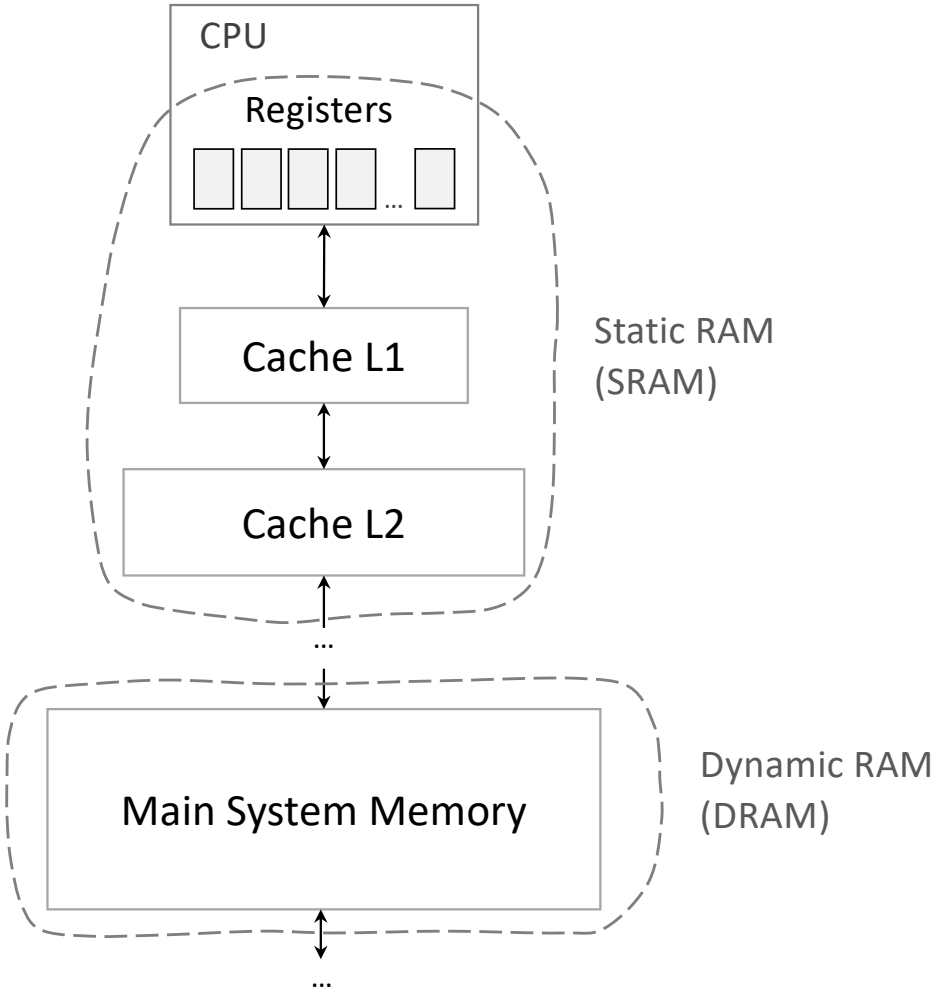
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage		
Chip Reliability		
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
Storage Element	Flip-flop	Capacitor
Usage	CPU cache, registers	System memory
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage	Not present	Significant
Chip Reliability		
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



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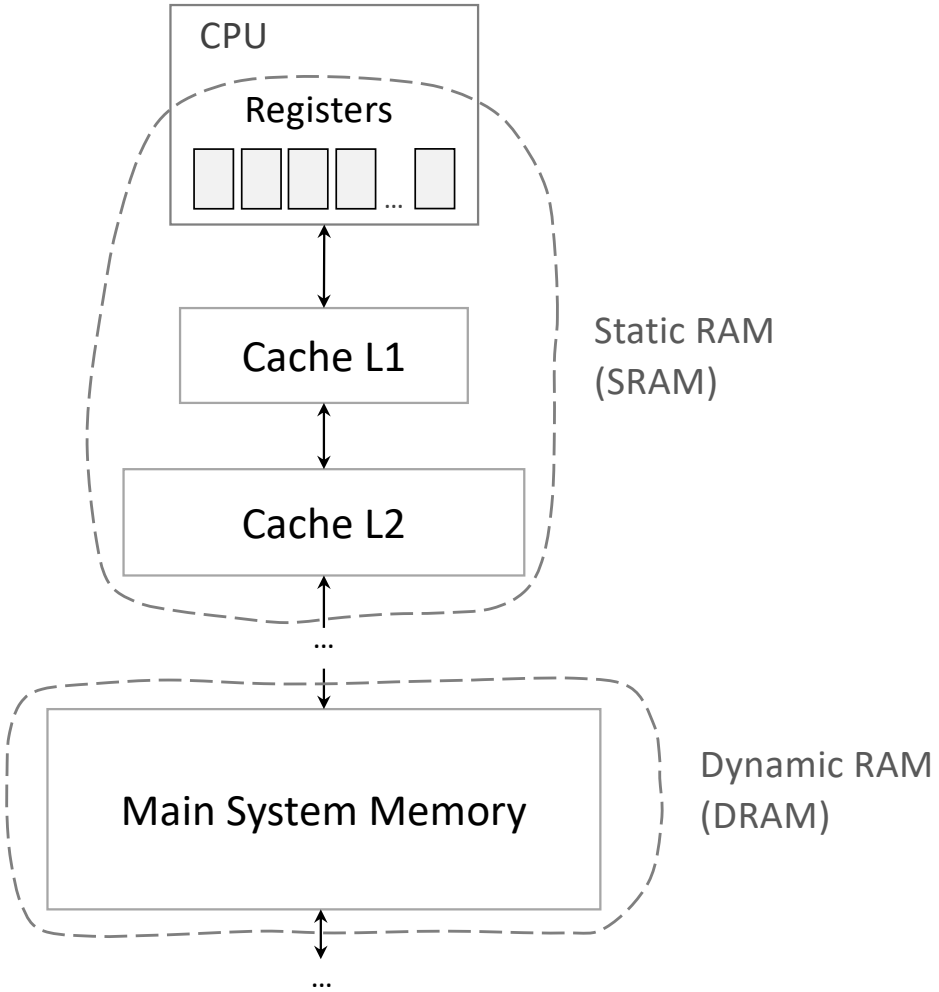
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage	Not present	Significant
Chip Reliability	More reliable	Less reliable
Volatility		
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
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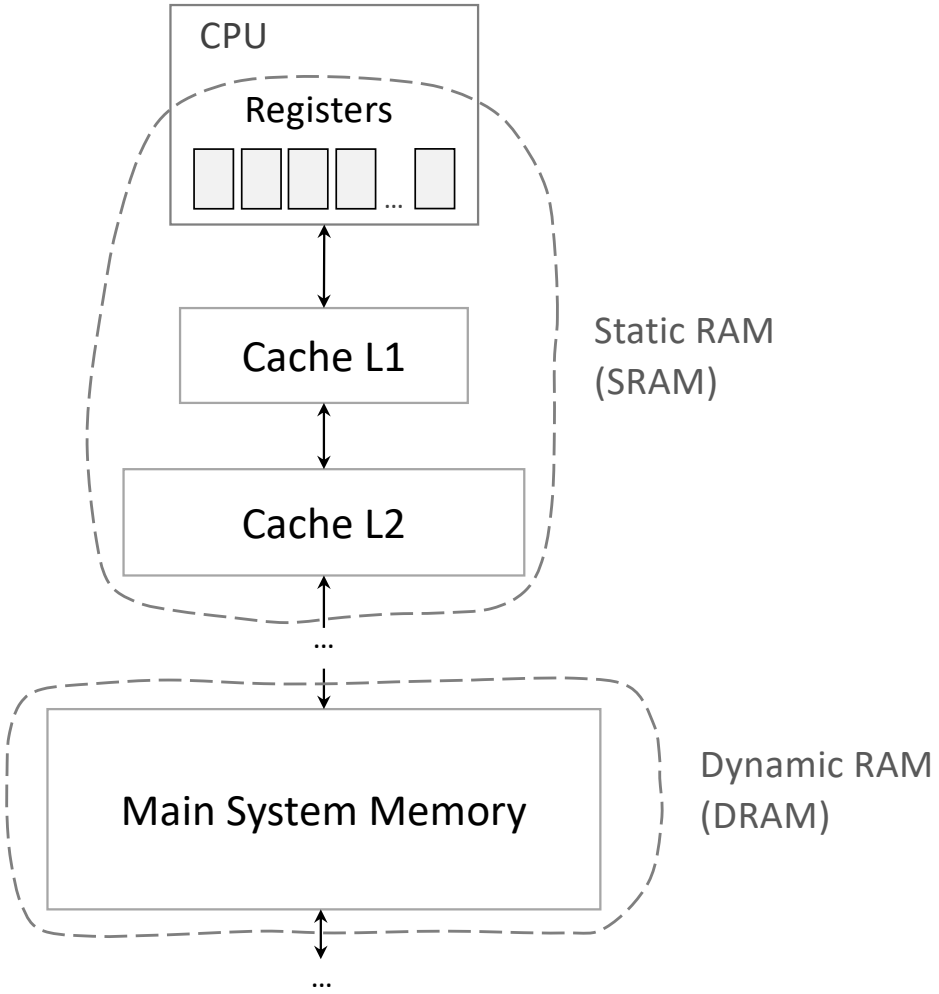
Storage Element	Flip-flop	Capacitor
Usage	CPU cache, registers	System memory
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage	Not present	Significant
Chip Reliability	More reliable	Less reliable
Volatility	Both are volatile (loose data if power is off)	
Memory Cell Access		

The Comparison of DRAM and SRAM Memory Types



Characteristic	SRAM	DRAM
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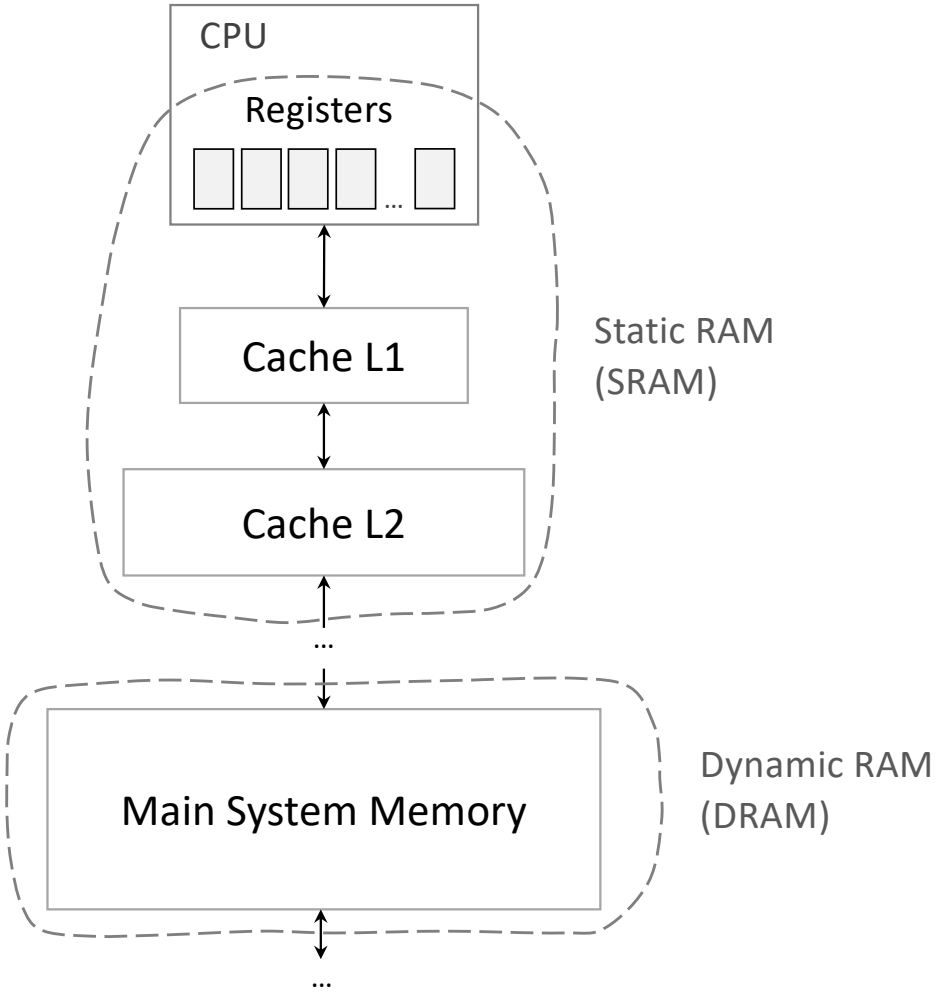
Storage Element	Flip-flop	Capacitor
Usage	CPU cache, registers	System memory
Cost	Expensive	Cheaper
Power Consumption	Lower	Higher
Organisation	Complex	Simpler
Power Leakage	Not present	Significant
Chip Reliability	More reliable	Less reliable
Volatility	Both are volatile (require electrical power to keep data)	
Memory Cell Access	Each cell is accessed directly, unlike Sequential Access Memory (SAM)	

The Comparison of DRAM and SRAM Memory Types



Characteristic	**SRAM**	**DRAM**
Access Speed	Faster	Slower
Storage Capacity	Smaller	Larger
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Usage	CPU cache, registers	System memory
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