Computer Architecture
Lecture 4

Combinational Logic Circuits (Cont.)

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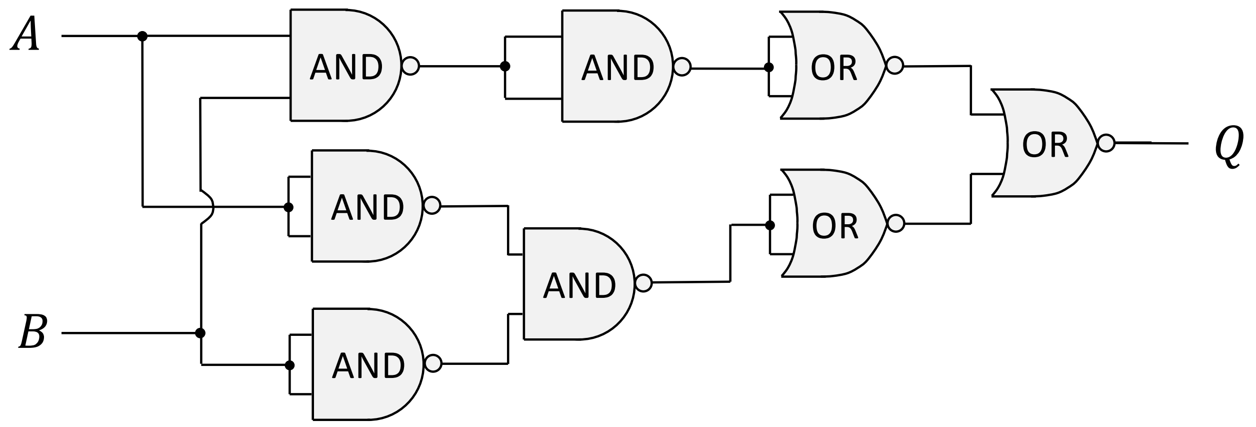
Recap: Characteristics of Combinational Logic Circuits

Sample combinational logic circuit:



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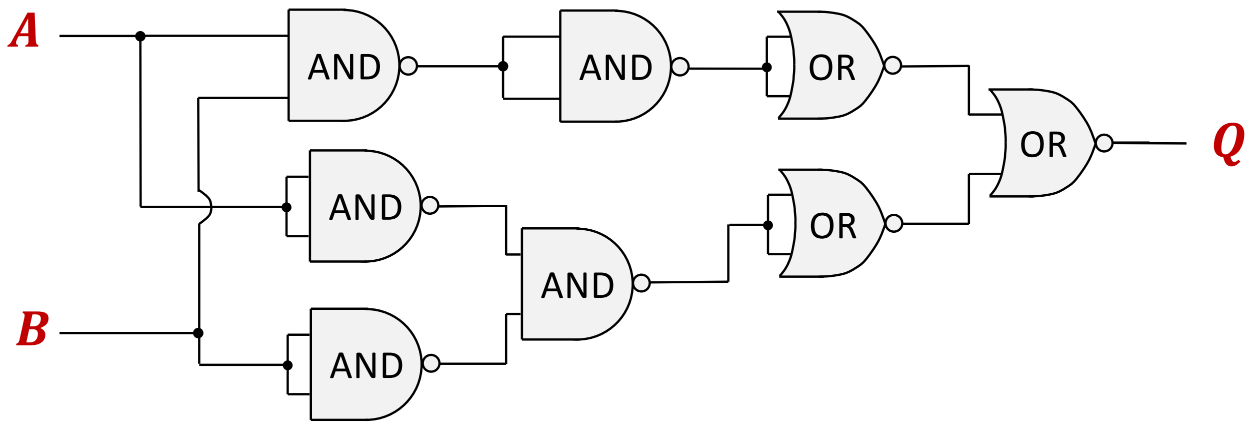

1) An output signal depends just on "current" input signals

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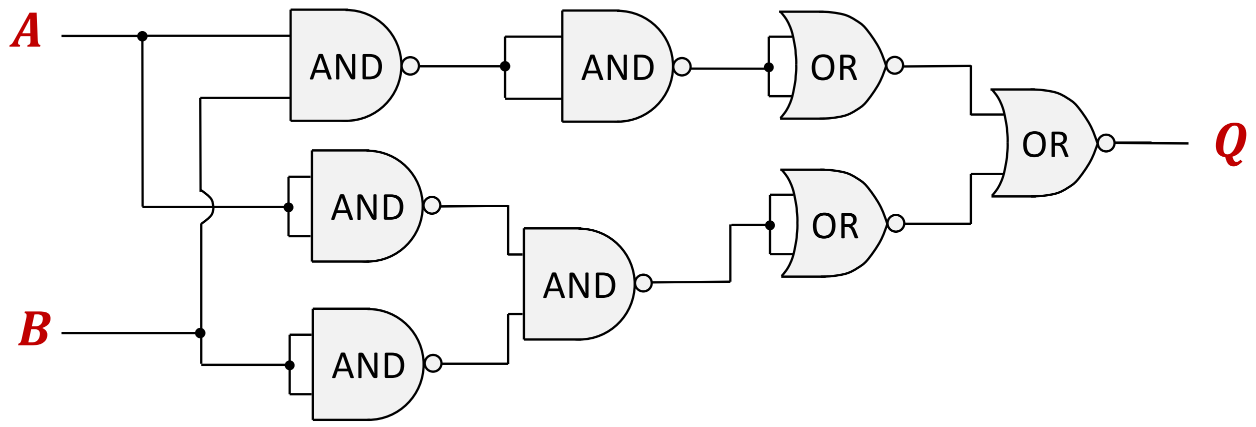

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"Combinational circuit" = combine inputs and get the output

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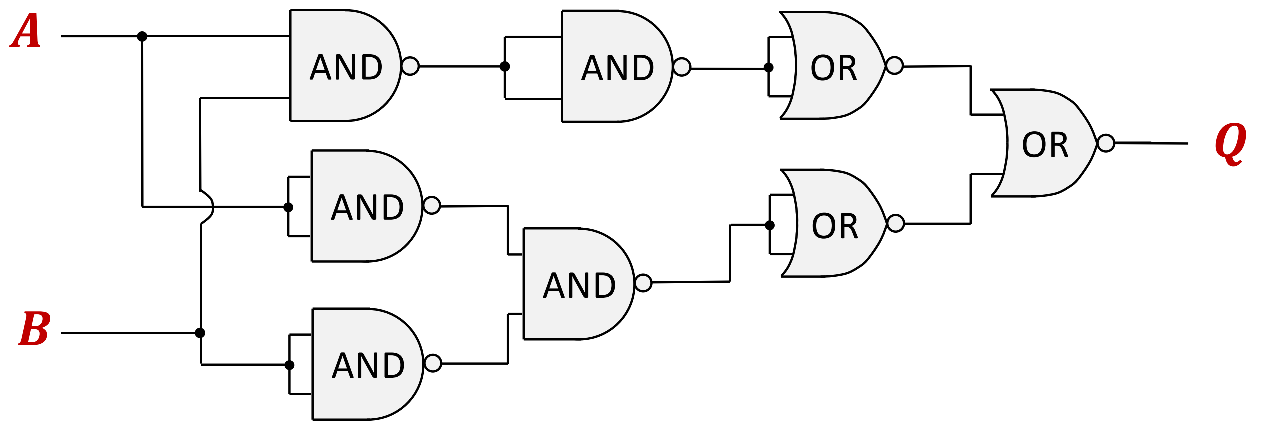

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"Combinational circuit" = combine inputs and get the output

There is no dependency on previous signals or computation results

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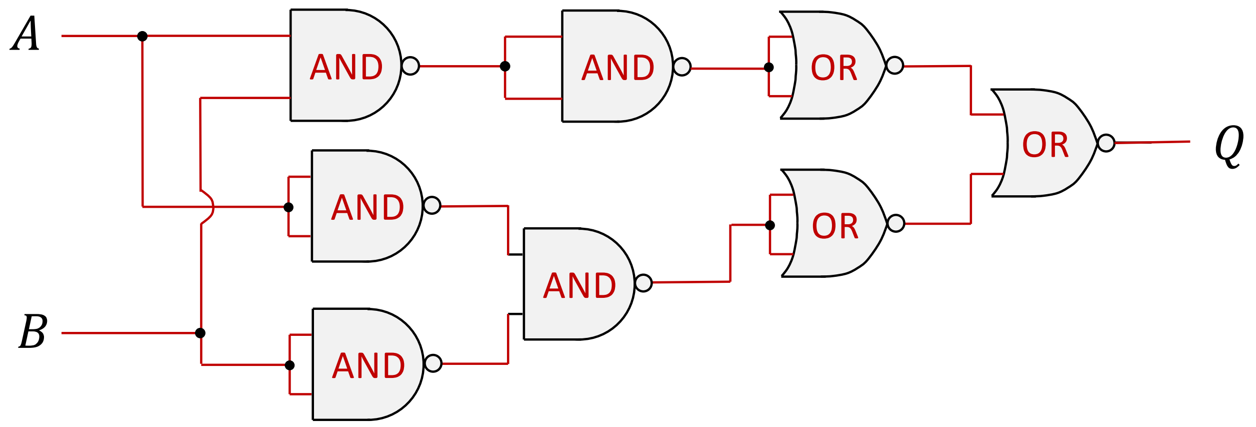

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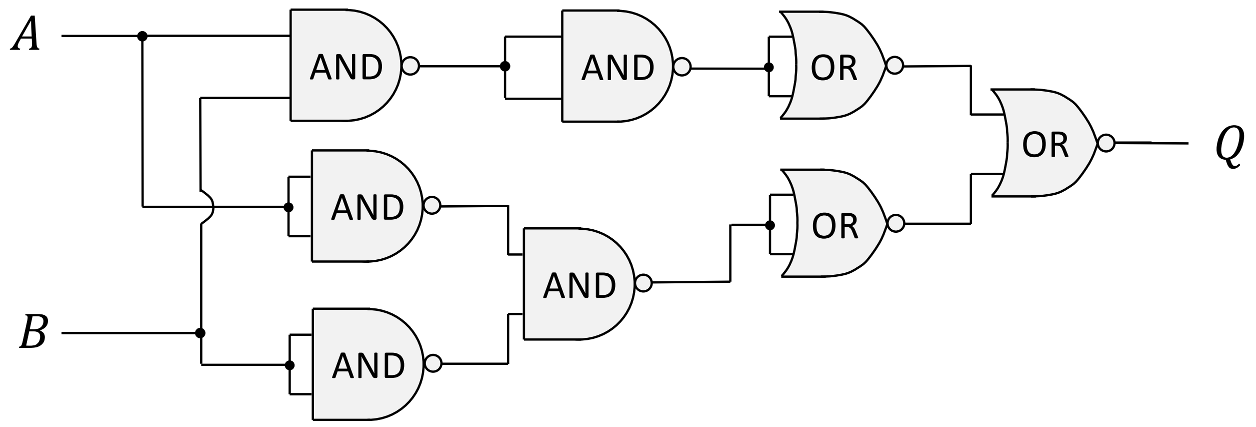

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Observation: “shorter” wires are better, e.g. due to lower propagation delays (there is some connection to Moore’s law)

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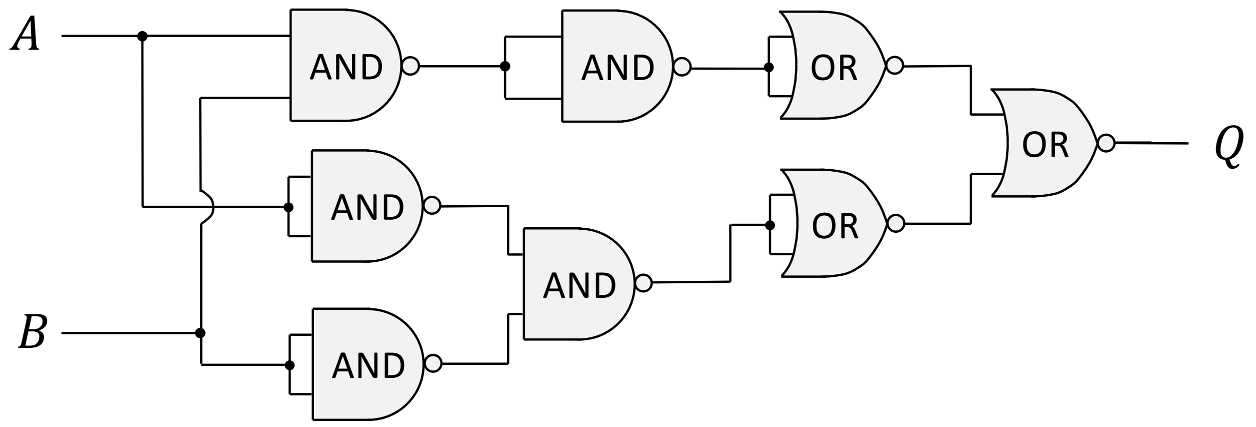

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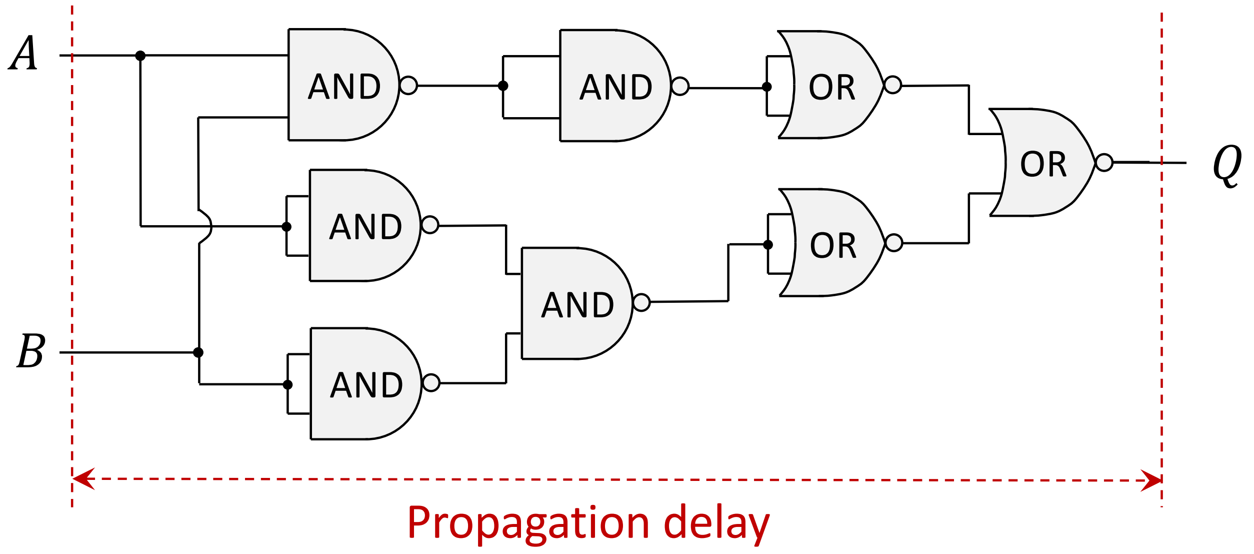

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Propagation delay – time delay between the change of inputs and the update of output

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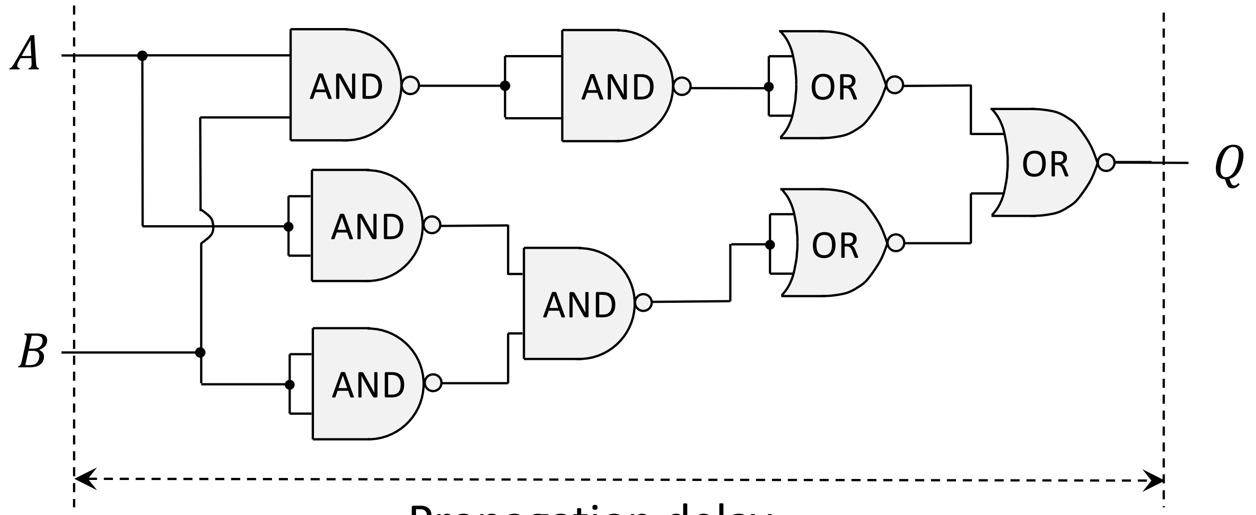

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   Critical Path of the Integrated Circuit – the one taking the longest time (results in the "worst case" propagation delay)

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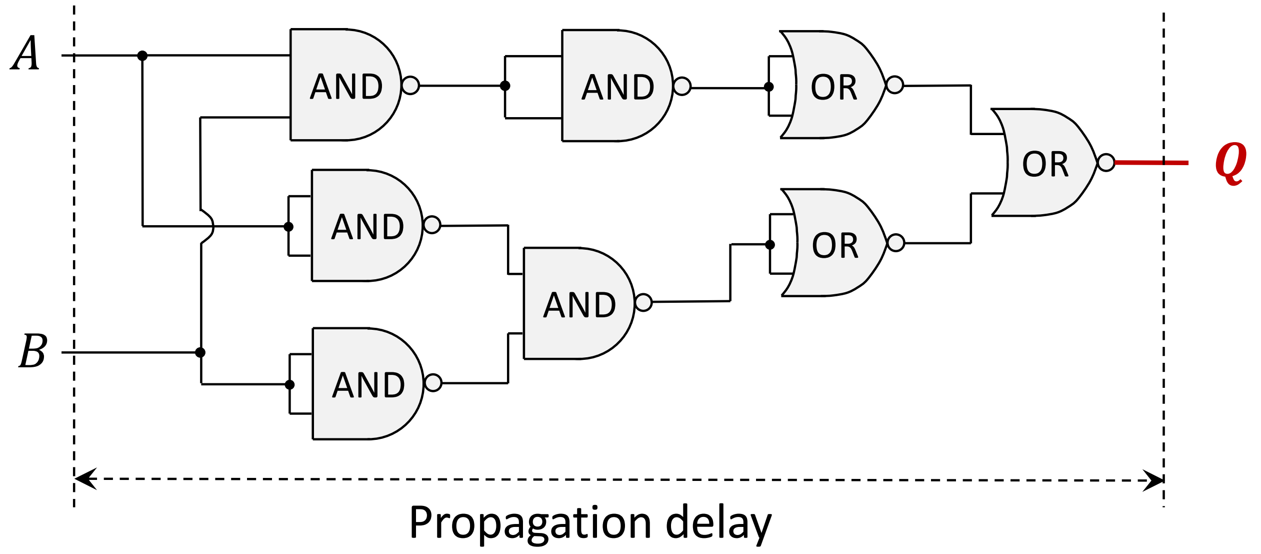

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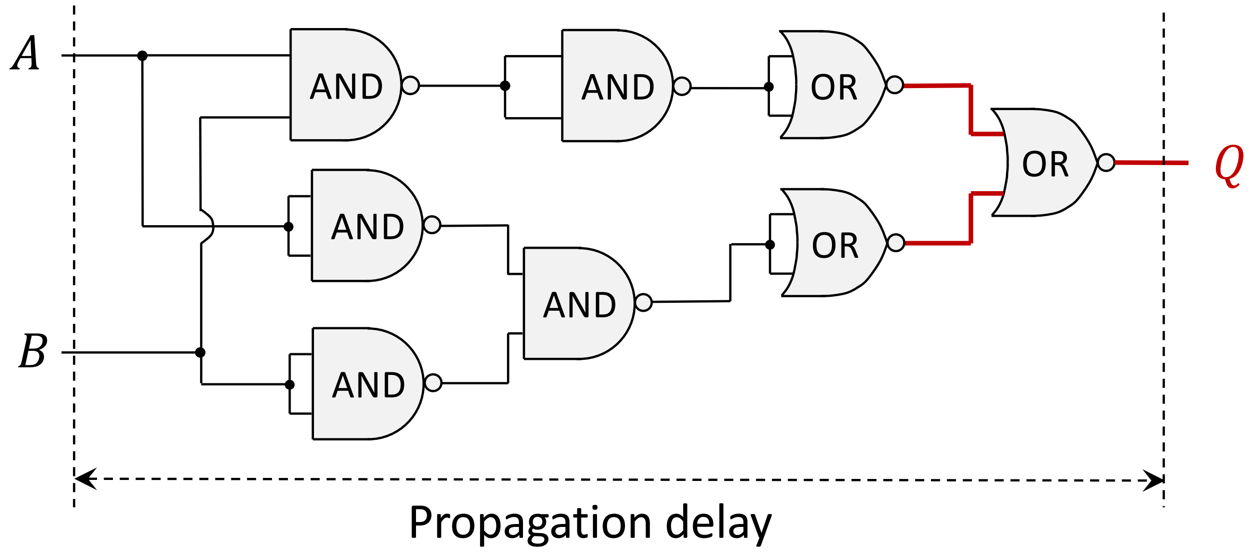

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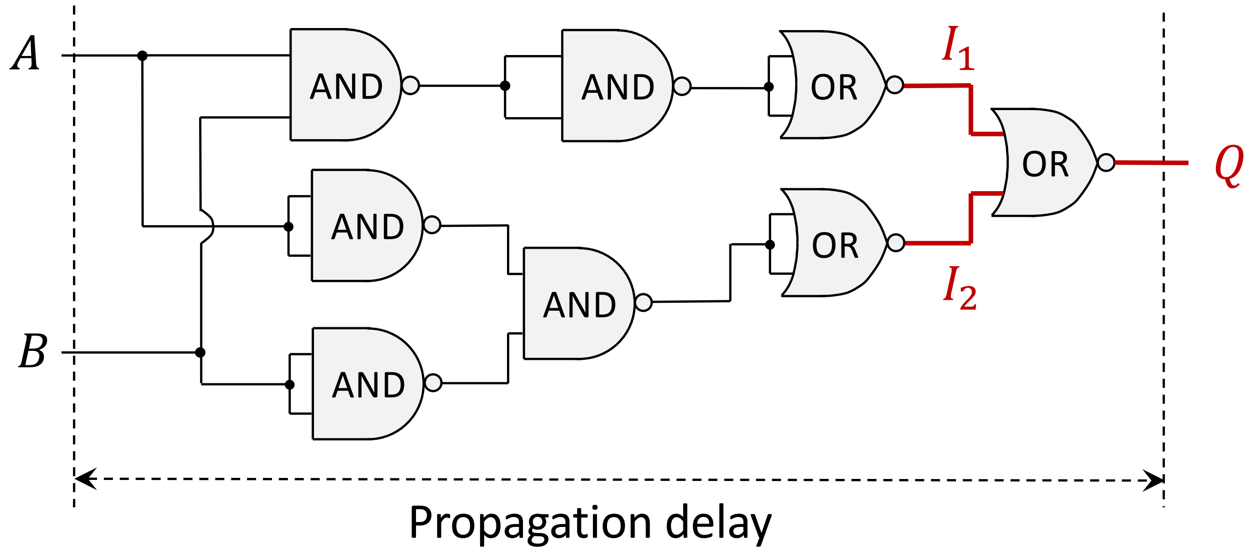

Q is updated when both inputs, I_1 and I_2, are updated;

Inputs I_1 and I_2 are in turn outputs of other logic gates;

Repeat backtracking, to compute the worst case delay

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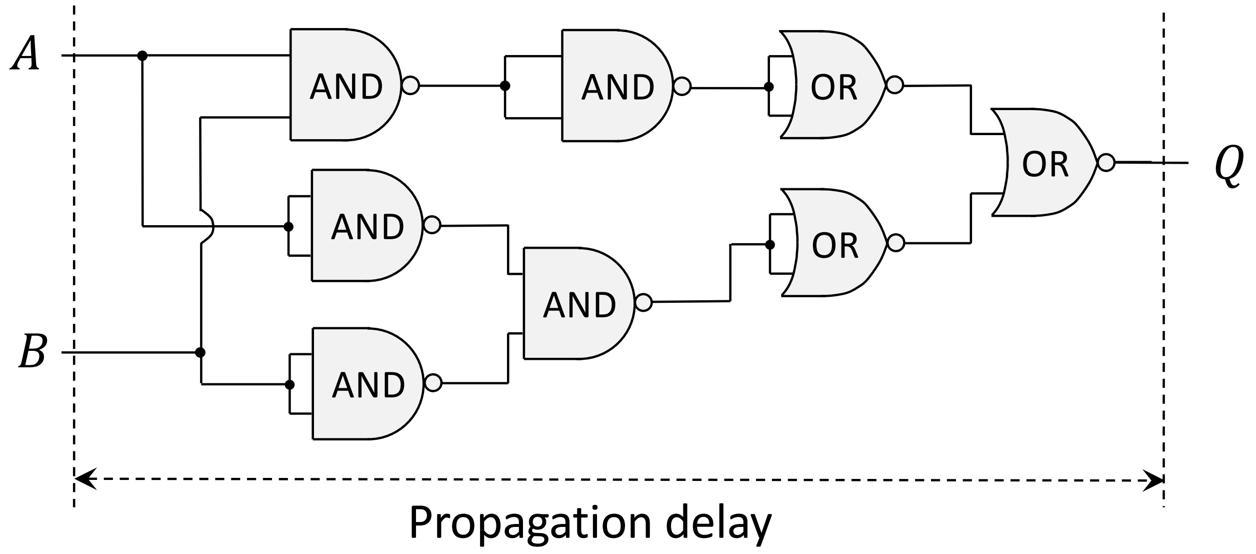

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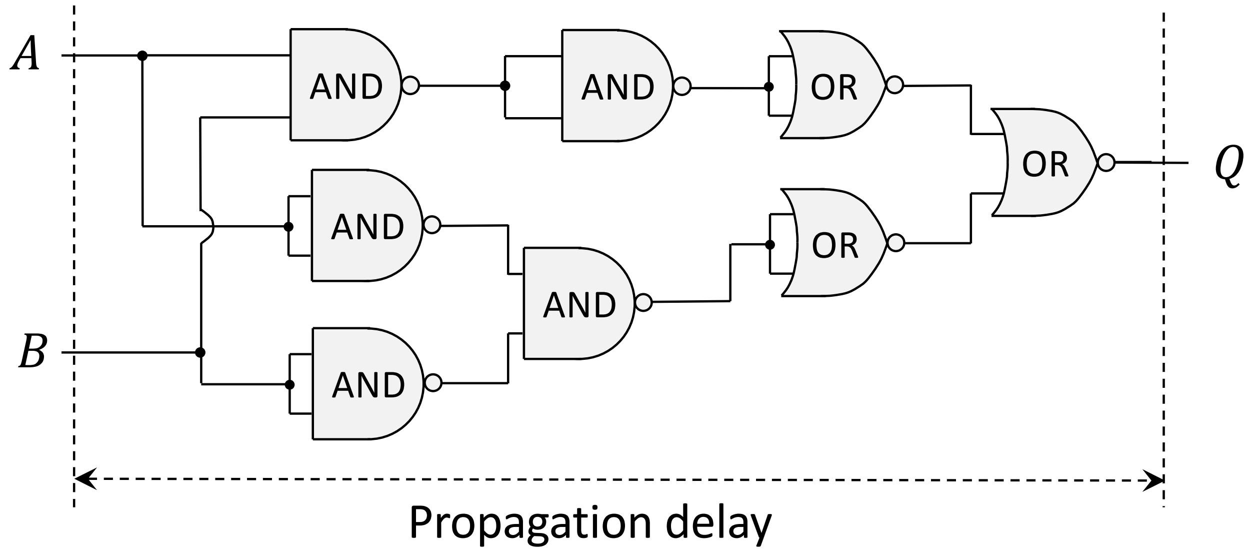

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Sample timing diagram:

"0" – deasserted state;
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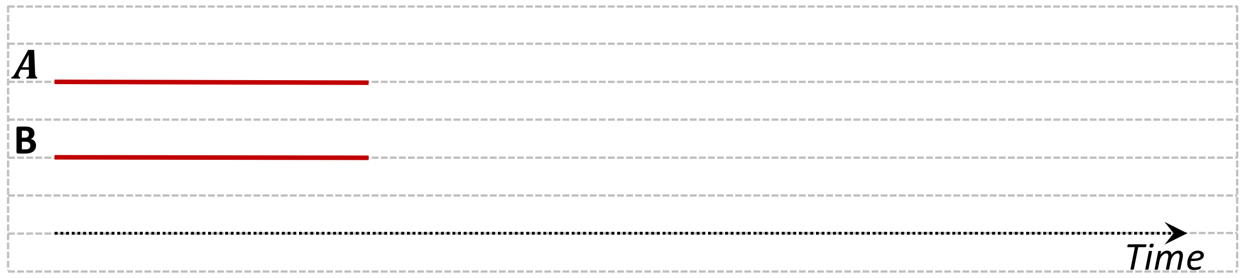

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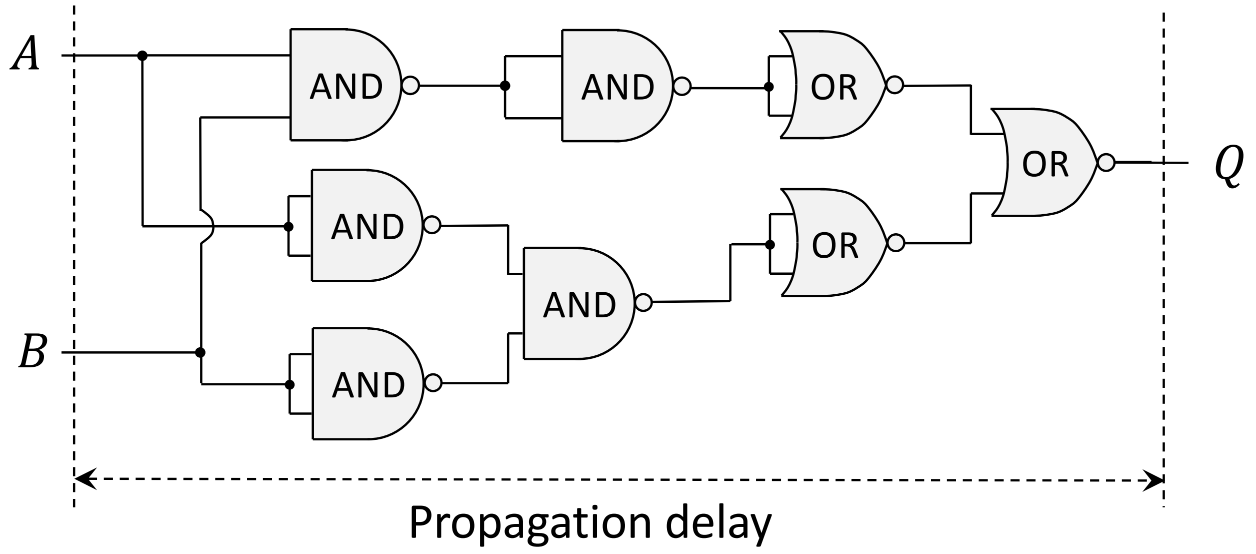

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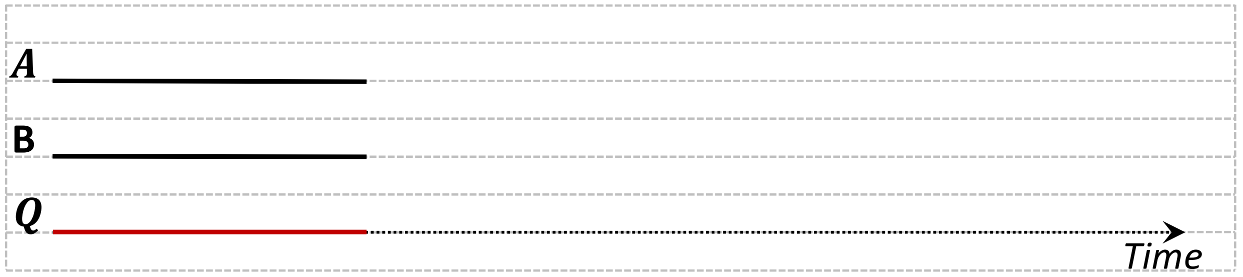

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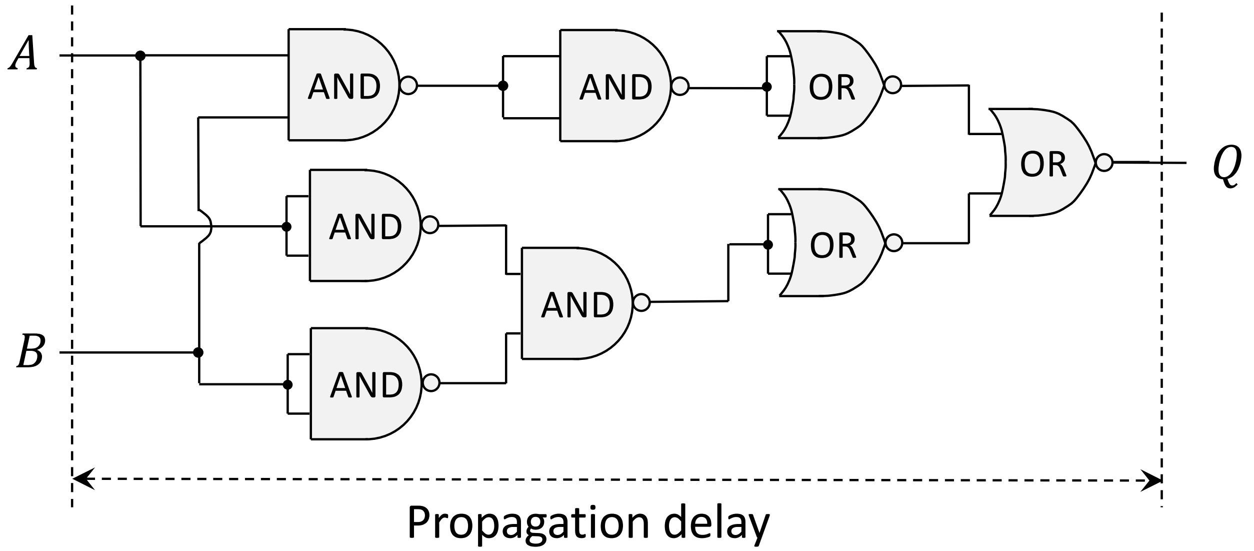

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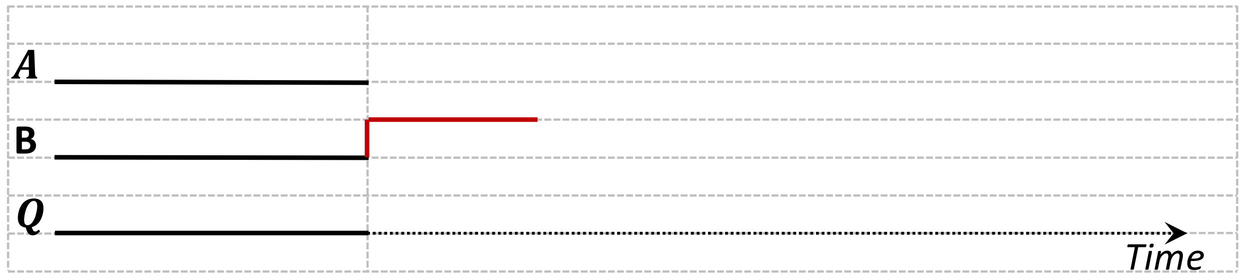

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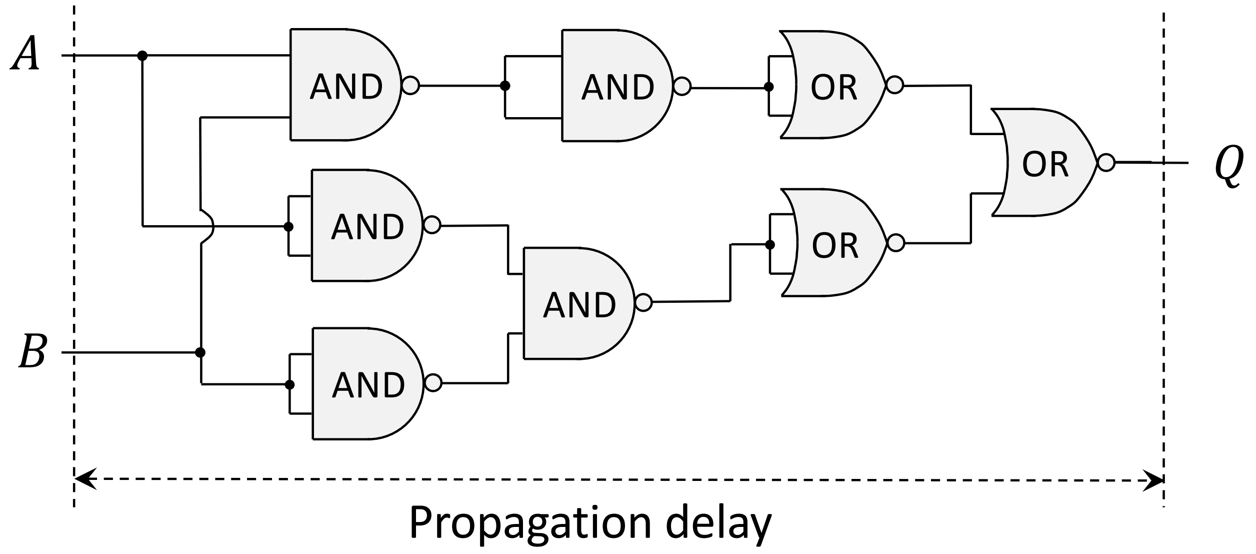

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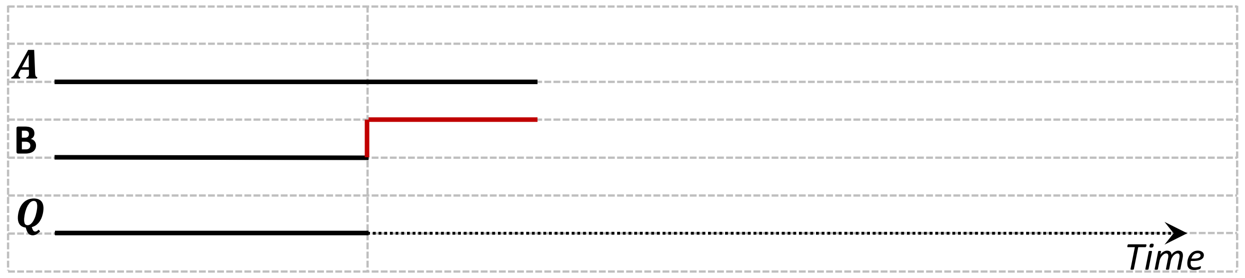

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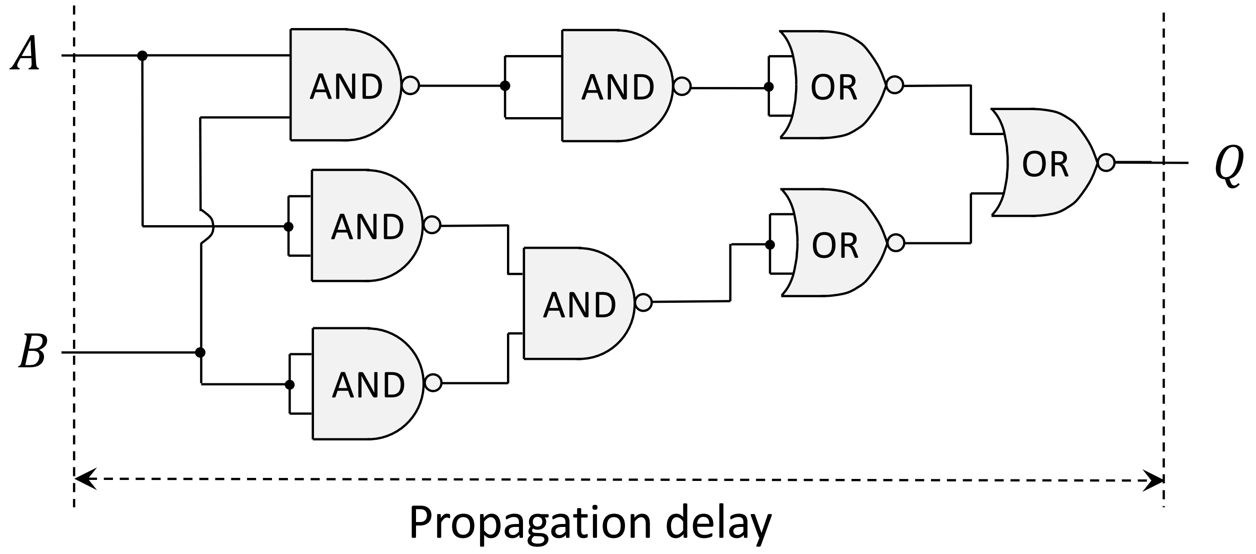

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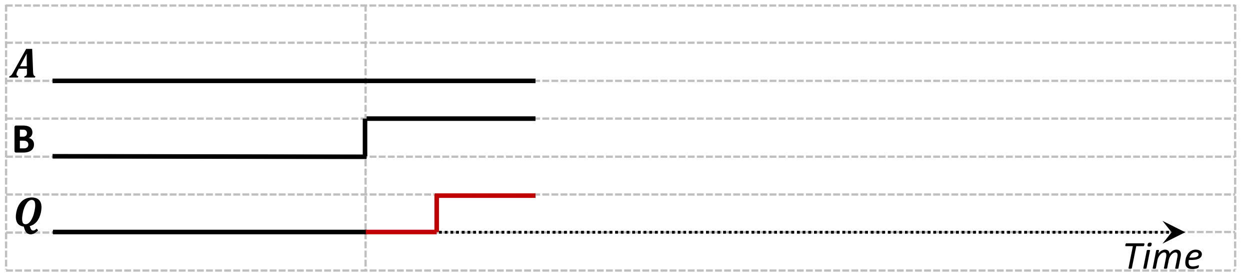

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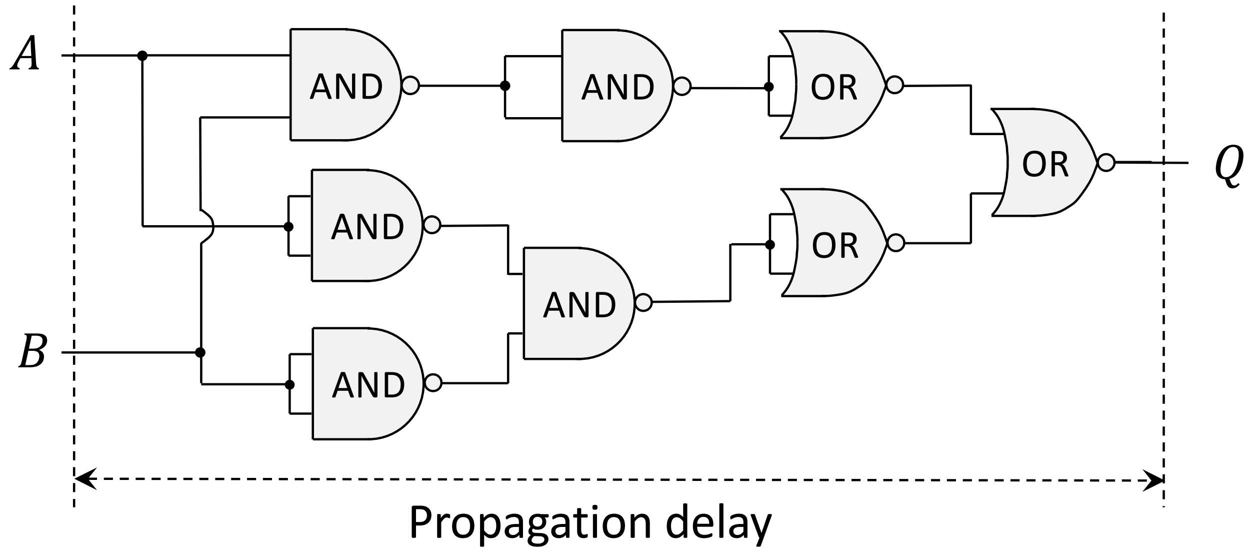

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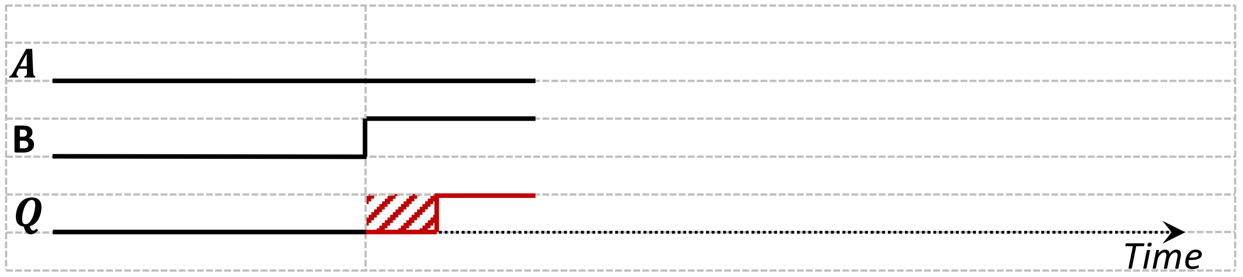

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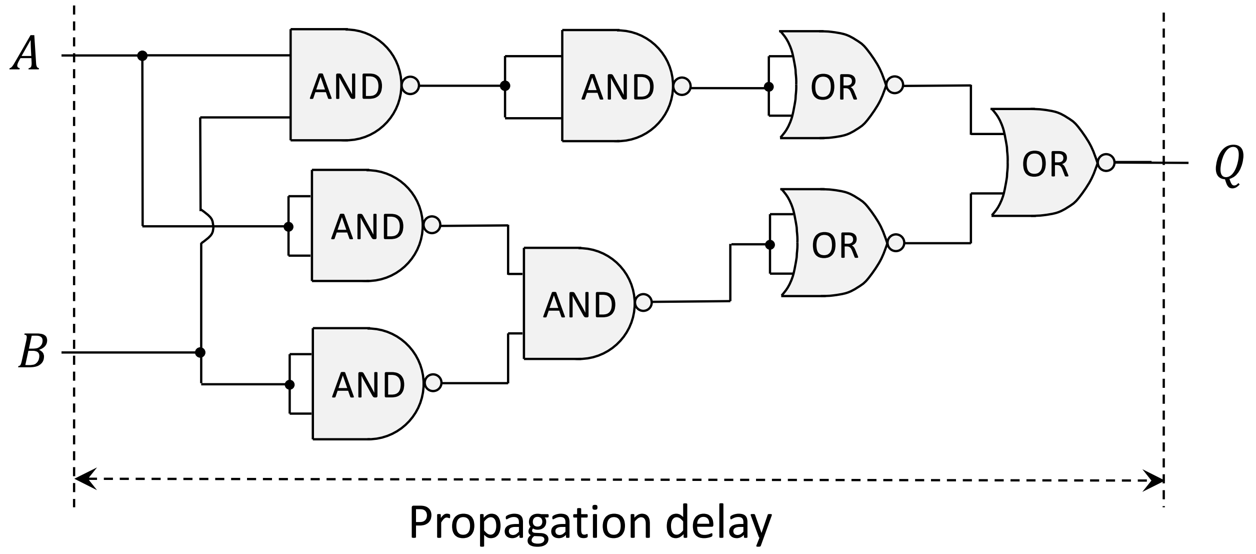

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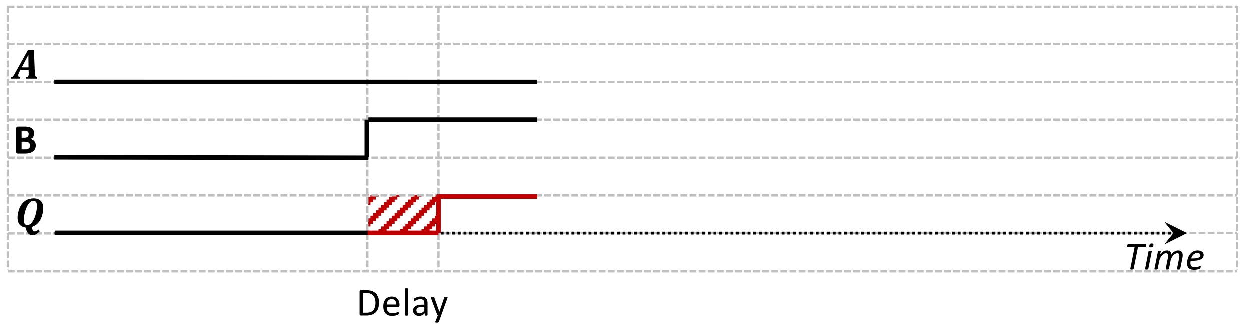

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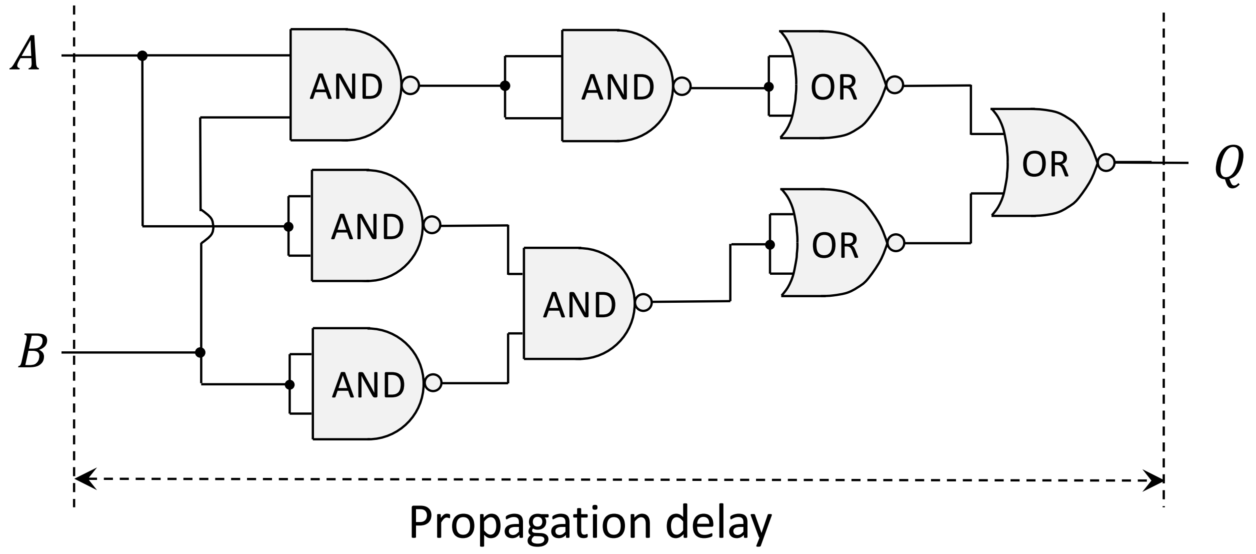

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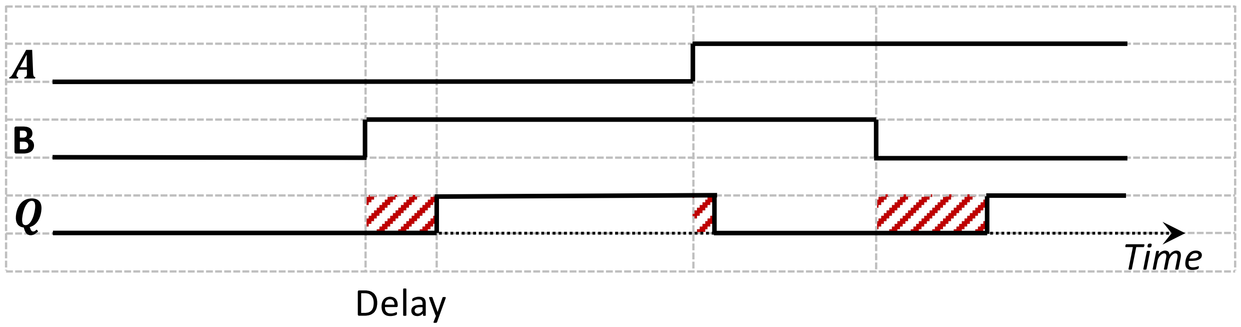

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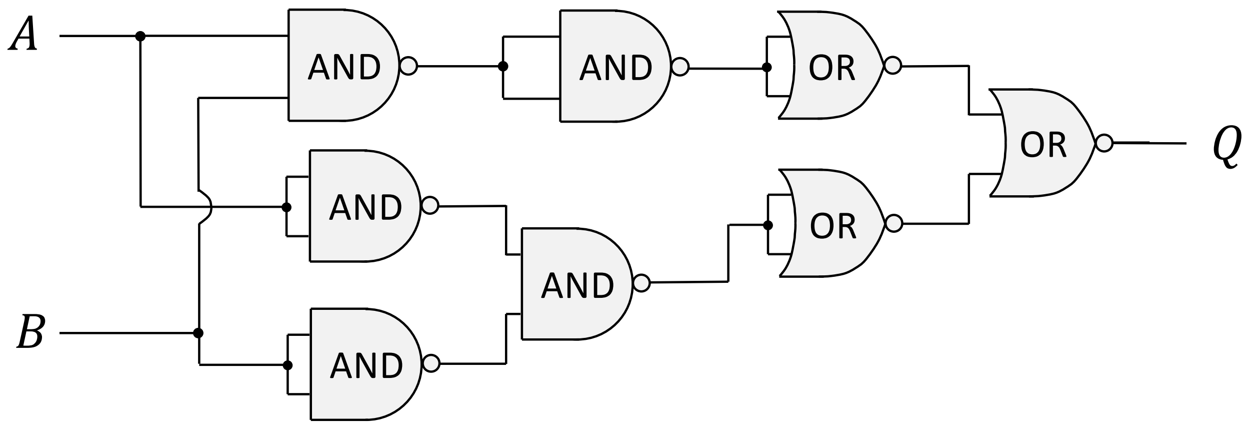

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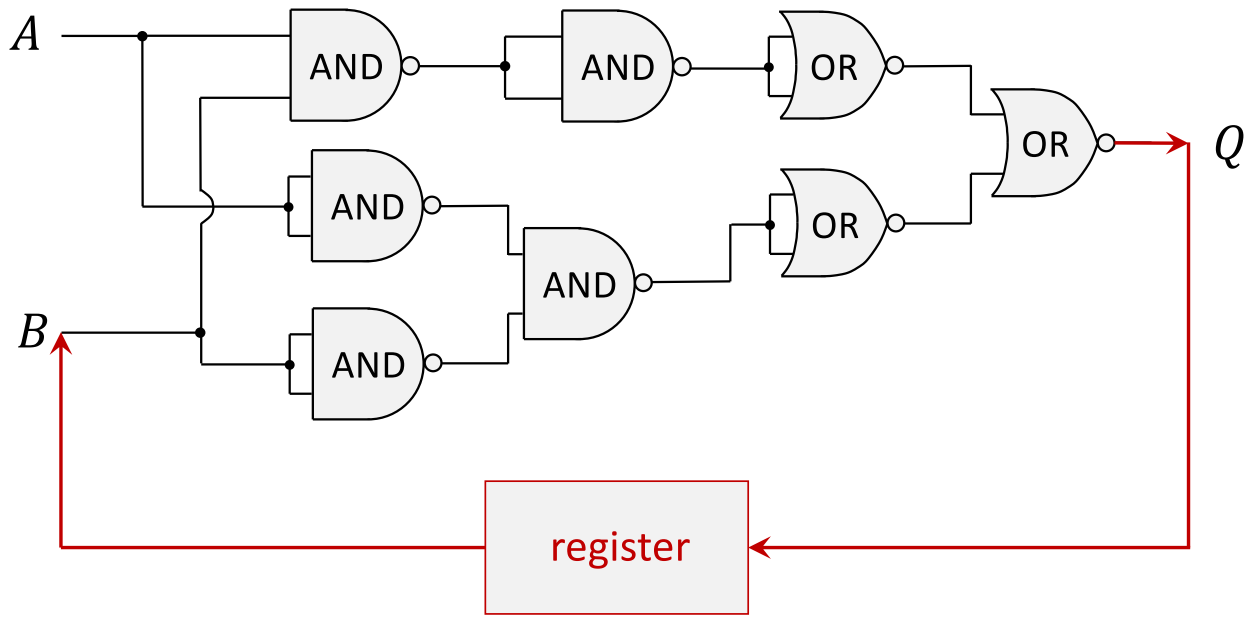

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Sequential circuits – an alternative to combinational

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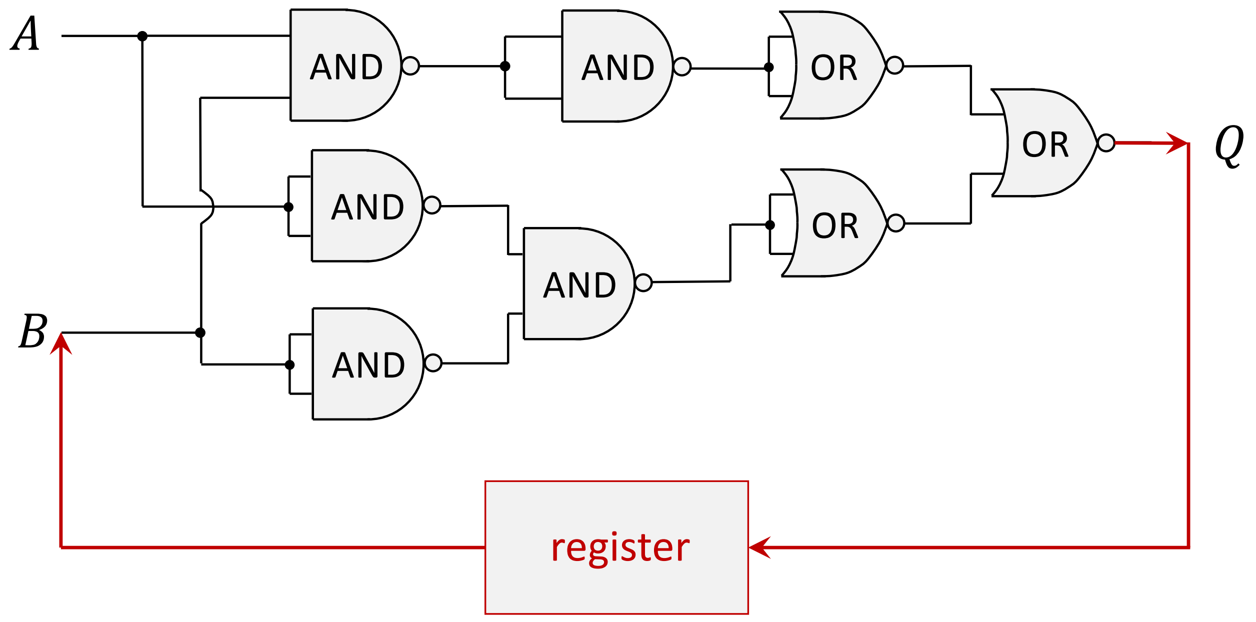

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Sequential circuits – an alternative to combinational

Register (from “to register” = “to remember”) – a memory element, to store electrical signal

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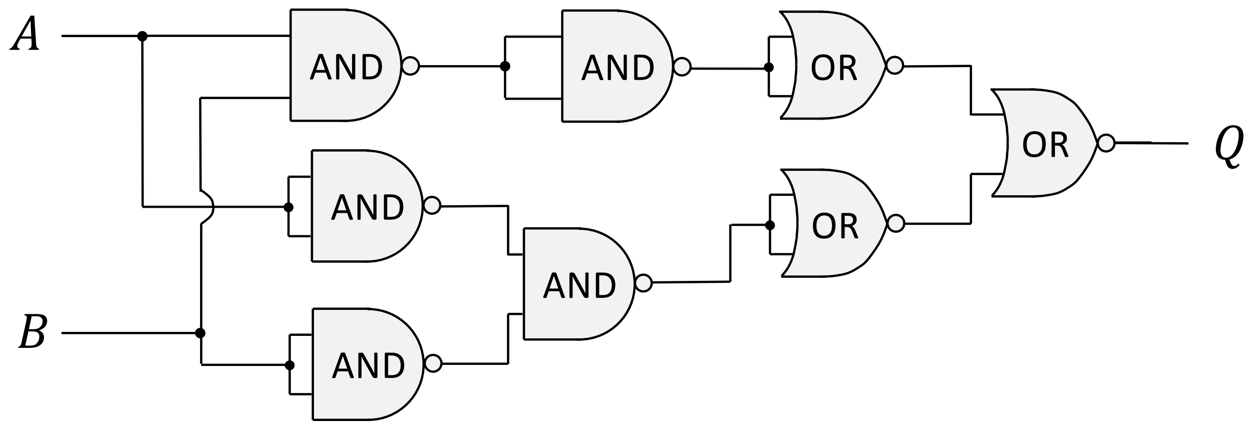

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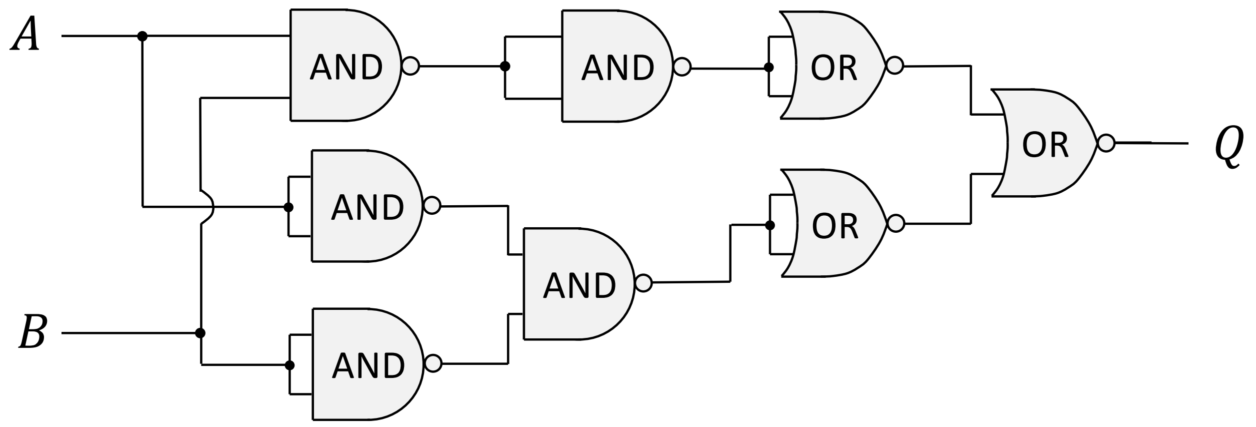

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Key advantage: Fast (thus, used in such components, as processor ALU)

Key disadvantage: No support of inputs synchronization (will be discussed later)

Implementation of Arithmetic Operations in Computers

Key principles:

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Boolean Function Implementation: Key Results from Discrete Math

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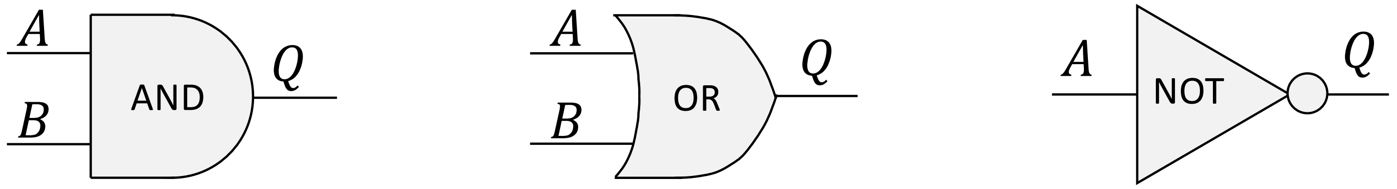
Any Boolean function can be implemented by using only one out of these sets of logic gates:

1) AND, OR, NOT



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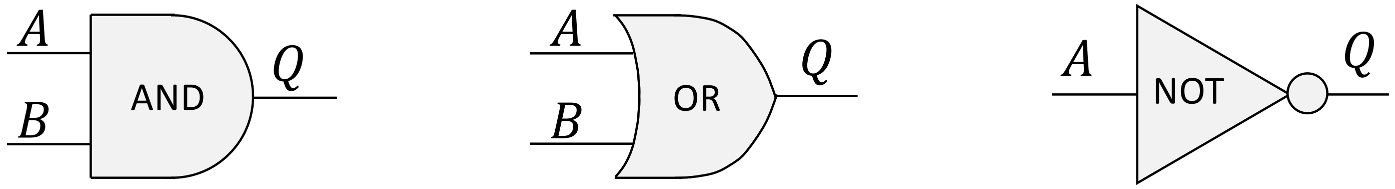
1) AND, OR, NOT These is the basis:

If some of these logic gates is removed, some functions are not implementable



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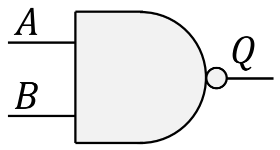

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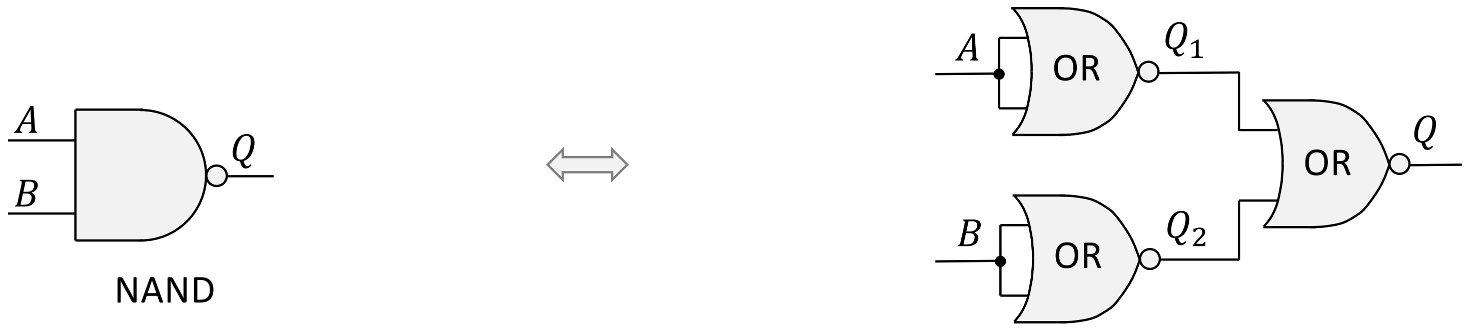

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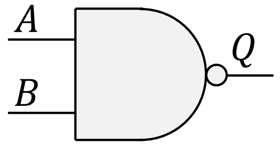

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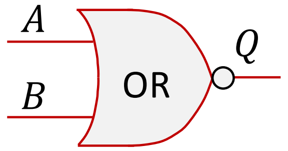

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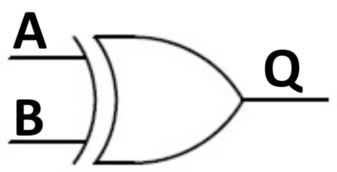

+ “1”

There is a notion of hardwired “1” or “0”

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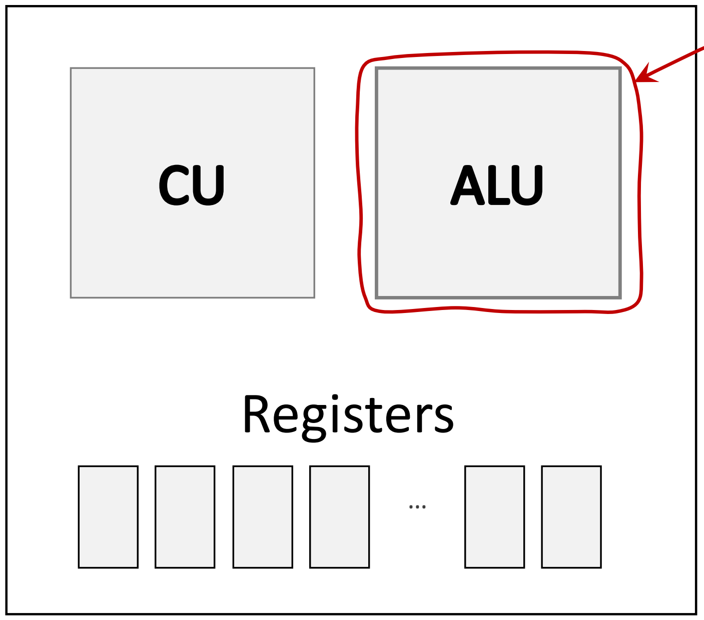
Zhegalkin polynomial – another interesting result

Types of Logic Circuits for CPU Components



Combinational logic circuit for arithmetical and logic operations

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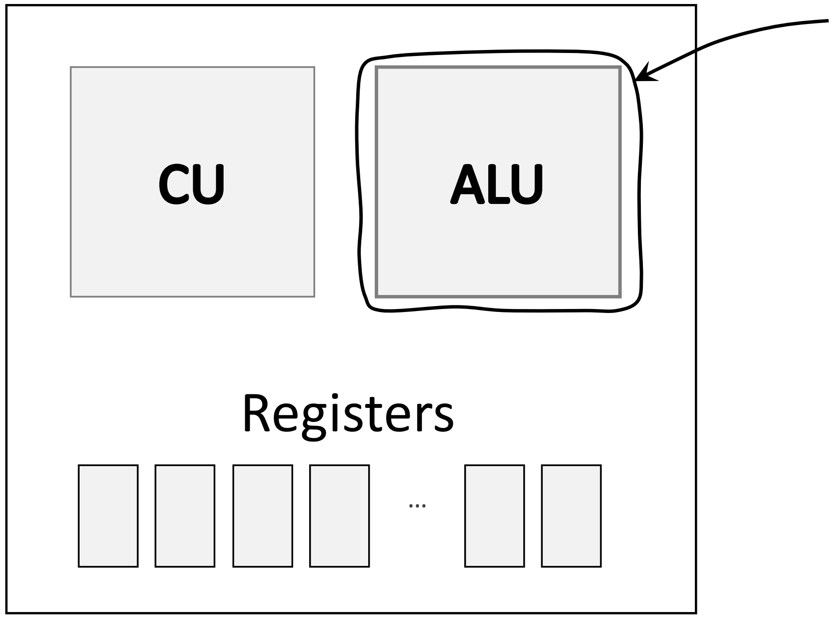

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Fast - advantage

No synchronization support - disadvantage

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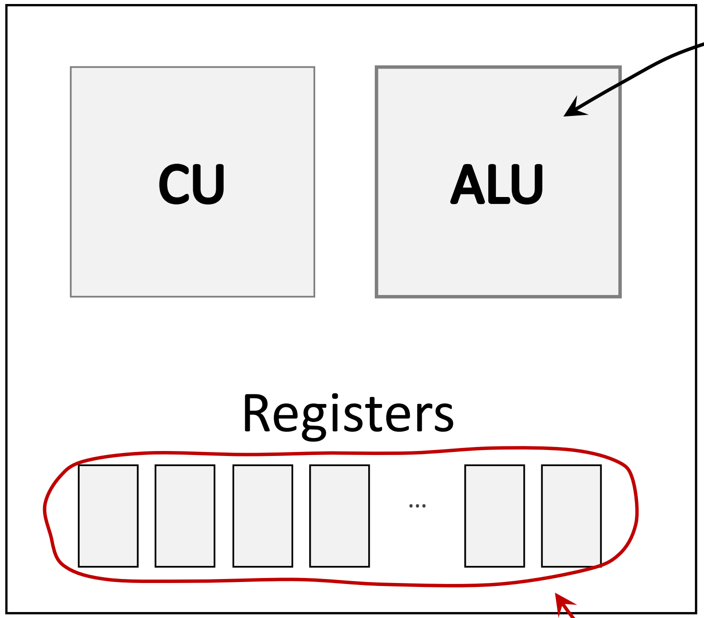

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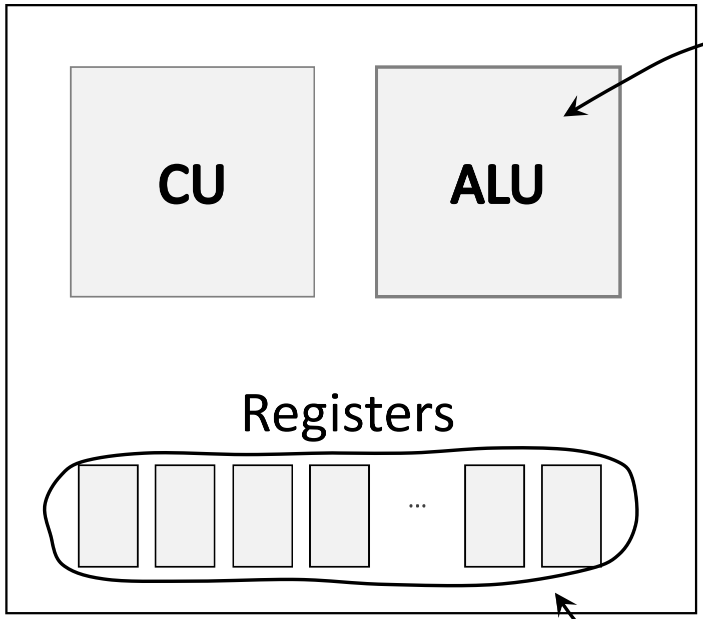

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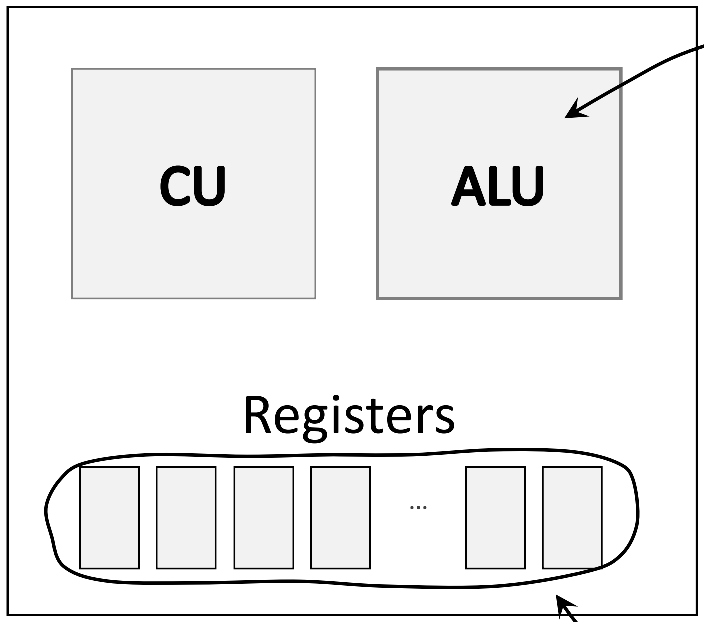

Combinational logic circuit for arithmetical and logic operations

Fast - advantage

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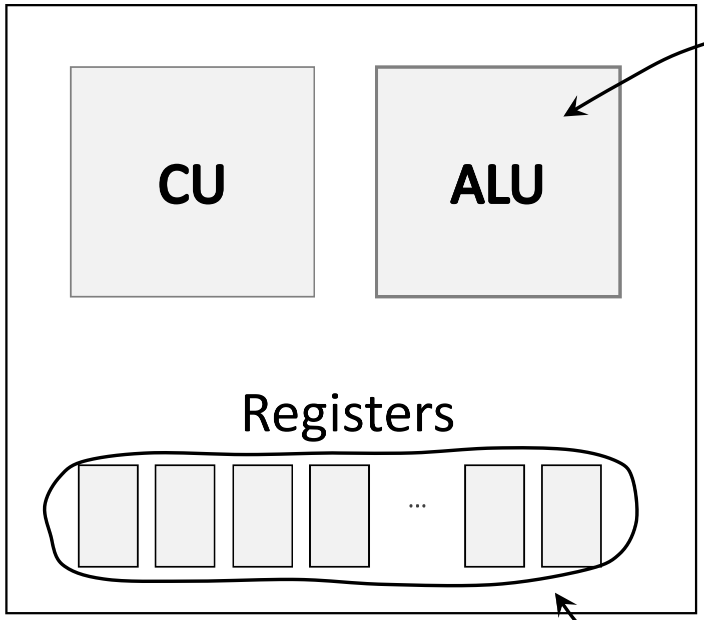
Sequential logic circuits (clocked)

1) Capture inputs (might arrive not simultaneously);
2) Store inputs until a certain time instant;

Types of Logic Circuits for CPU Components



Combinational logic circuit for arithmetical and logic operations

Fast - advantage

No synchronization support - disadvantage

Sequential logic circuits (clocked)

1) Capture inputs (might arrive not simultaneously);
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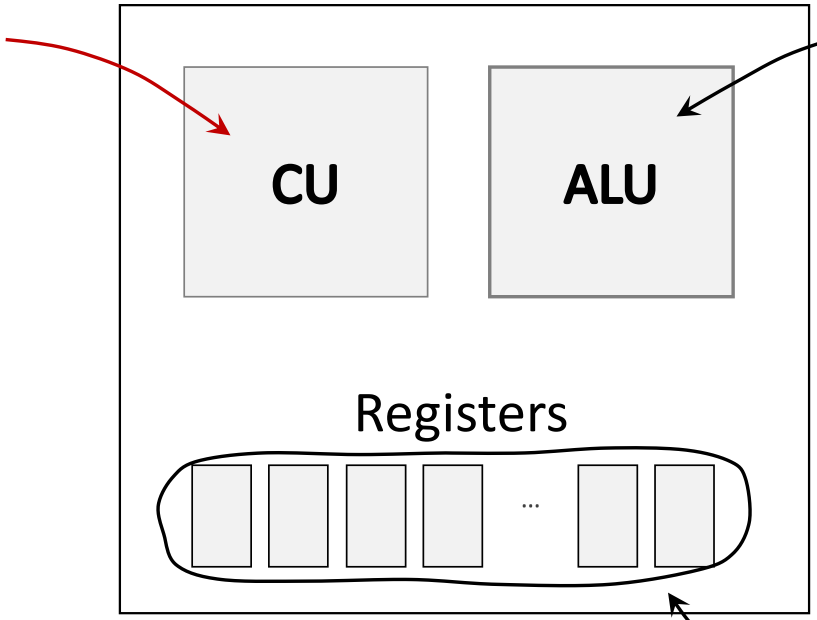
Types of Logic Circuits for CPU Components

Not a pure combinational circuit

(for example, typically has IR – instruction register)



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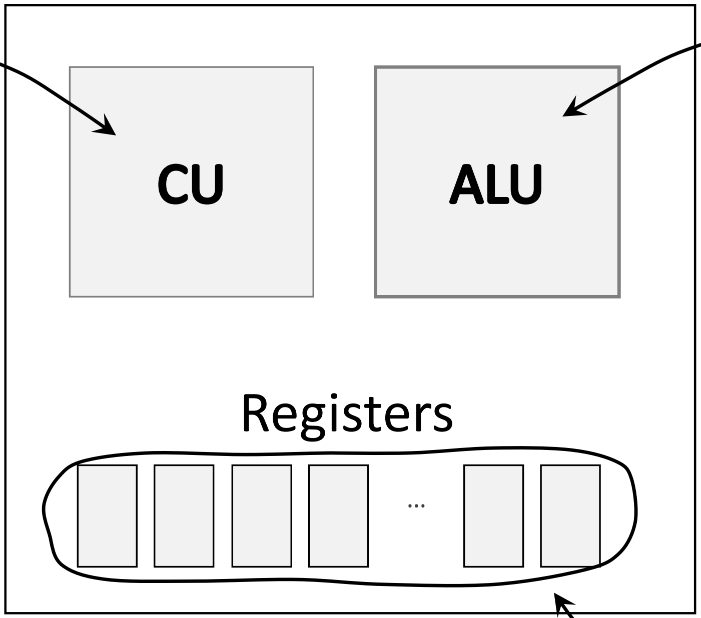
Recall Instruction Fetch (IF) stage of a pipelined execution for instructions



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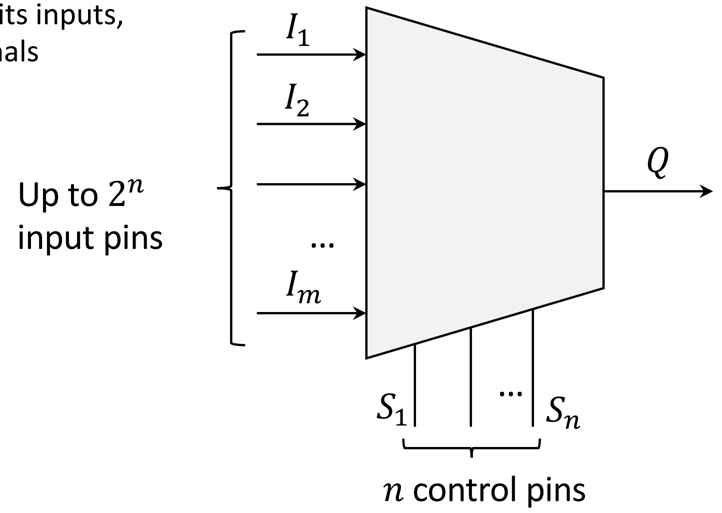
Key Hardware Building Blocks for Combinational Circuits

1) Multiplexer
2) Demultiplexer
3) Decoder
4) Encoder

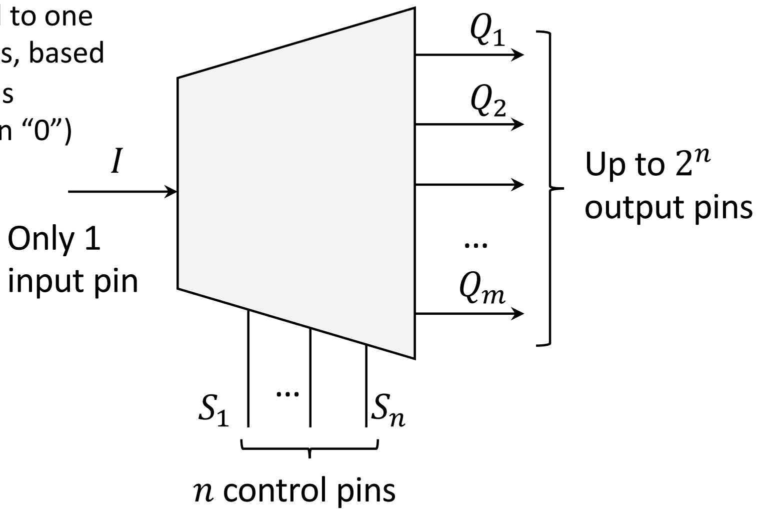
Multiplexor

Sets output to one of its inputs, based on selector signals



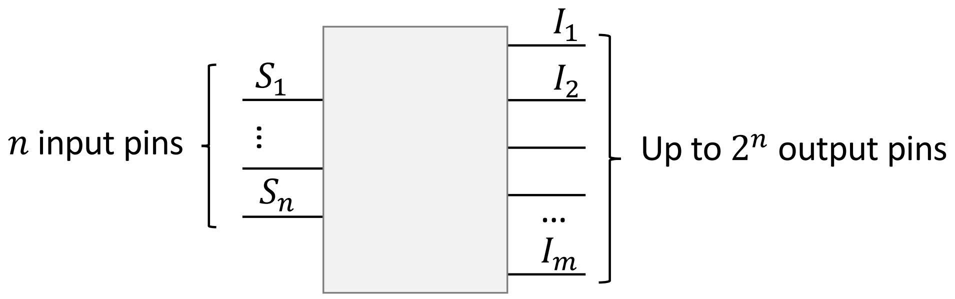
Demultiplexor

Forwards input signal to one of its multiple outputs, based on the selector signals (other outputs remain "0")



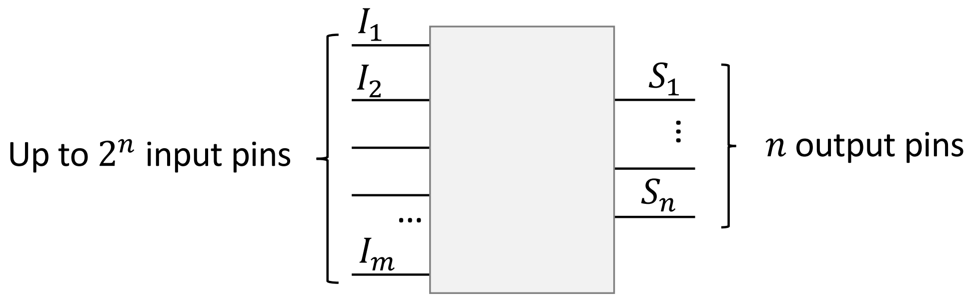
Decoder

Sets to "1" exactly one output pin, which corresponds to the signals of input pins;
All other pins are set to "0"



Encoder

The opposite function of a decoder;
Only one output pin is set to "1", while all others – "0"



Key Hardware Building Blocks for Combinational Circuits

1) Multiplexer
2) Demultiplexer
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These circuits are generously used in the implementation of real hardware, such as the main system memory, ALU, etc.

Sample Use Case for Multiplexer: ALU Implementation (An Oversimplified Concept)

ALU (Arithmetic Logic Unit) – the part of CPU to implement arithmetic and logic instructions

Let our ALU support 4 instructions: “+”, “-”, “*”, “/”

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Circuit for “+”

Circuit for “-”

Circuit for “*”

Circuit for “/”

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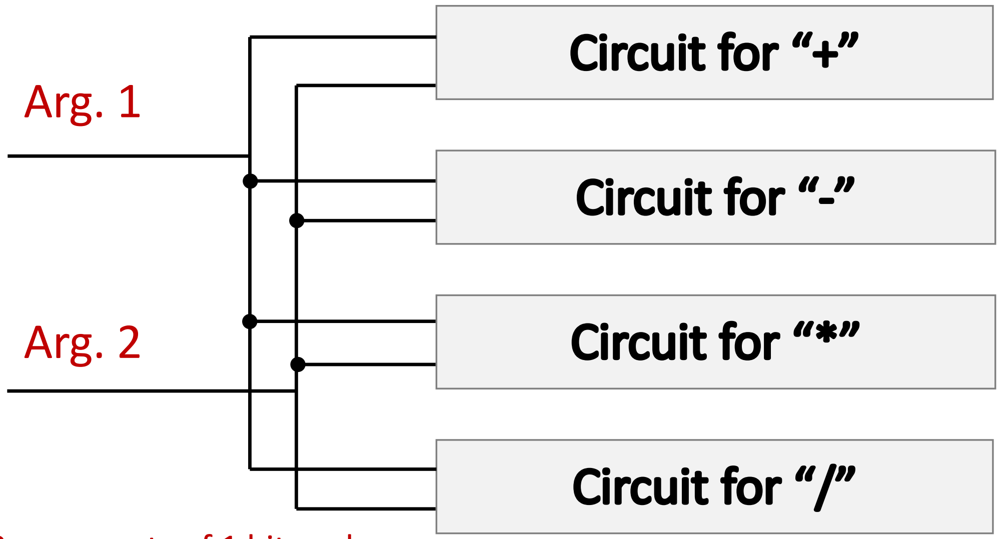

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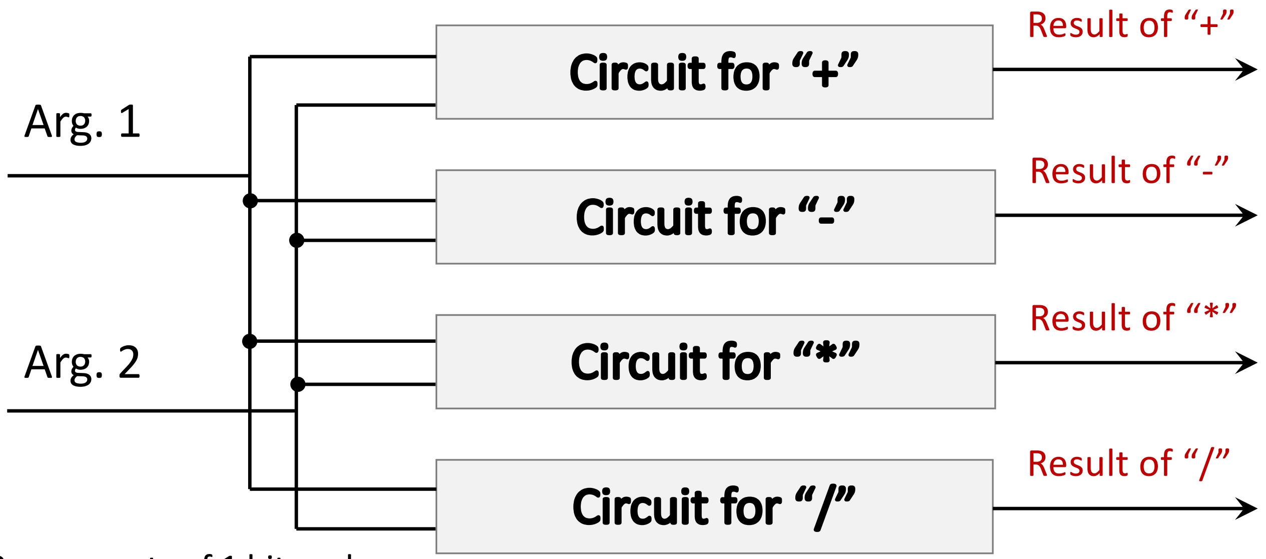

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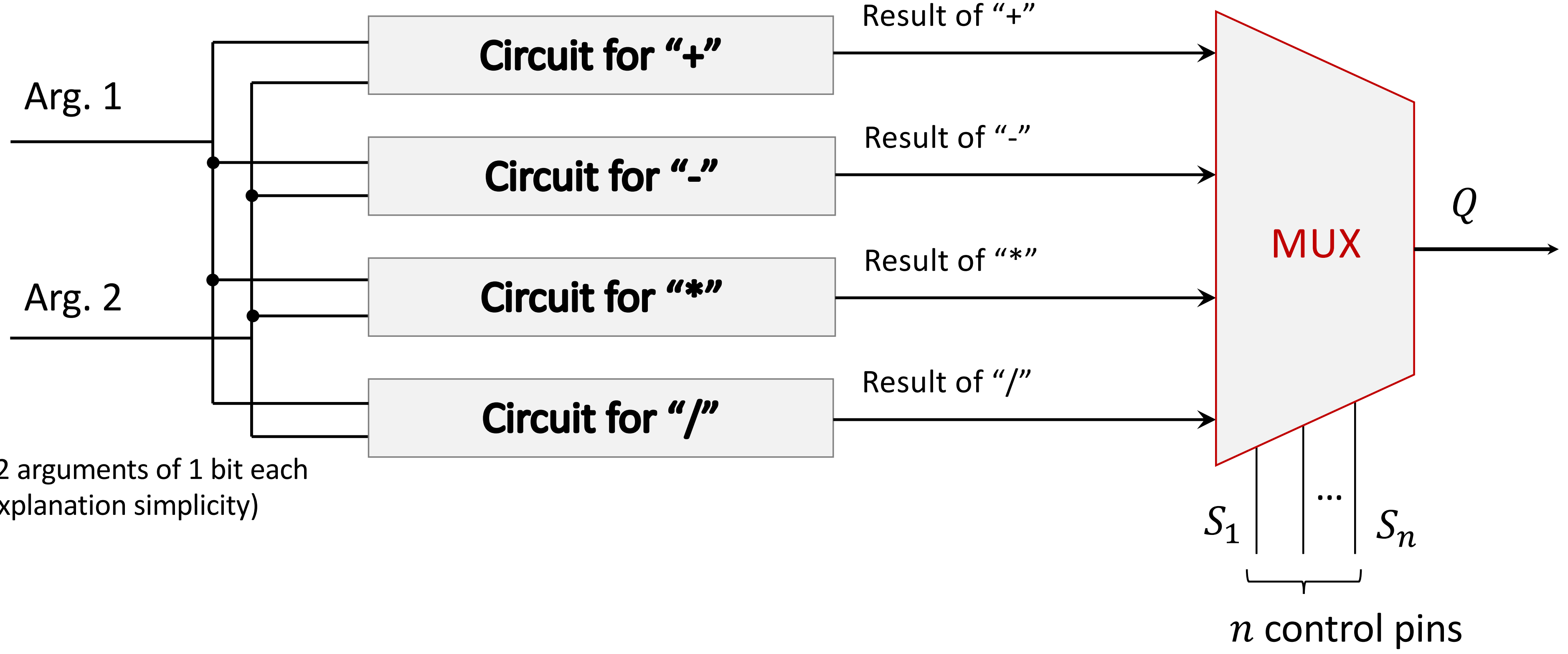

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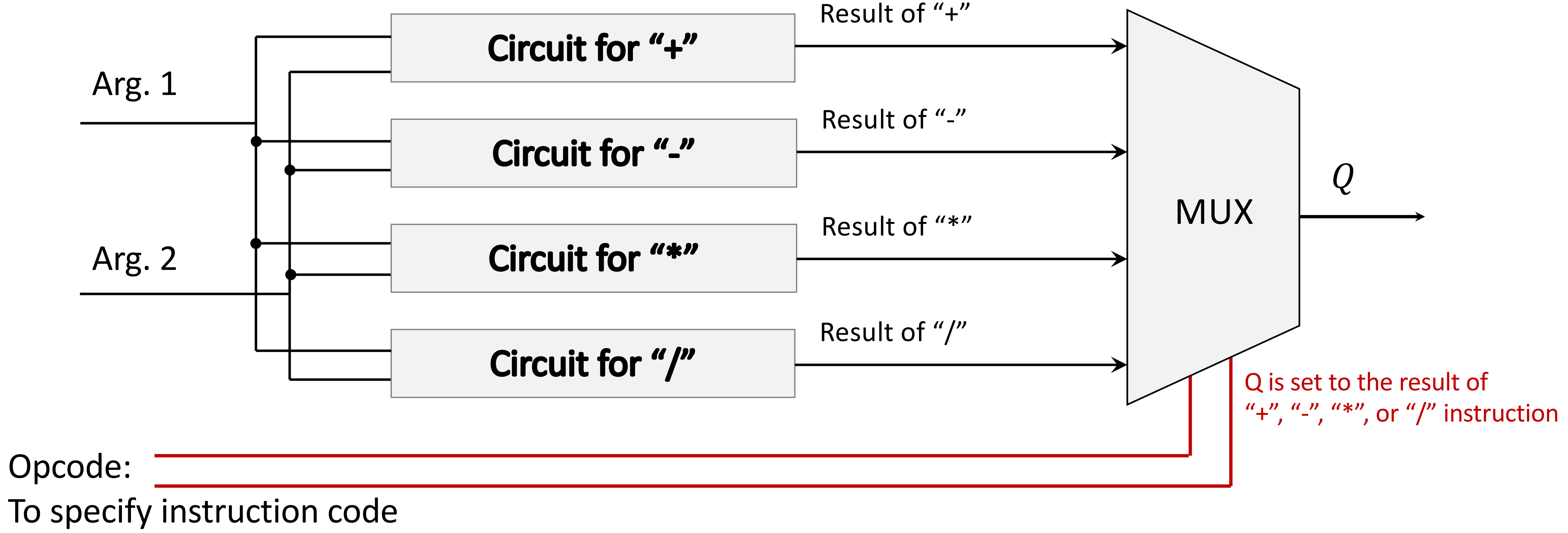

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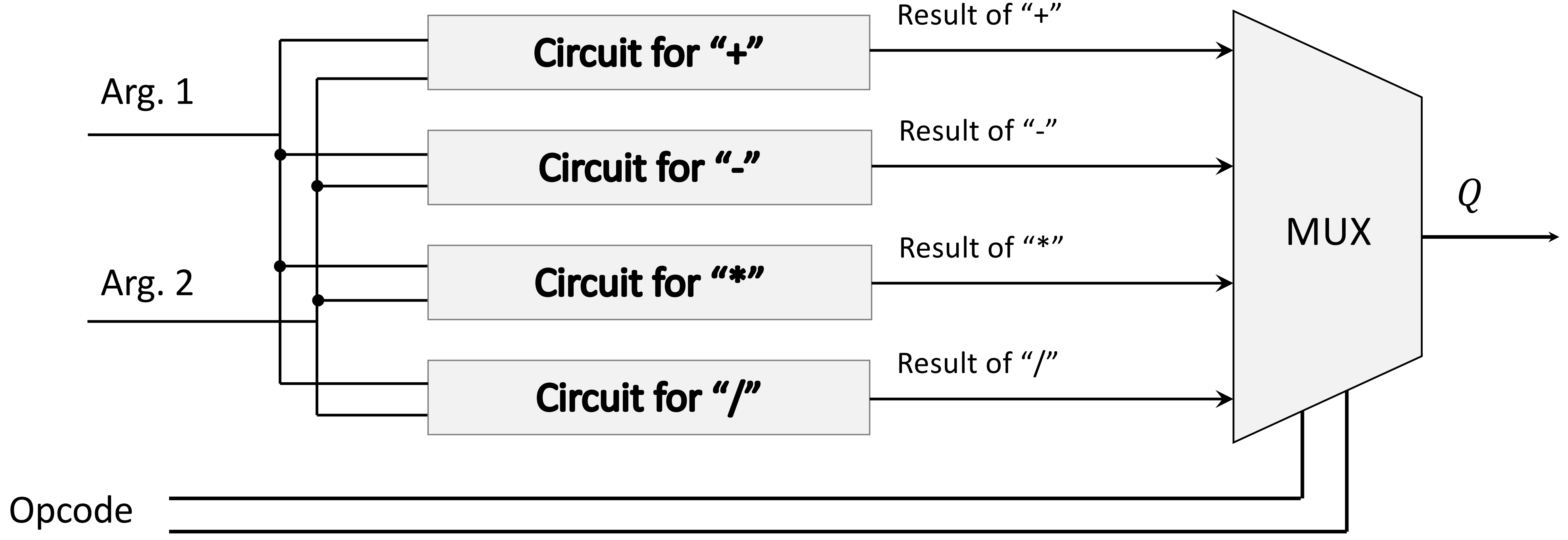

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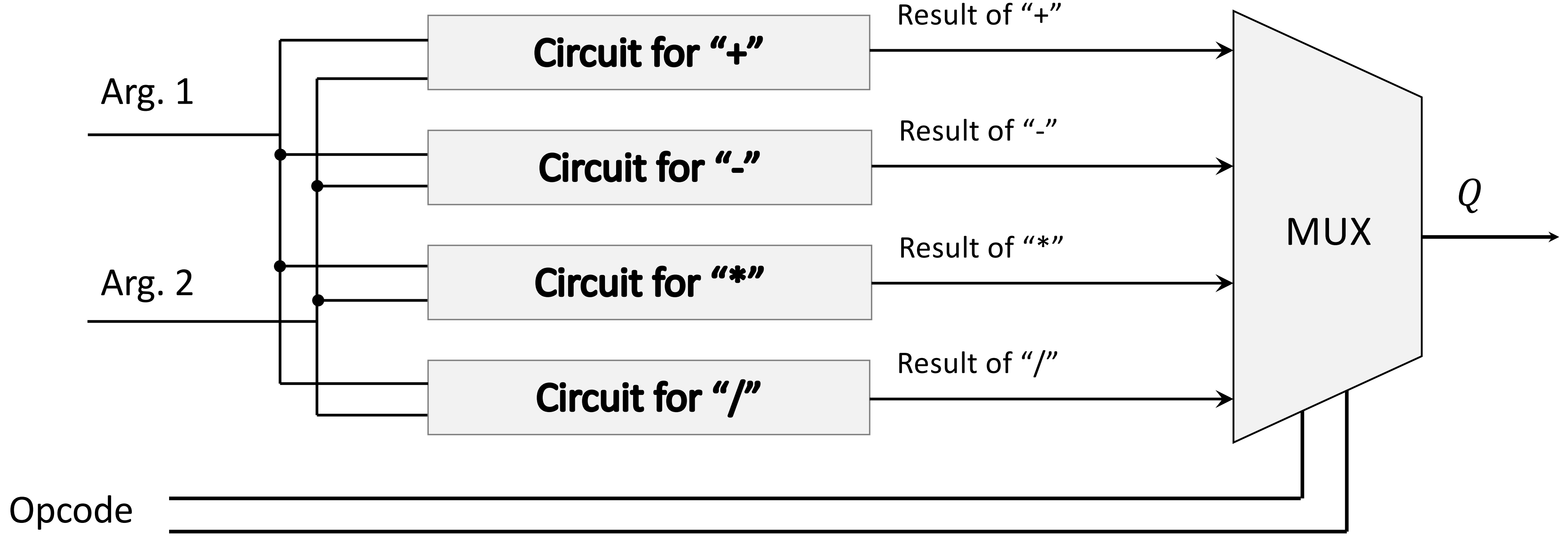

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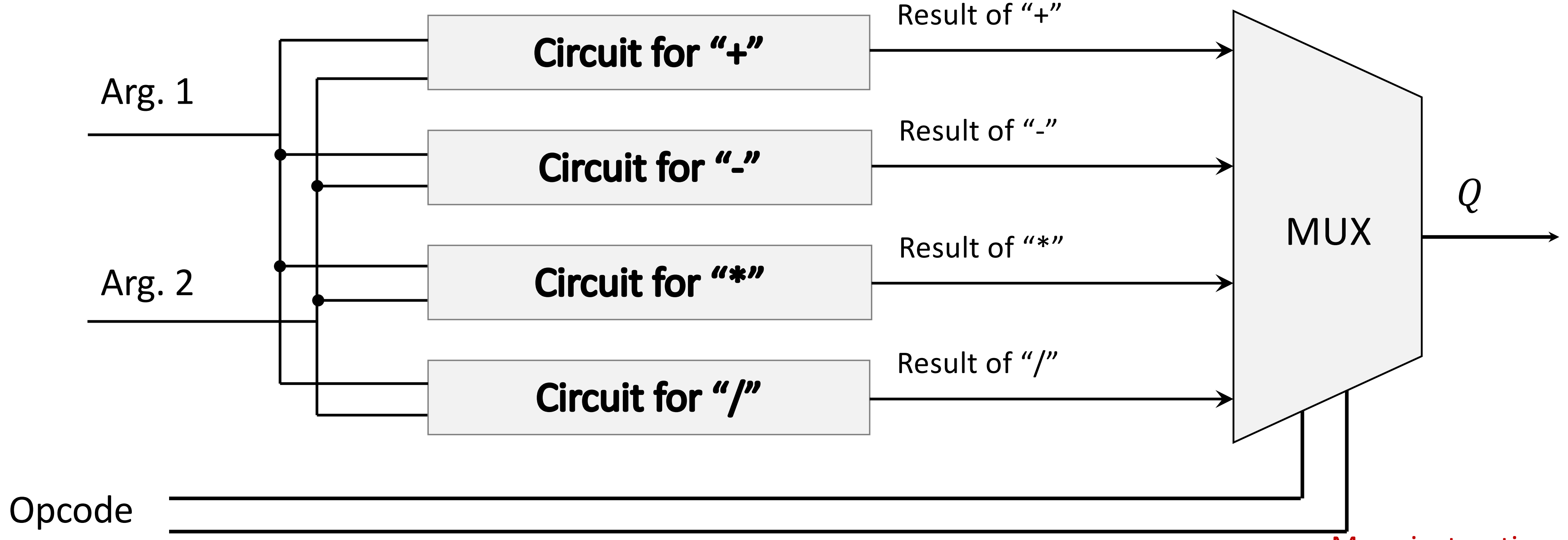

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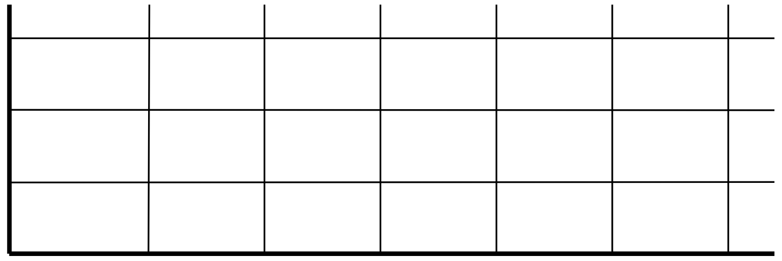
For this example, the longest instruction must complete within 1 CPU clock cycle

More instructions supported is not necessary better (recall RISC vs. CISC designs)

Sample Use Case for Demultiplexer: Memory Addressing (Simplified View)

Memory Unit –

a set of memory cells
(each cell has its address)



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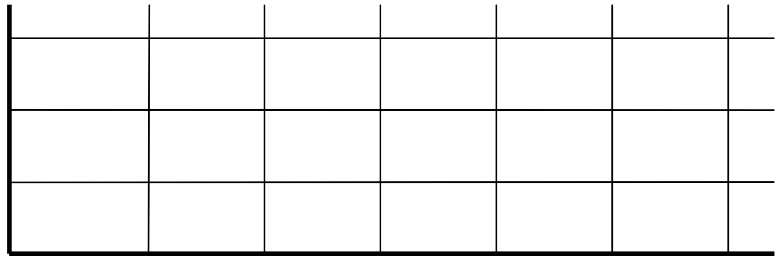

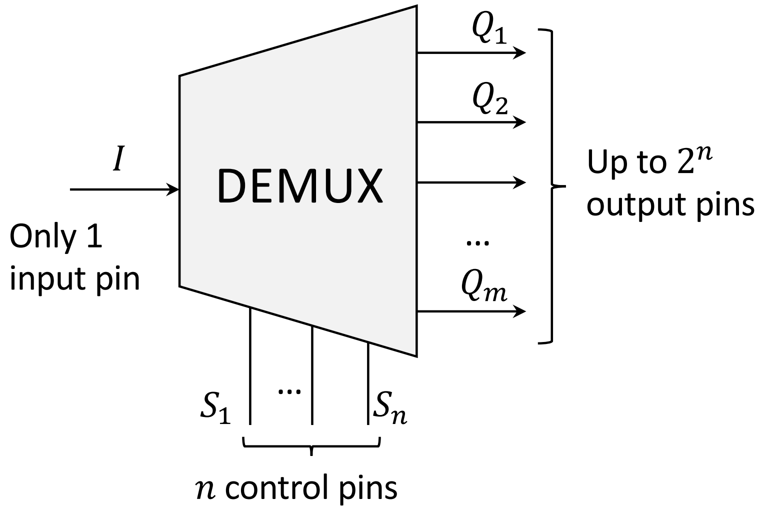

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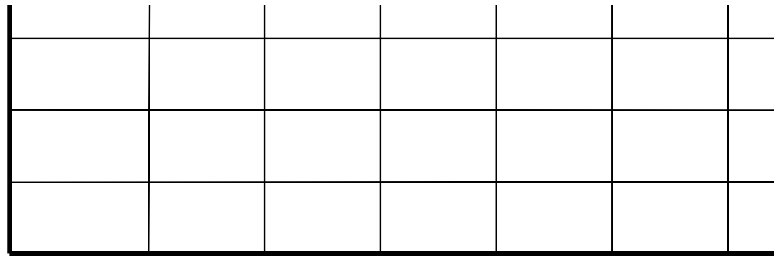

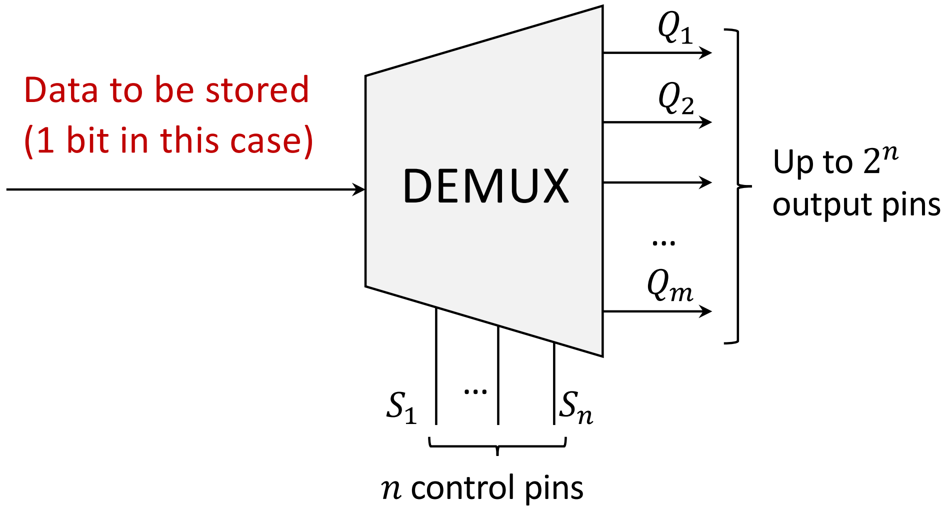

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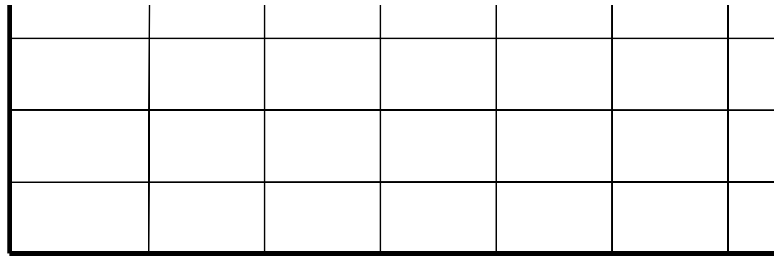

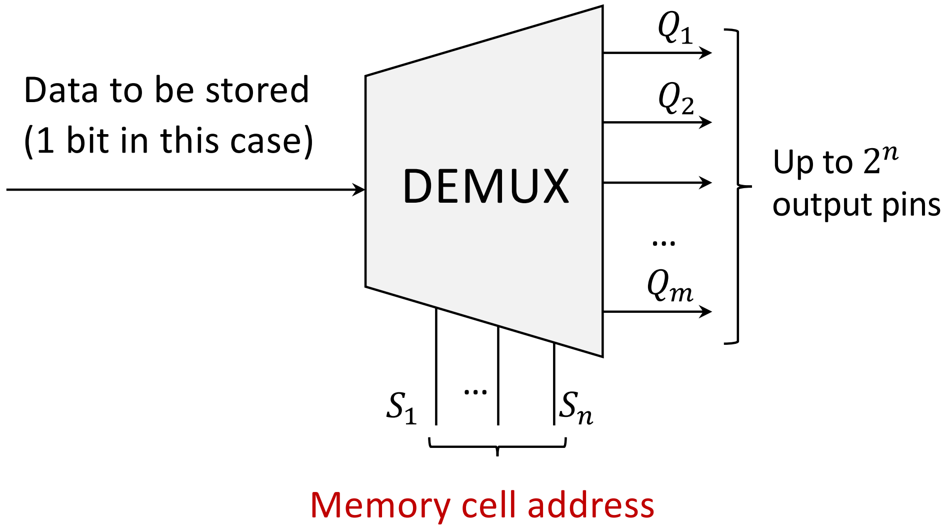

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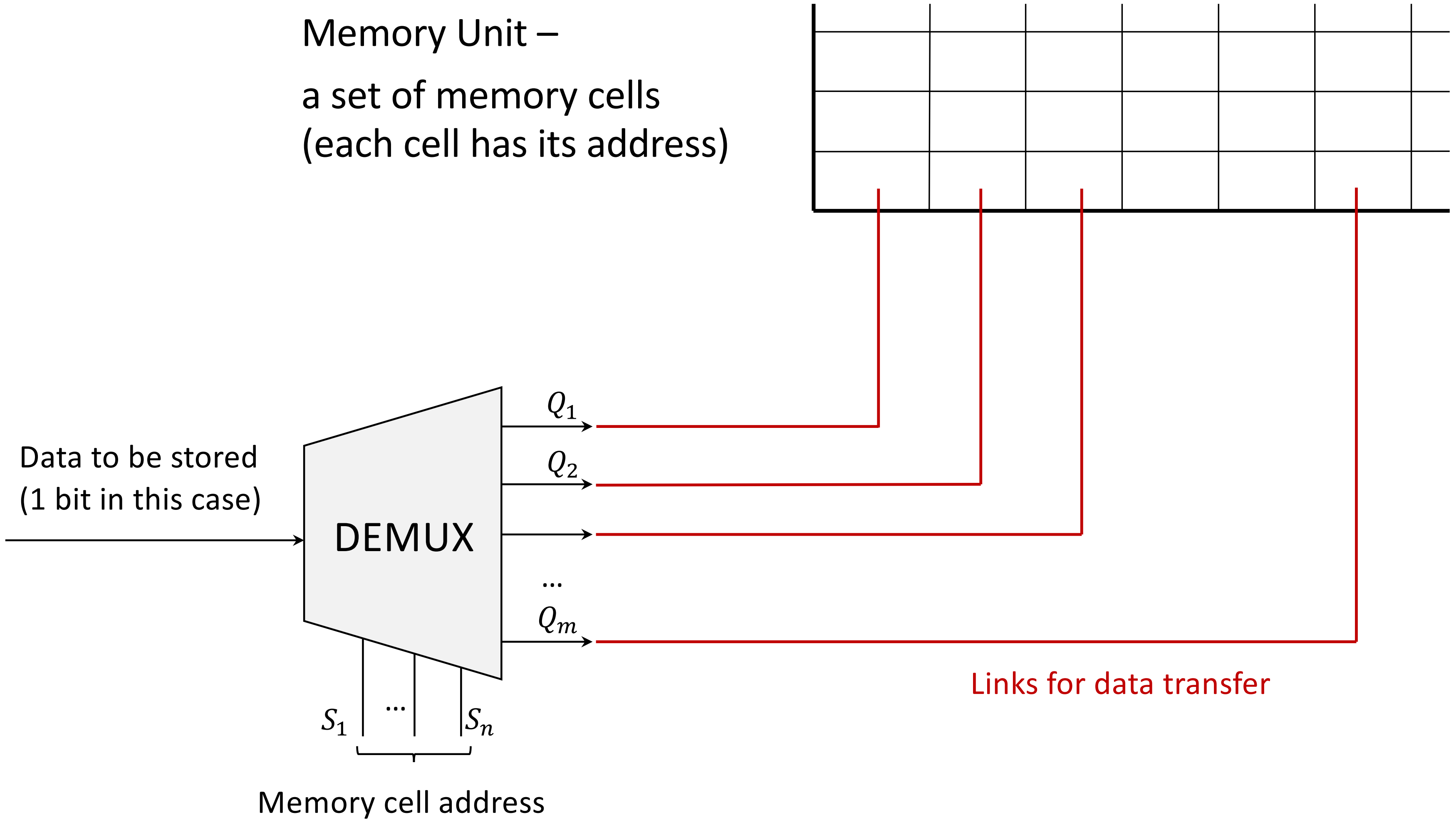

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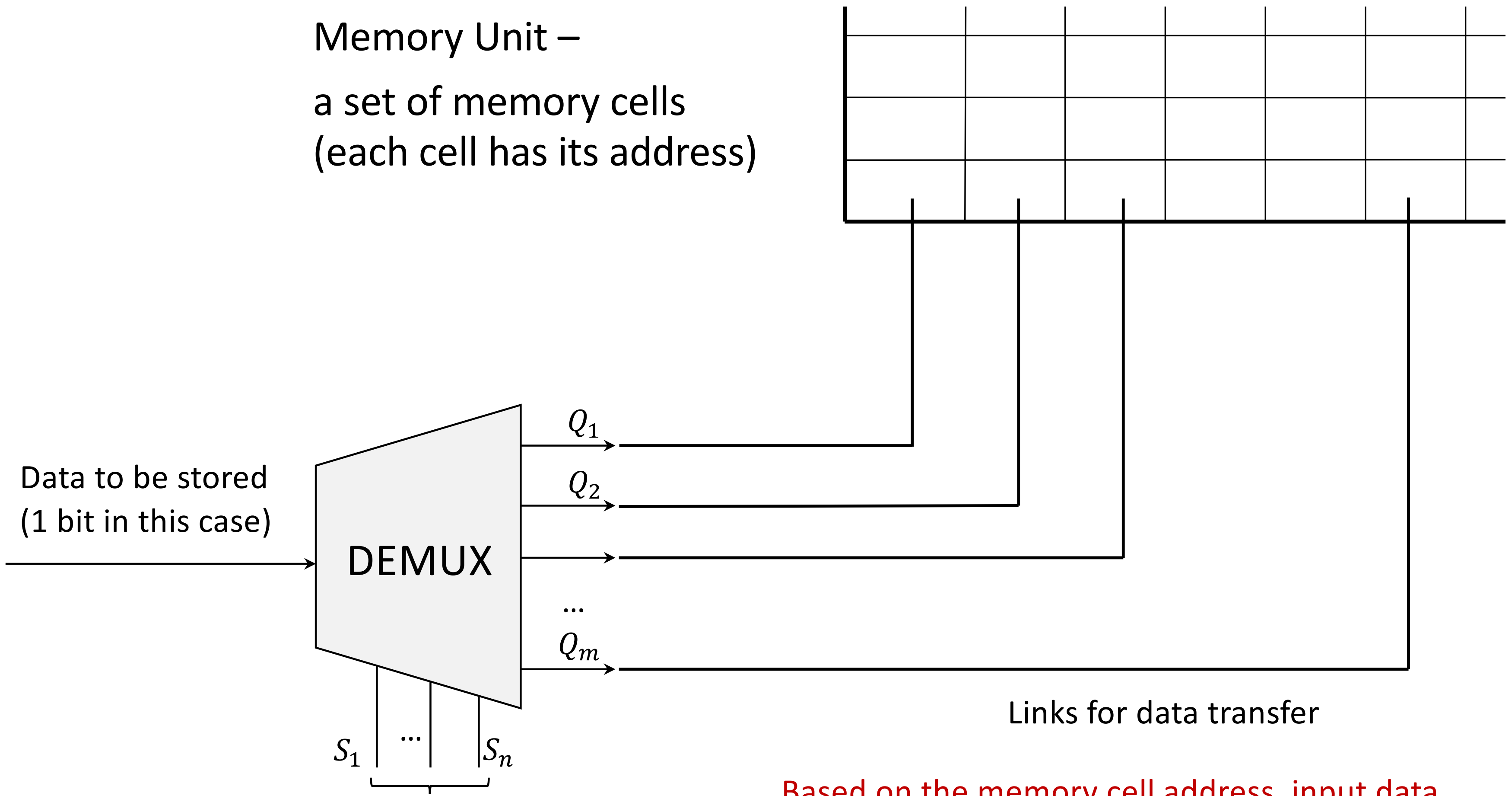

Memory cell address

Based on the memory cell address, input data is propagated to one of the memory cells

Sample Use Case for Demultiplexer: Memory Addressing (Simplified View)

Memory Unit –

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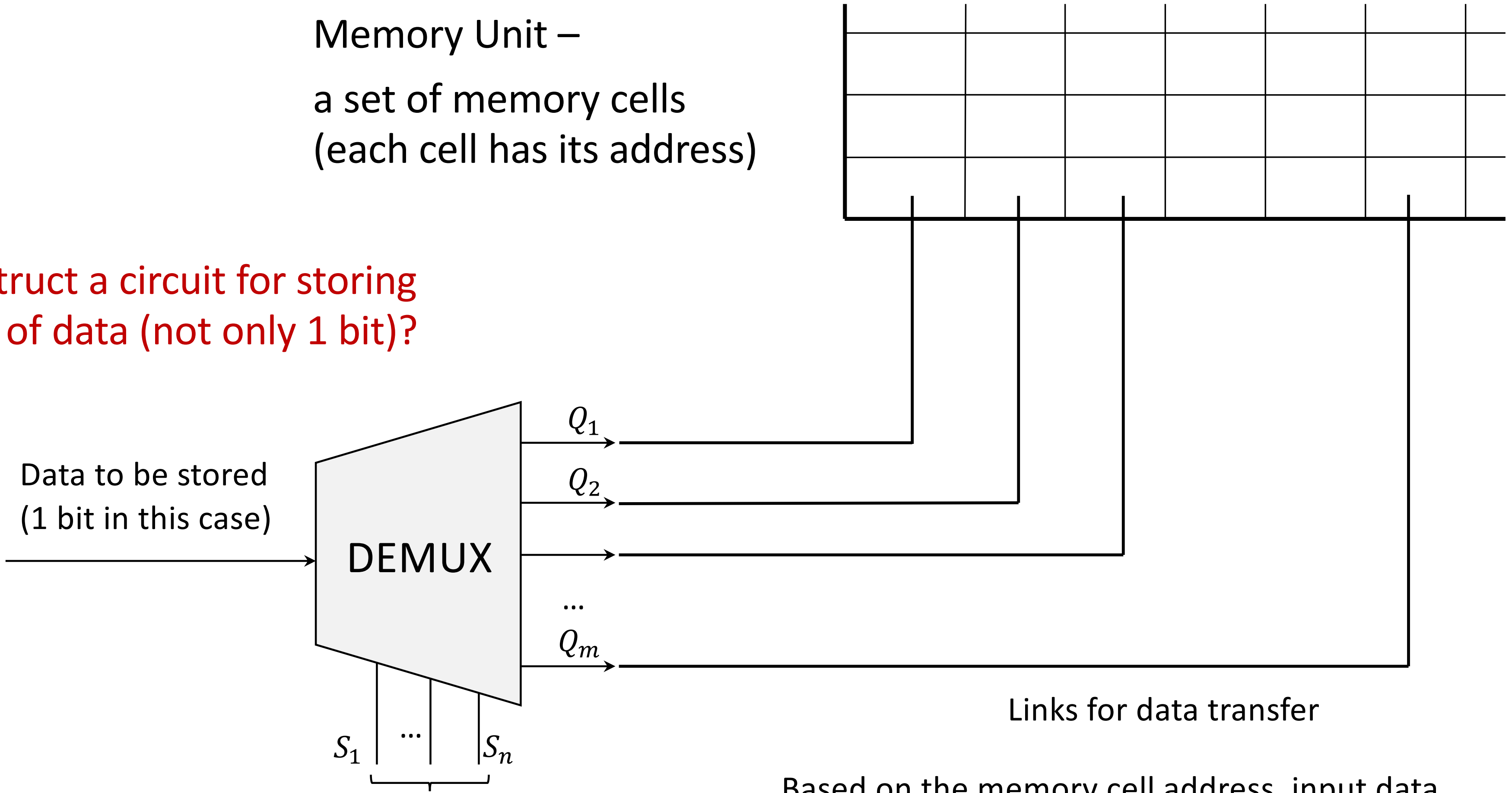
Question:

How to construct a circuit for storing multiple bits of data (not only 1 bit)?



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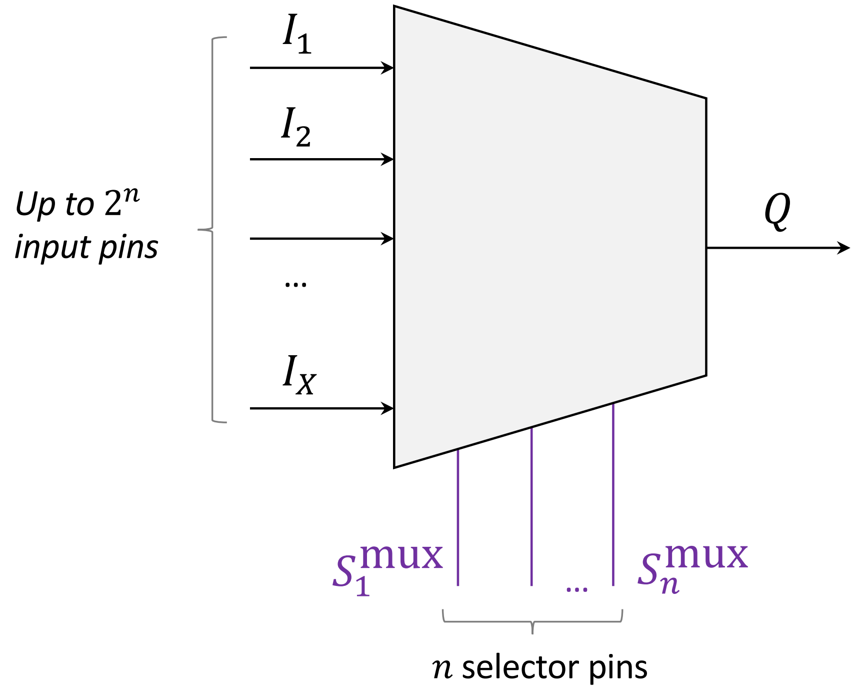
X-to-1 Multiplexer

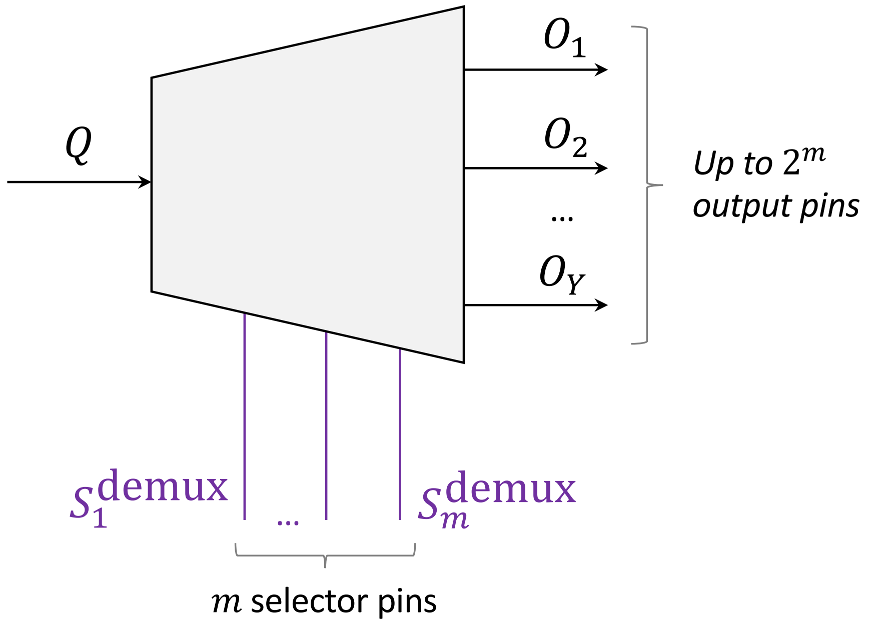
Based on the values of its n selector (control) pins, a multiplexer sets the value of its output Q to the value of one of its $X \leq 2^n$ inputs



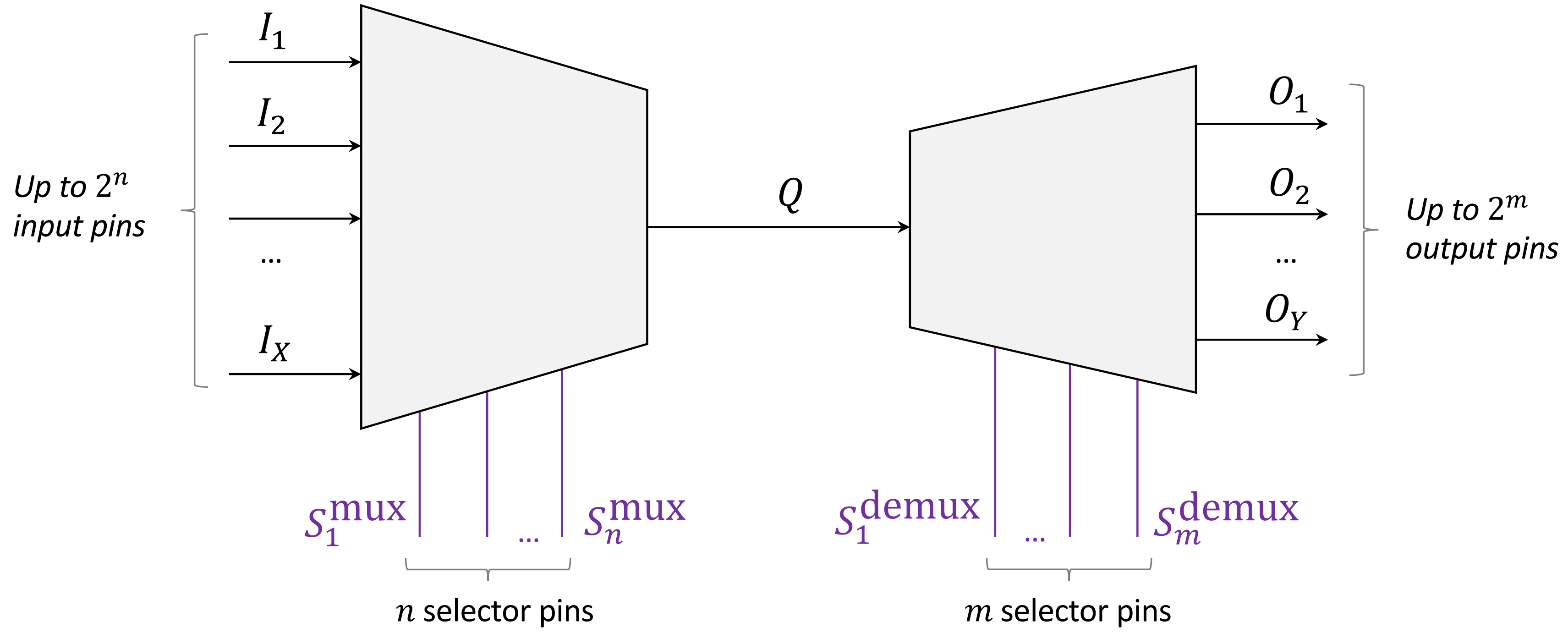
Question: How to construct an X-to-Y Multiplexer?

1-to-Y Demultiplexer

Based on the values of its m selector pins, a demultiplexer outputs its input value Q at one of its $Y \leq 2^m$ output pins, while all other output pins are set to 0s

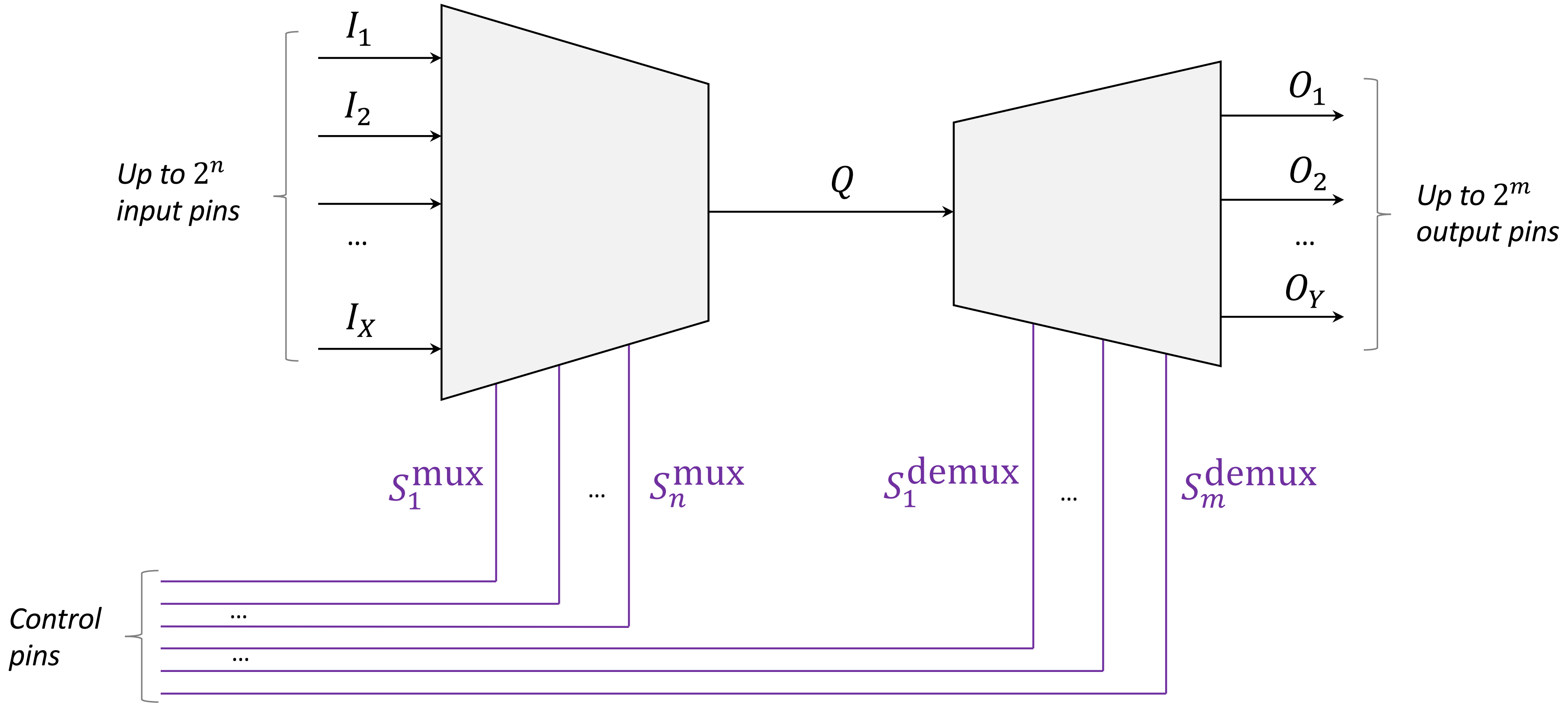


Multiplexer-Demultiplexer Composition

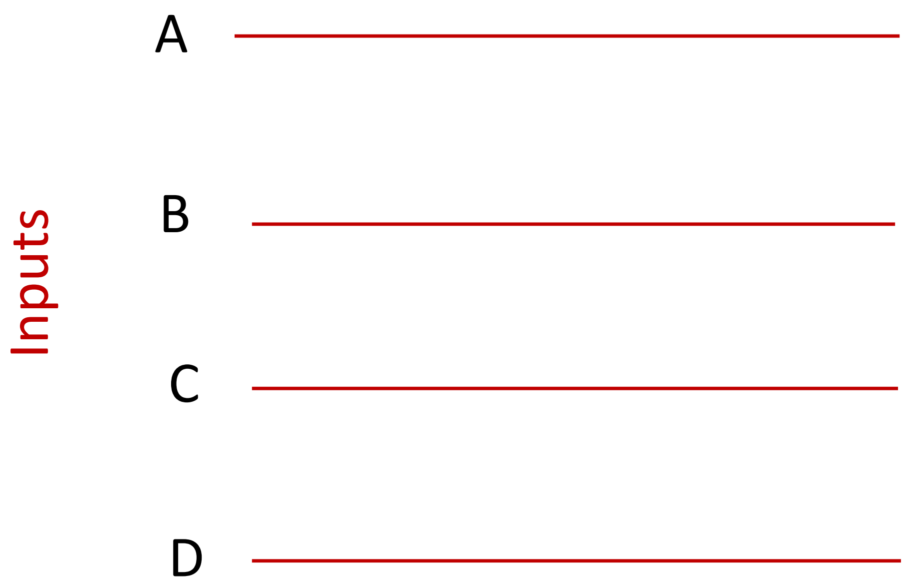


X-to-*Y* Multiplexer:

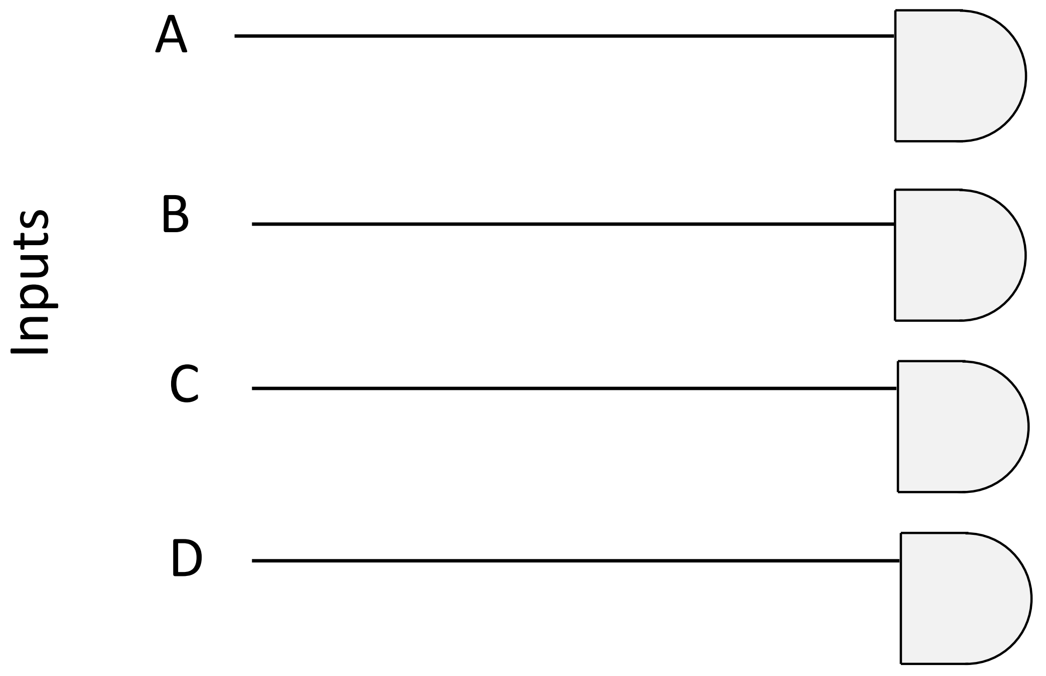
Chooses one of its *X* input pins, and outputs its value at one of its *Y* output pins, while all other output pins are reset to 0s (usually)



4-to-1 Multiplexer Implementation

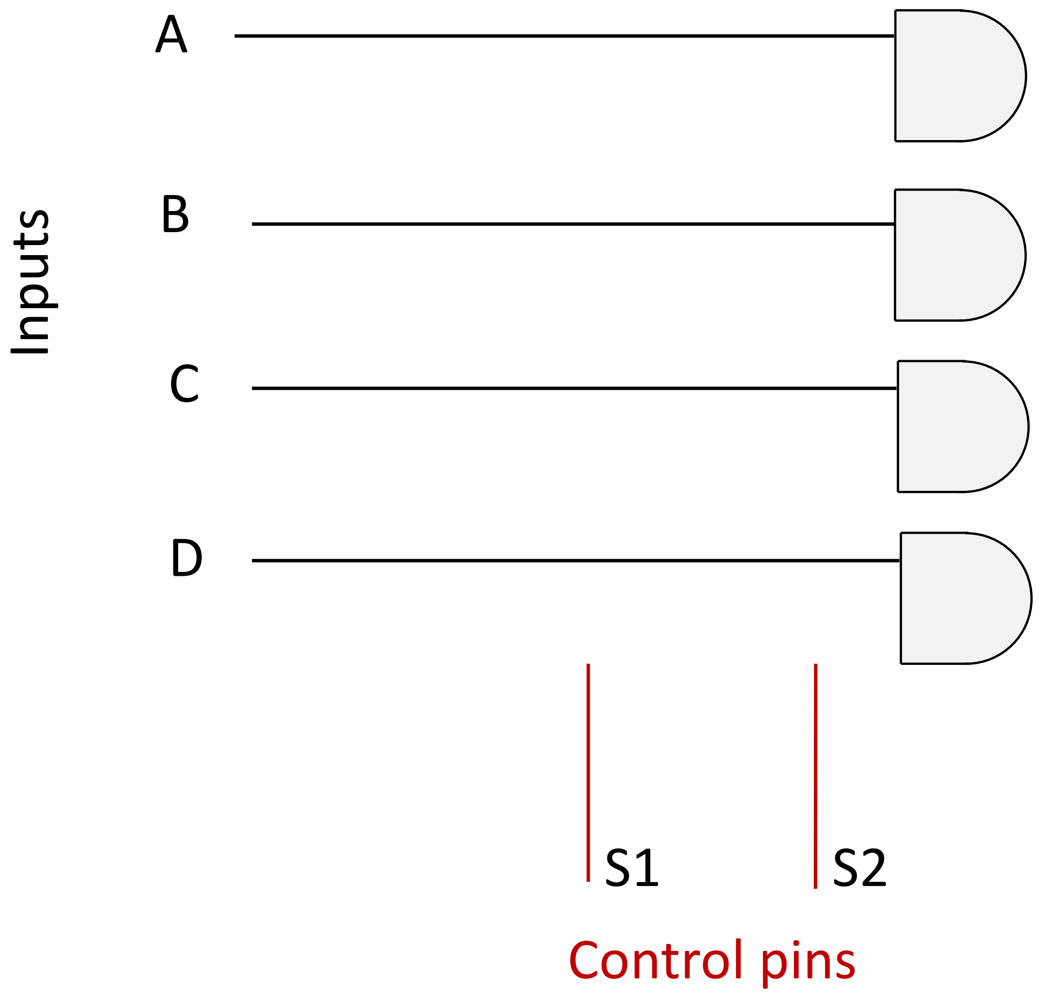


4-to-1 Multiplexer Implementation



AND logic gate
for each pin

4-to-1 Multiplexer Implementation



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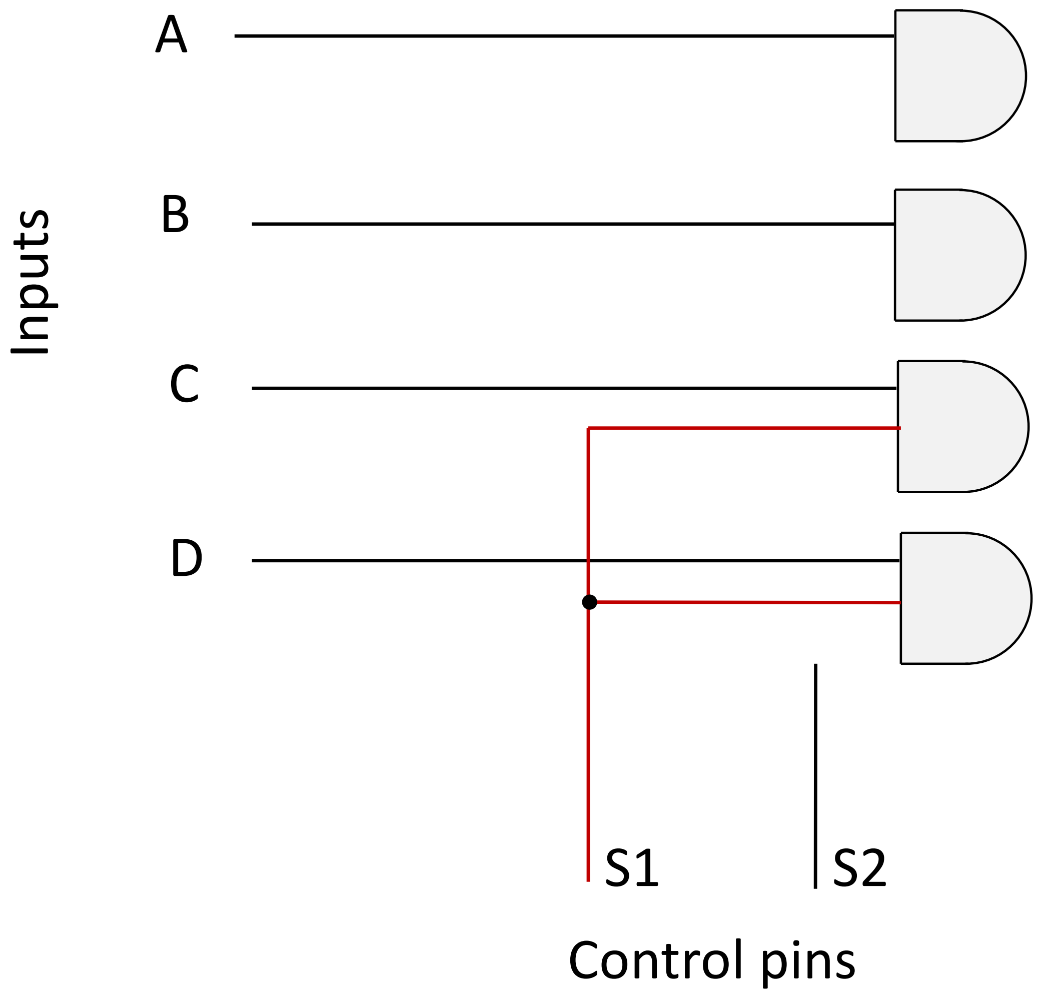

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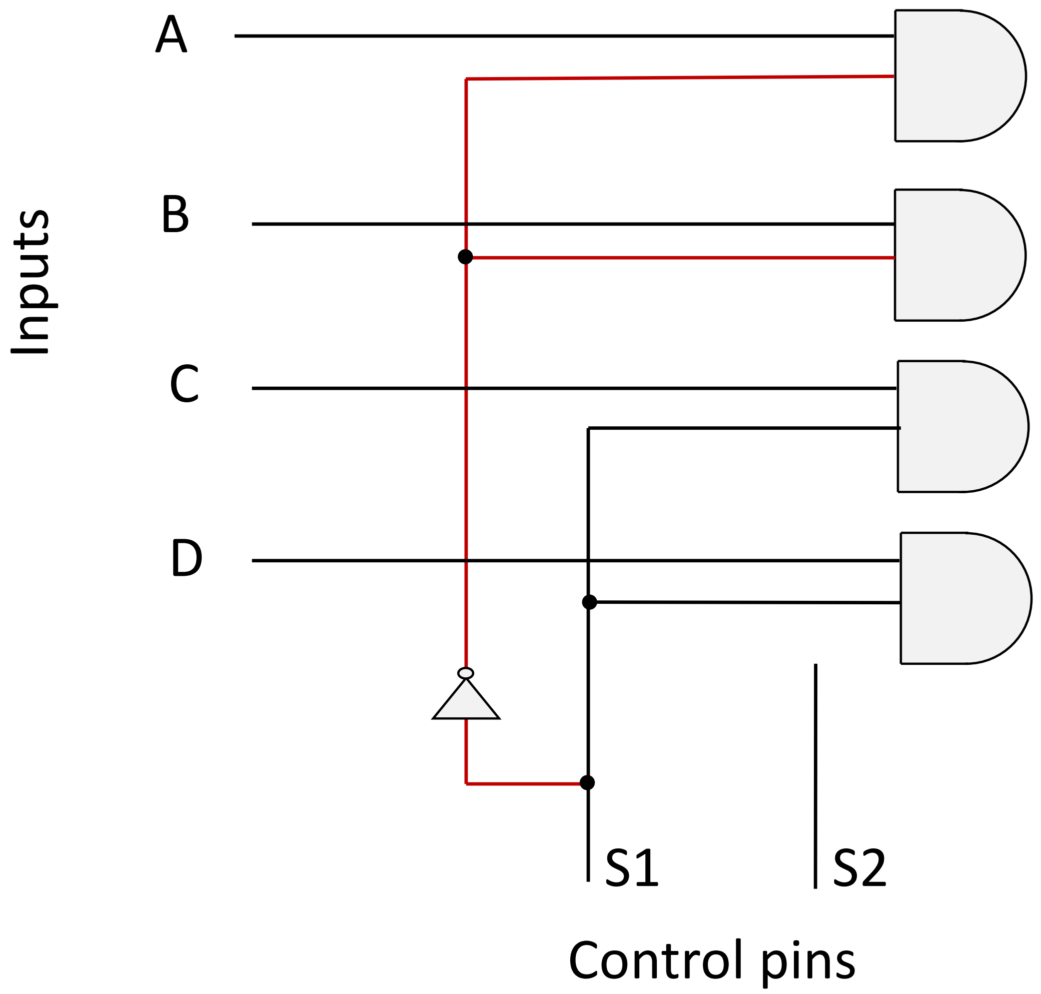

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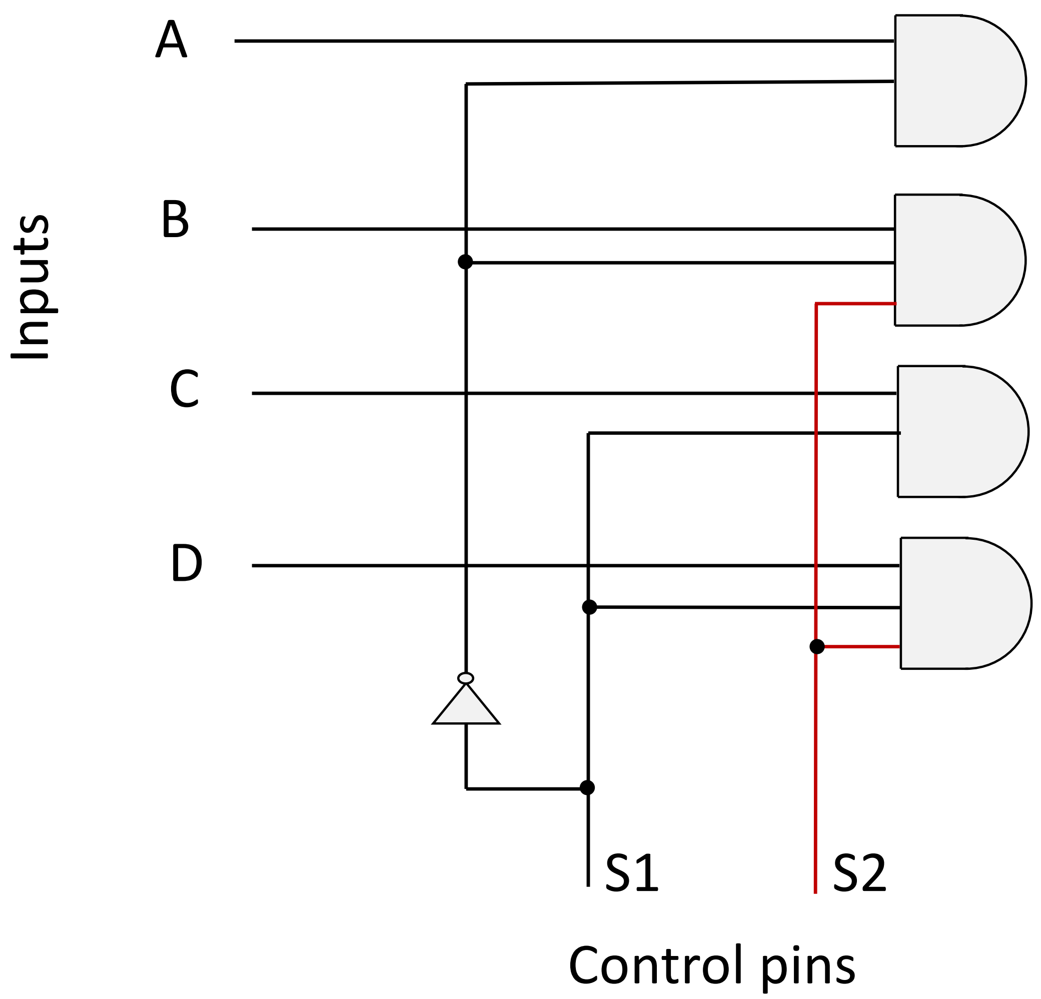

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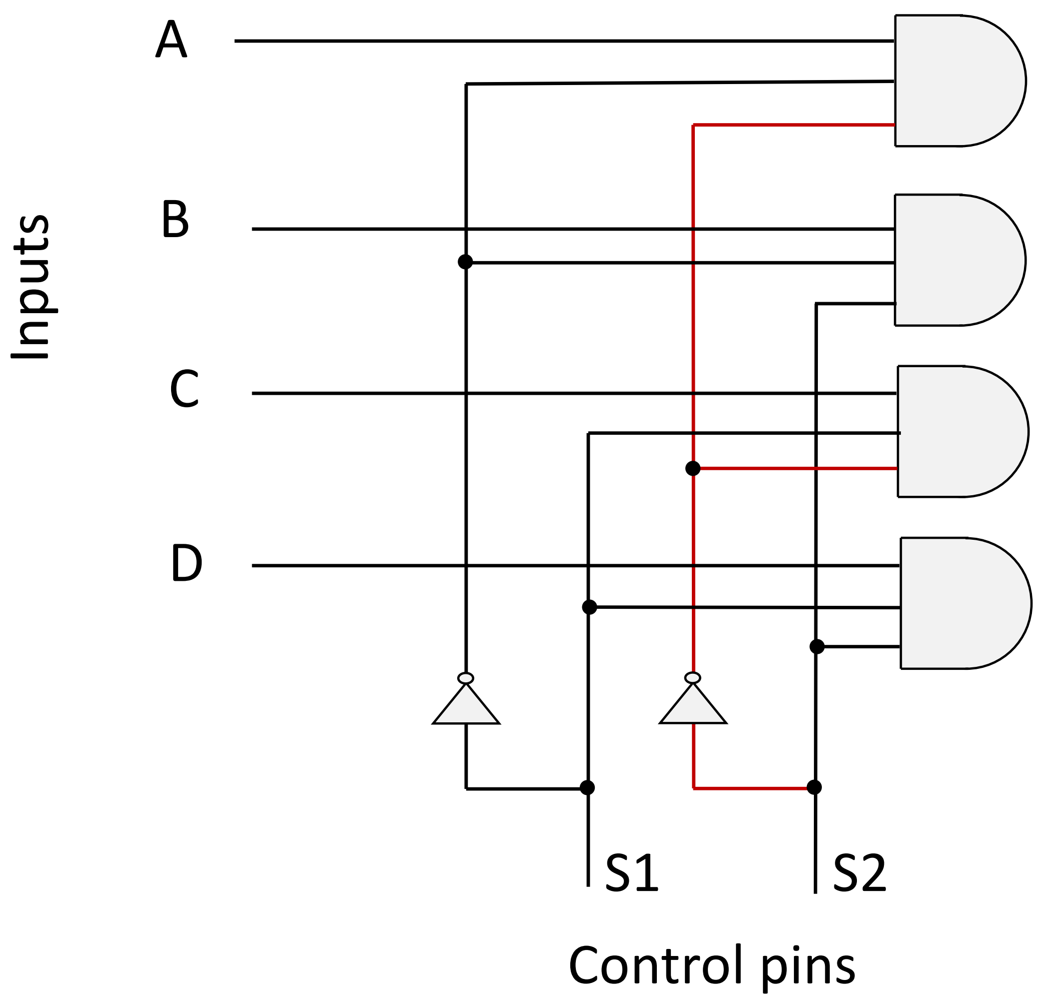

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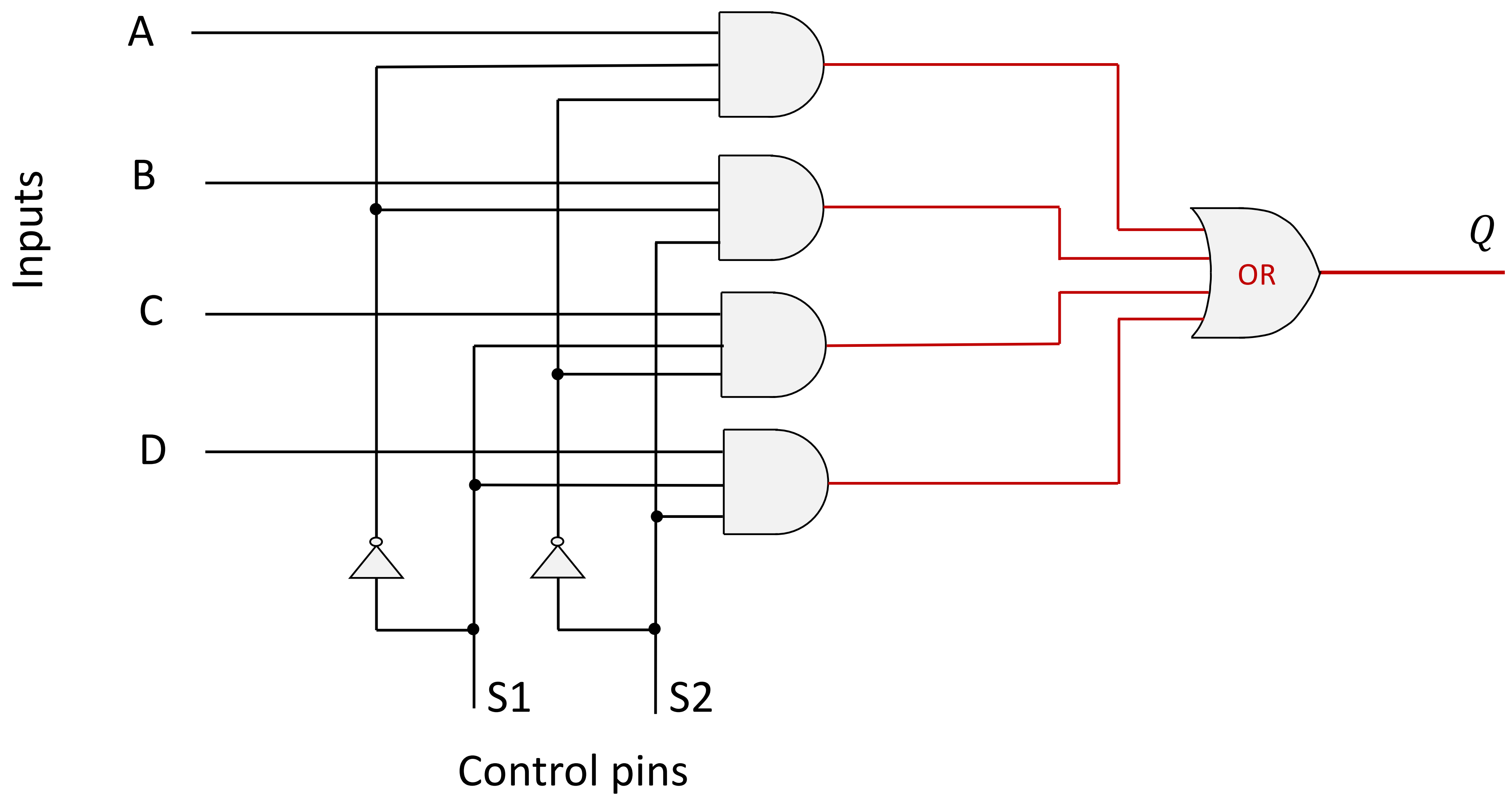

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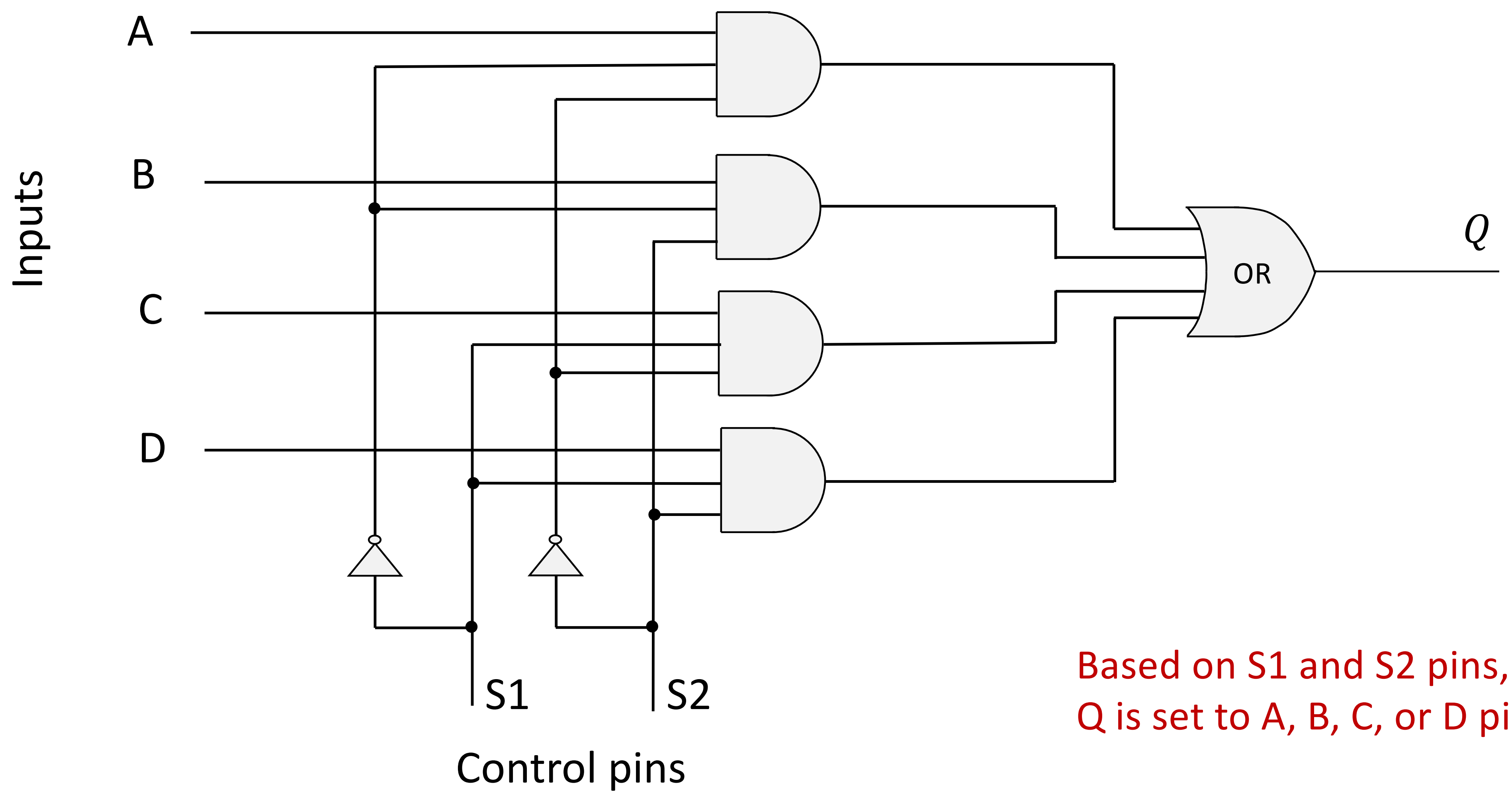
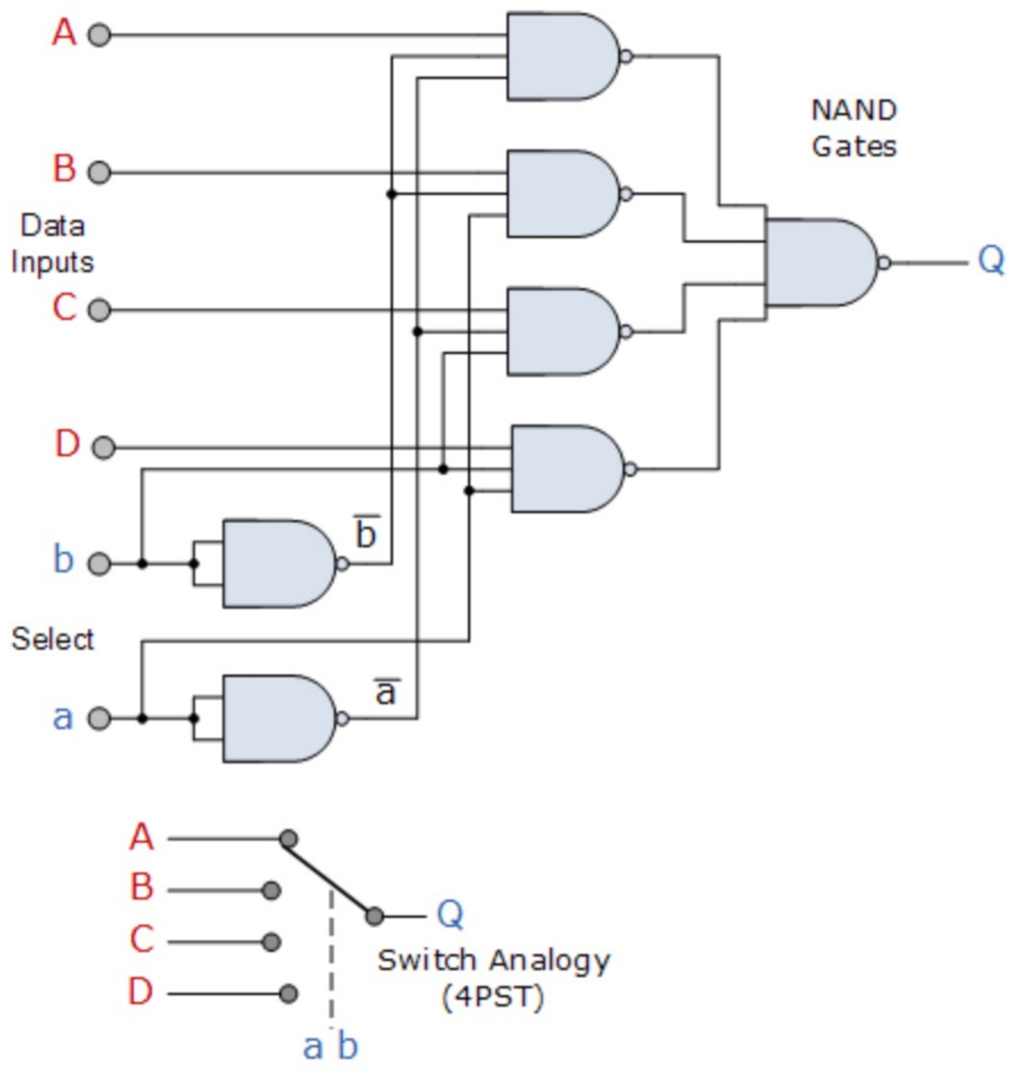


Based on S1 and S2 pins,
Q is set to A, B, C, or D pin

An Alternative Implementation: 4-to-1 Multiplexer by Using NAND Gates



A
B
Data Inputs
C
D
b
Select
a
$\overline{b}$
$\overline{a}$
NAND Gates
Q
A
B
C
D
Q
Switch Analogy (4PST)
a b