ANALOG CIRCUITS

EE301

Name: Vilasagaram Keerthan

Roll Number: 2022EEB1226

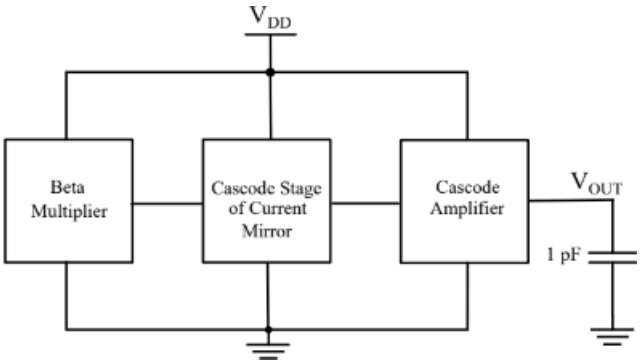
Course Instructor: Dr. Mahendra Sakare

Aim:

To design Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (in 180nm and 22nm technologies) in LTSpice and Magic.

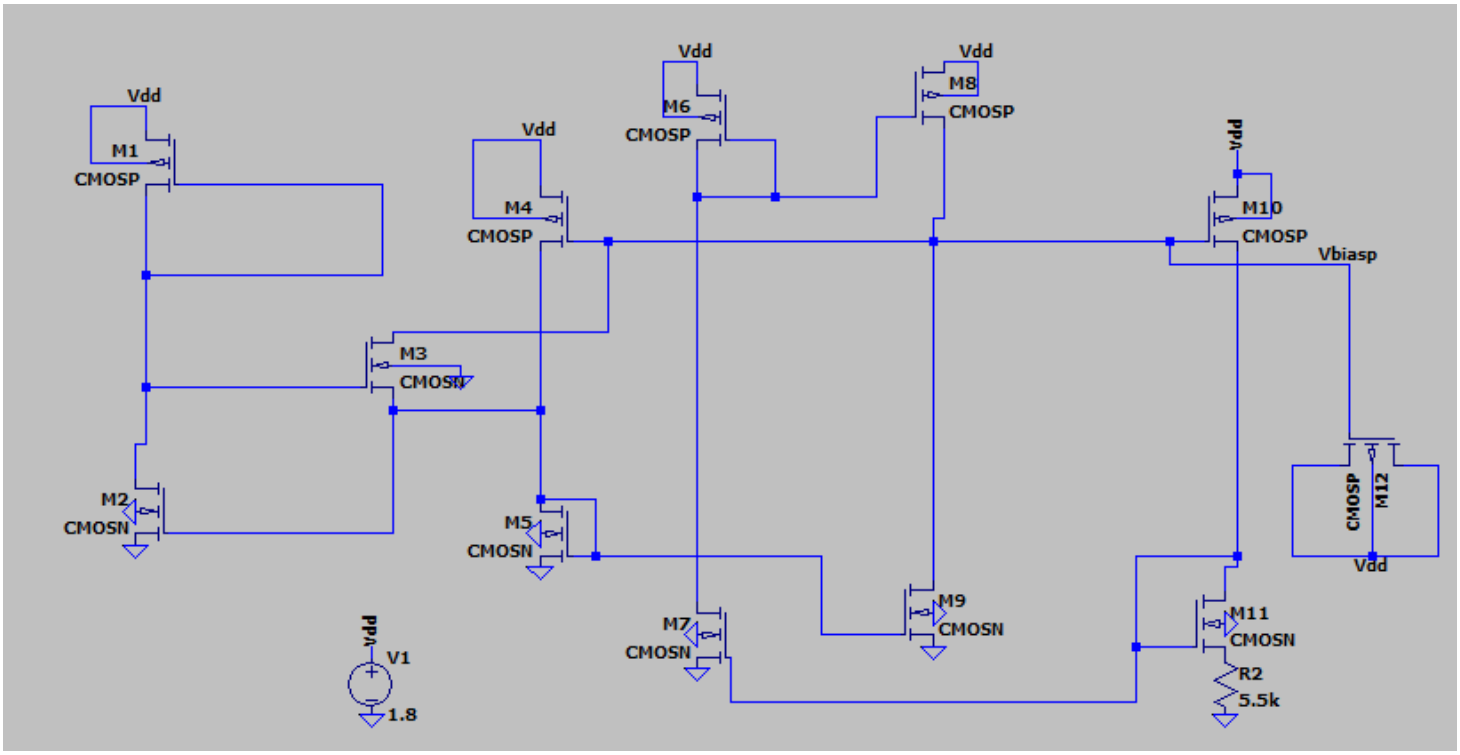
LTSpice Simulation:

The overall block diagram of cascode amplifier with other blocks:

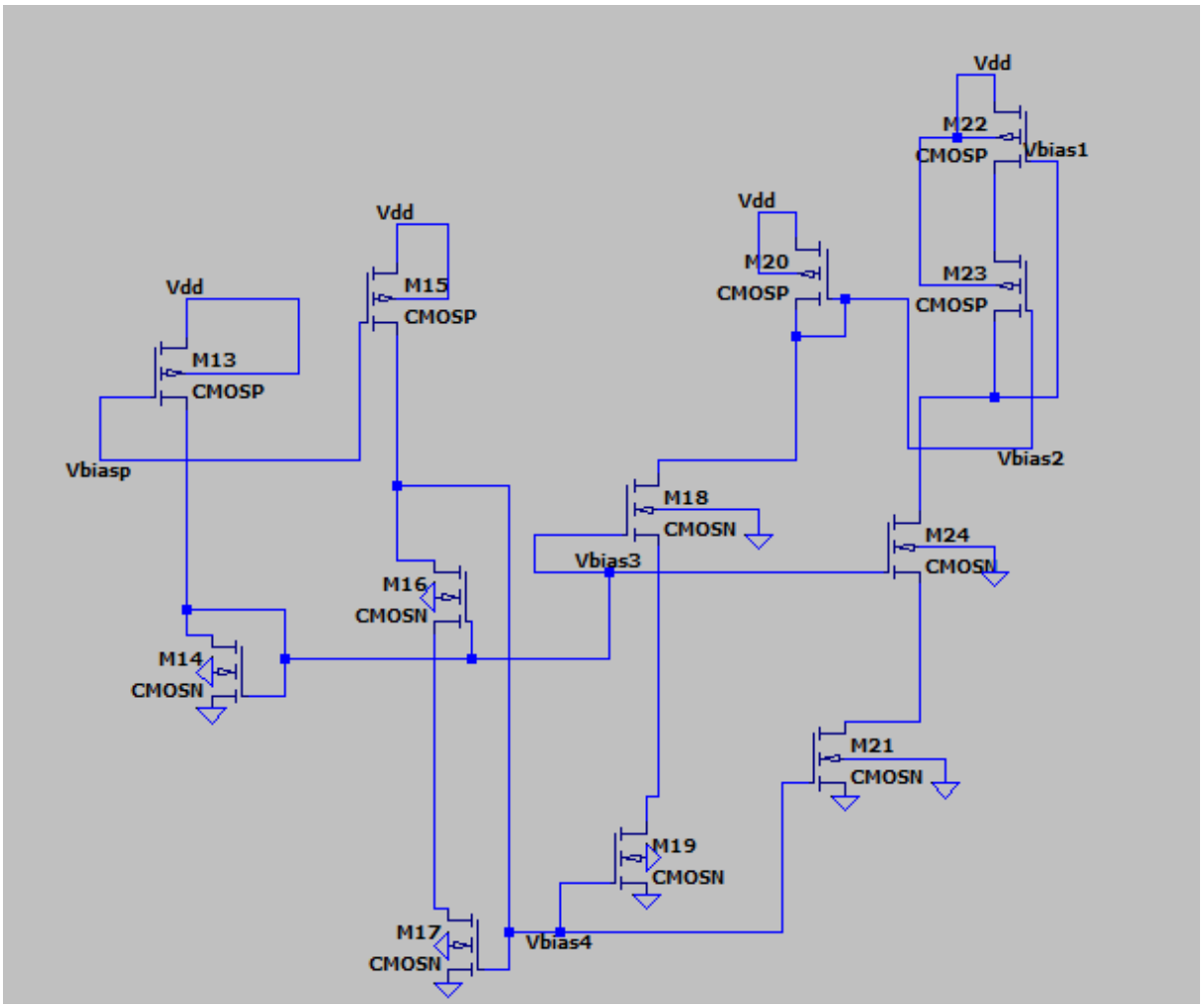


a. 180nm Technology:

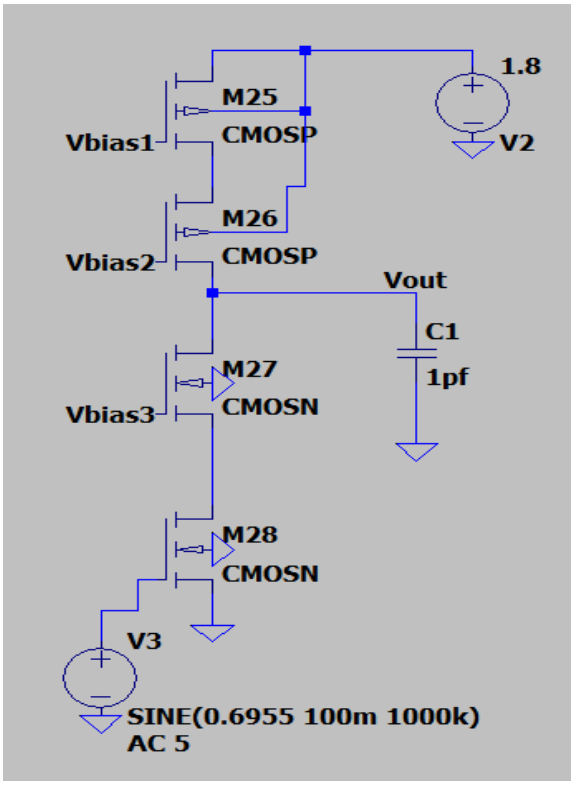
LTspice Simulation photos for beta Multiplier, Cascode Mirror and Cascode Amplifier(180nm). w/L are set in the Beta Multiplier and Cascode Current Mirror circuits.



Beta Multiplier



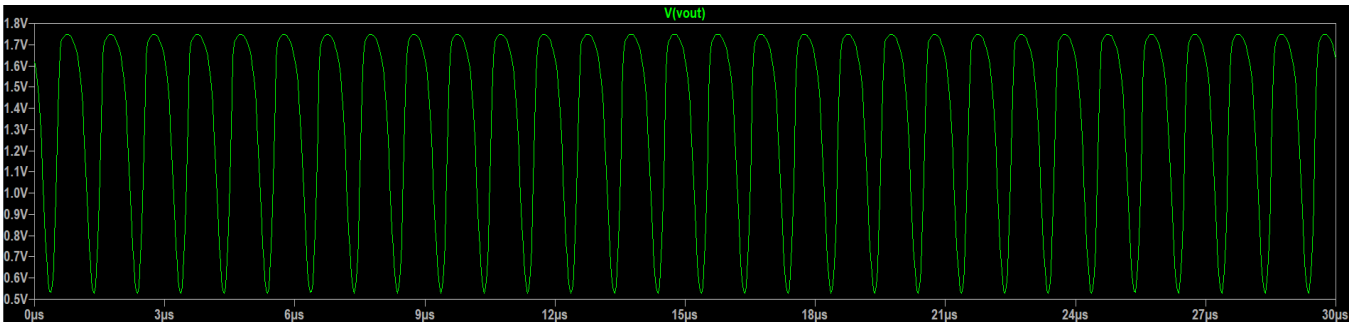
Cascode Current Mirror



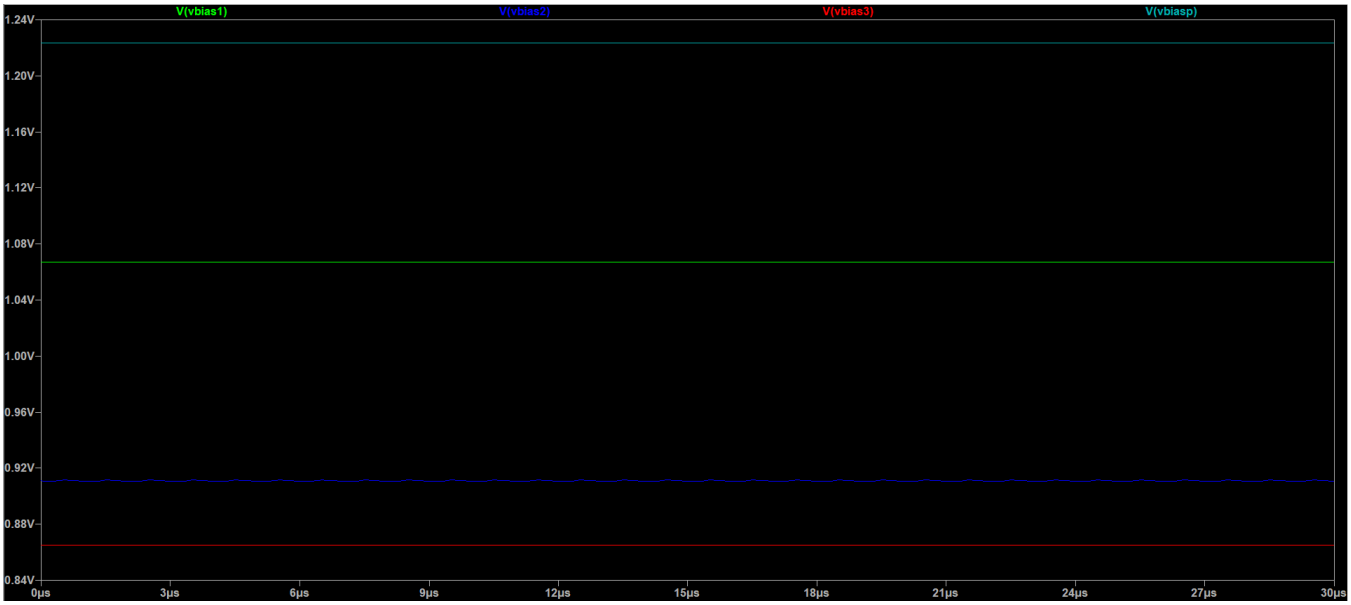
Cascode Amplifier

Output:

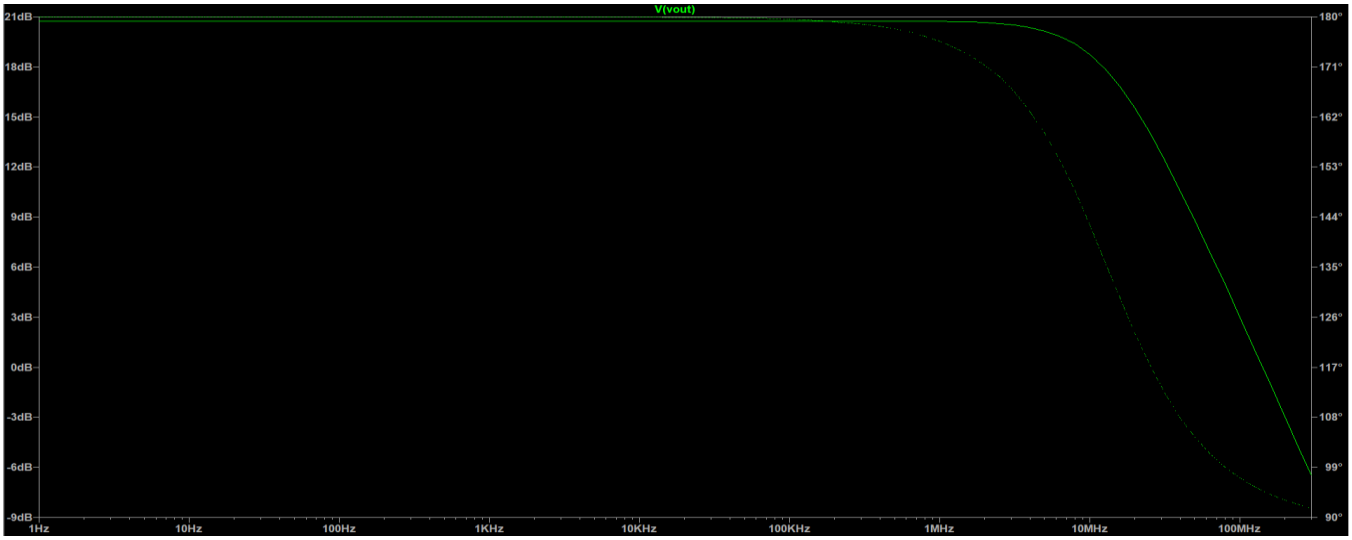
The simulation output values are attached here:



Output Waveform



Vbiasp, Vbias1, Vbias2, Vbias2, Vbias3 values



Frequency Response Graph(AC Analysis)

Calculations:- For Calculating the specifications $\left(\frac{W}{L}\right)$ of Cascode Amplifier.

Given, $V_{DD} = 1.8V$, $A_v = 20V/V$ $C_L = 1pF$

Power Dissipation (P_D) < 5mW, Unity Gain B.W (UGB) > 500KHz

$\mu_n C_{ox} = 350.8\mu A/V^2$; $\mu_p C_{ox} = 71.2\mu A/V^2$ $\lambda = 0.09$ (channel modulation)

for 180nm technology:-

Assumption:- let Pole frequency $f_p = 2.2MHz$

$$\because f_p = \frac{1}{2\pi R_{out} C} \Rightarrow R_{out} = \frac{1}{2\pi f_p C} = 72343.156\ \Omega$$

$$\because g_m = \frac{A_v}{R_{out}} \Rightarrow g_m = \frac{20}{72343.156} = 0.000276\ S$$

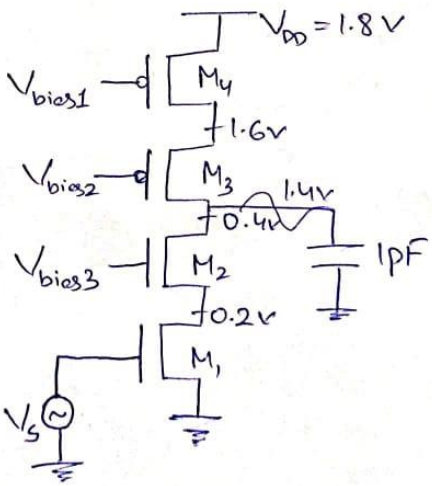
$$\because g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_{NMOS} V_{ov}$$

for finding V_{ov} lets consider the ckt diagram.

Considering all the MOSFETs to be in saturation

$V_{ov} = V_{DS}$

Considering the Industrial standards, drop across each MOSFET be $\boxed{V_{ov} = 0.2V}$



$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_{NMOS} V_{ov}$$

$$0.000276 = 350.8 \times 10^{-6} \left(\frac{W}{L}\right)_{NMOS} \times 0.2 \Rightarrow \left(\frac{W}{L}\right)_{NMOS} = 3.94$$

Since, the same current is flown through all the MOSFETs

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{NMOS} V_{ov}^2 (1+\lambda V_{DS}) \quad \text{(for NMOS)}$$

$$I_D = \frac{1}{2}\mu_p C_{ox_p}\left(\frac{W}{L}\right)_{PMOS} V_{ov}^2 (1+\lambda V_{DS}) \quad \text{(for PMOS)}$$

Equating Both

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_{NMOS} = \mu_p C_{ox}\left(\frac{W}{L}\right)_{PMOS}$$

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{350.8 \times 3.94}{71.2} = 19.41$$

Power Dissipation (P.D) $= V_{DD} \times I_D$

$= 1.8 \times I_D$

$= 49.34\,mW$ (<

$= 0.05\,mW$ (<5mW)

$I_D = \frac{1}{2} \times 350.8\mu \times 3.94 \times (0.2)^2 (1+0.09\times 0.2)$

$= 28.14\,\mu A$

For Range of V_{bias1} & V_{bias2} & V_{bias3}:

$V_{ov} = 0.2V$

for M_3, $V_D = 1.4V$, $V_S = 1.6V$

For Saturation, : $|V_{GS} - V_{TH}| \leq V_{DS}$

$$|V_{bias2} - V_S| - |-0.5| \leq |1.4 - 1.6|$$

$$V_{bias2} \geq 0.9V$$

for M_4, $V_D = 1.6V$, $V_S = 1.8V$

$V_{bias1} \geq 1.1V$

for M_1 $V_D = 0.2V$, $V_S = 0$

$V_{ov} = 0.2V$

$V_S = 0.2 + V_{TH} = 0.7V$

$\left(\frac{W}{L}\right)_{NMOS} = 3.94$ $\quad L = 180nm$

$(W)_{NMOS} = 709.27nm$

for M_2

$V_D = 0.4V, V_S = 0.2V,$

$V_{ov} = 0.2V$

$V_{ov} = V_{bias3} - V_S - V_{Th} \Rightarrow$

$V_{bias3} \geq 0.9V$

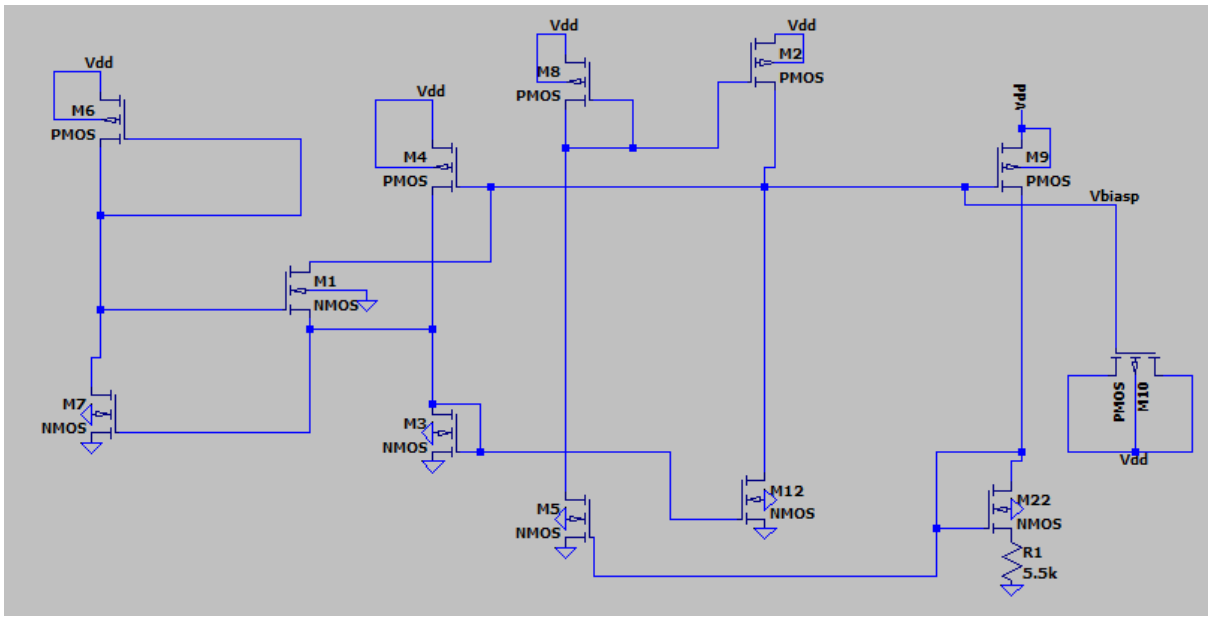
$\left(\frac{W}{L}\right)_{PMOS} = 19.41 \Rightarrow (W)_{PMOS} = 3494.55nm$

Comparing Simulation Results with Theoritical values:-

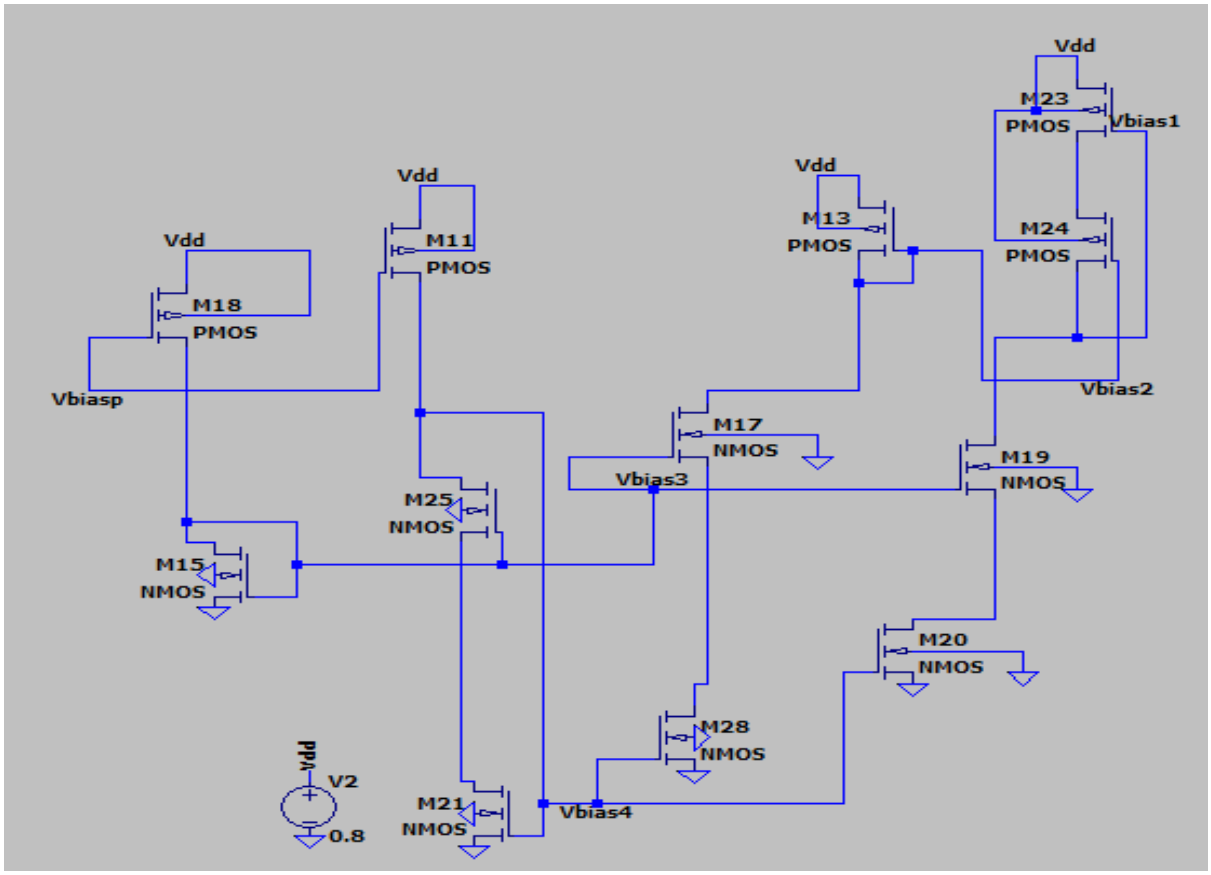
	Theoritical Values	Simulation values. for 180nm technology
V_{biasp}		1.223V
V_{bias1}	$\geq 1.1V$	1.11V
V_{bias2}	$\geq 0.9V$	~~0.865V~~ 0.911V
V_{bias3}	$\geq \leq 0.9V$	0.865V
UGB	>500kHz	150MHz
I_D	~~32.146μA~~ 28.14μA	~~28.14μA~~ 28.45μA
A_v	2602dB	21dB
P.D	< 5mW, 0.05mW	~~0.05mW~~ 28.45μ × 1.8 = 0.05121mW
V_S	0.7V	0.6955V

b. **22nm Technology:**

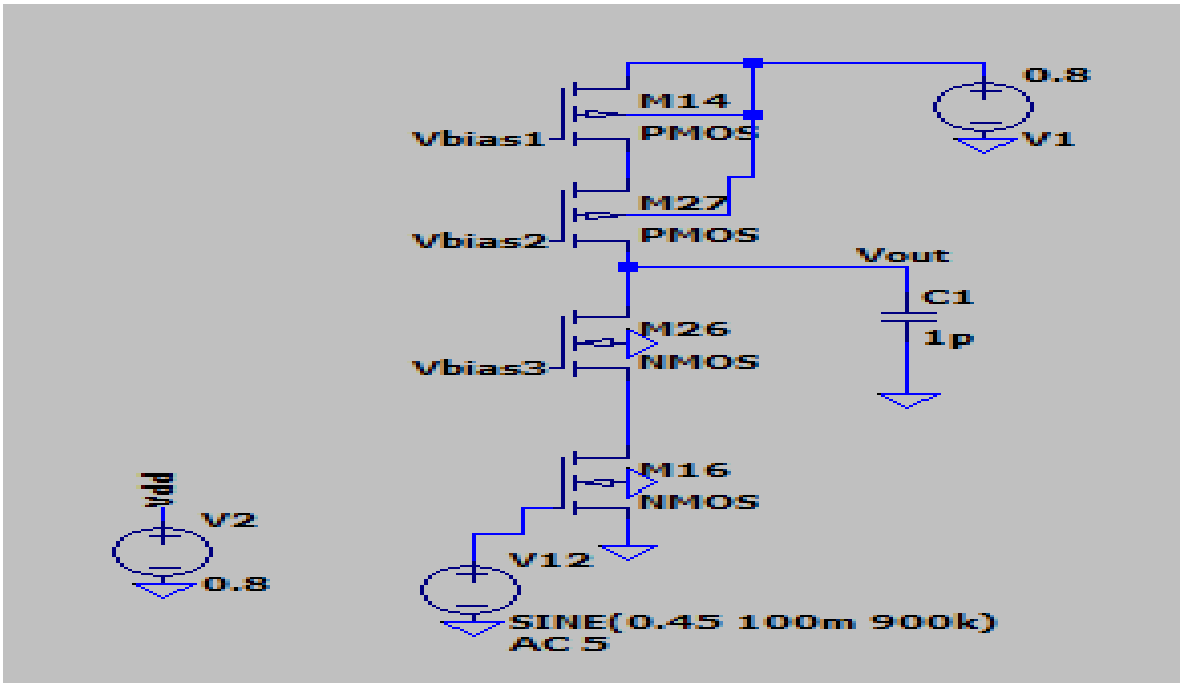
LTspice Simulation photos for beta Multiplier, Cascode Mirror and Cascode Amplifier(180nm). w/L are set in the Beta Multiplier and Cascode Current Mirror circuits.



Beta Multiplier



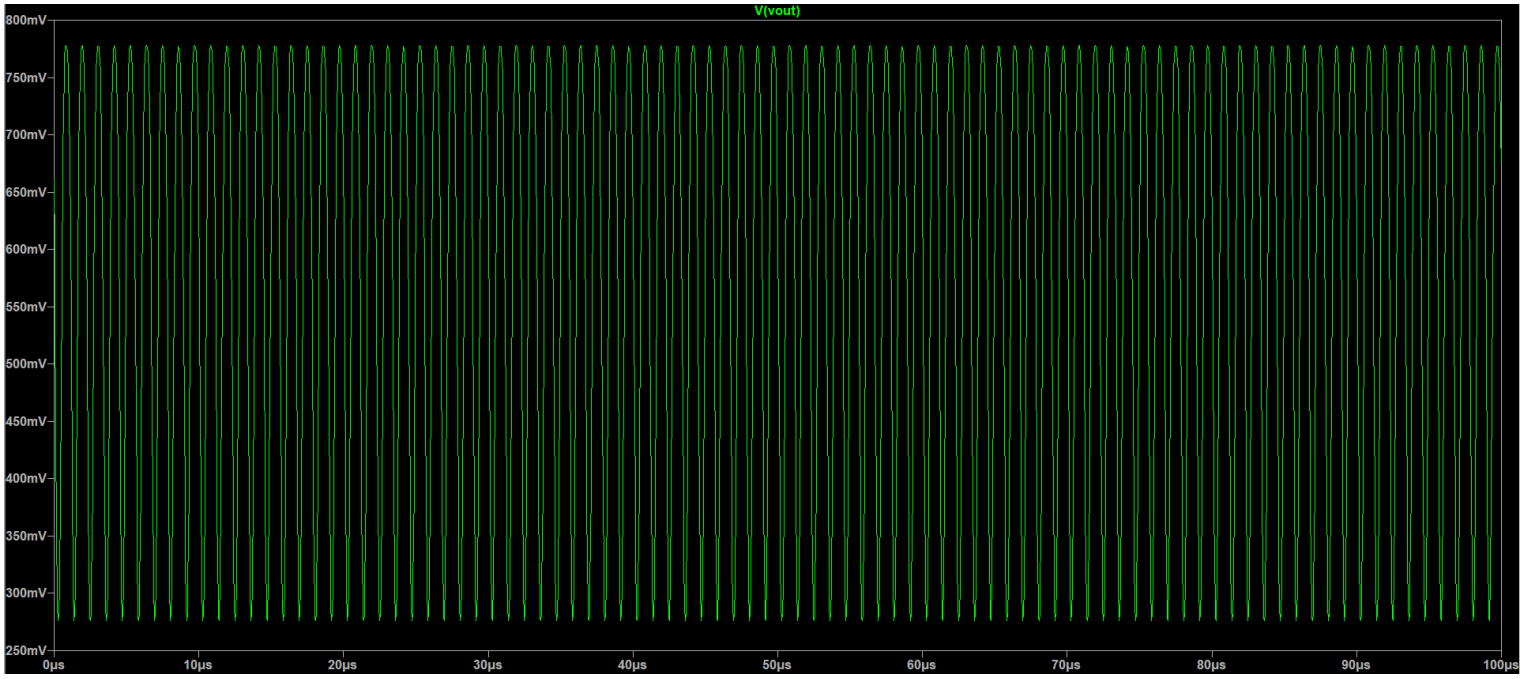
Cascode Current Mirror



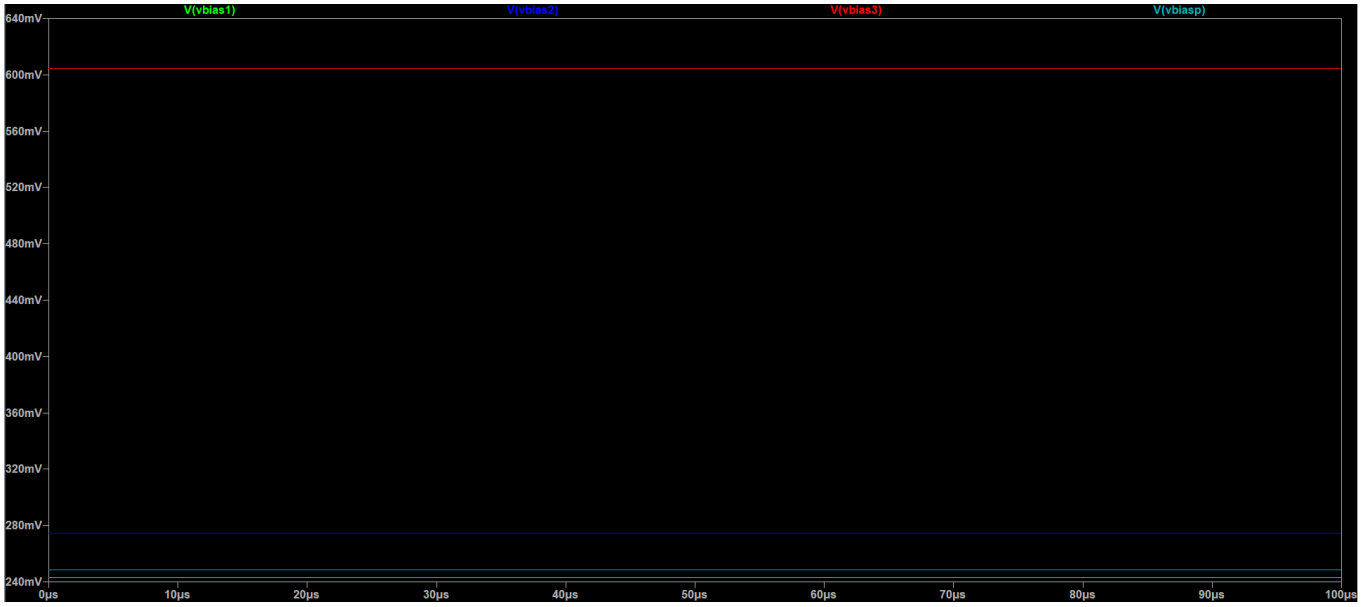
Cascode Amplifier

Output:

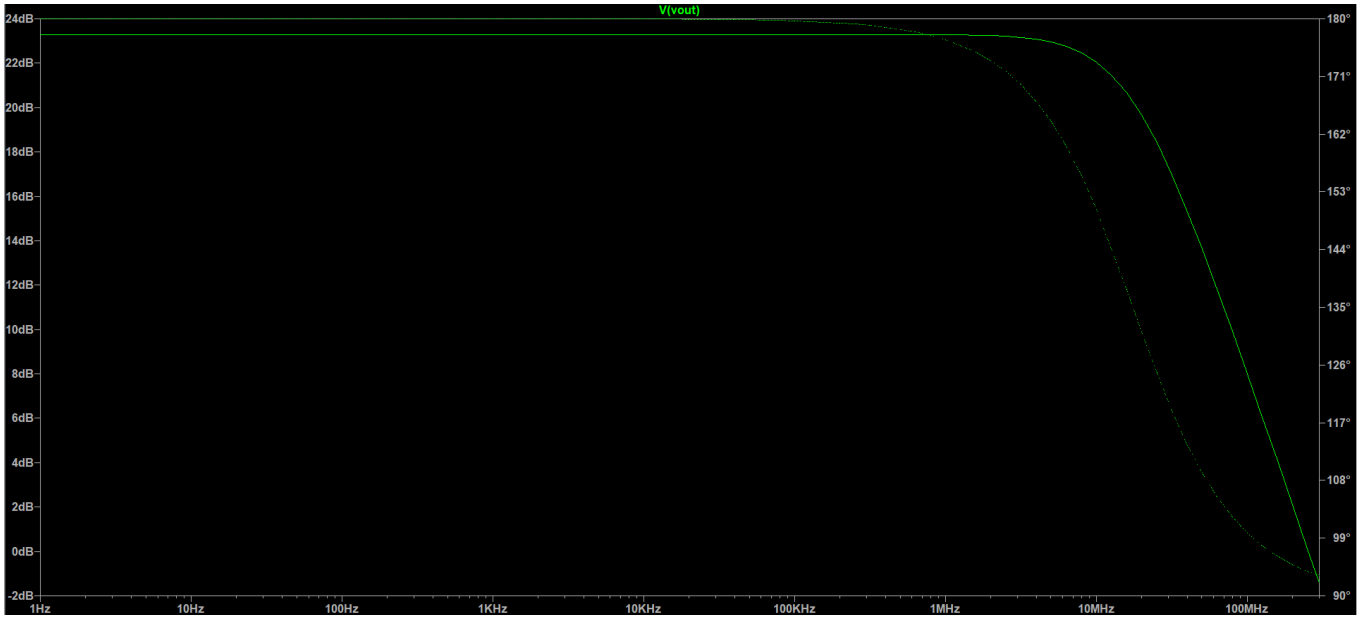
The Simulation outputs are Attached here:



Output Waveform



Vbiasp, Vbias1, Vbias2, Vbias3 values



Frequency response Graph(AC Analysis)

Calculations: For 22nm Technology

Calculations :- Considering the given values of some as 180nm technology.

for 22nm technology :- $\mu_n C_{ox} = 100\mu A/V^2$, $\mu_p C_{ox} = 50\mu A/V^2$

Assumptions :- let pole frequency $f_p = 2.6MHz$

$$f_p = \frac{1}{2\pi R_{out} C} \Rightarrow R_{out} = \frac{1}{2\pi f_p C} = 61213.44\Omega$$

$$g_m = \frac{A_v}{R_{out}} = \frac{20}{61213.44} = 0.000326\ S$$

$$\because g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_{NMOS} V_{ov}^2$$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_{NMOS} V_{ov} \Rightarrow 0.000326 = 100\times10^{-6}\left(\frac{W}{L}\right) \times 0.2$$

$$\Rightarrow \left(\frac{W}{L}\right)_{NMOS} = 16.336$$

$$I_D = \frac{1}{2} \times 100 \times 10^{-6} \times 16.336 \times (0.2)^2$$

$$\boxed{I_D = 32.672\mu A}$$

Since same current posses through the P-MOS also.

$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_{PMOS} V_{ov}^2$$

$$32.672^{\mu A} = \frac{1}{2} \times 50\times10^{-6} \times \left(\frac{W}{L}\right)_{PMOS} (0.2)^2$$

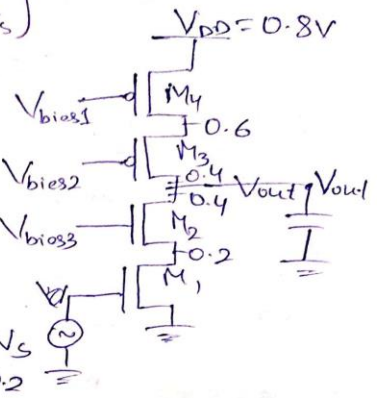
$$\left(\frac{W}{L}\right)_{PMOS} = 32.672$$

Power Dissipation (P.D) $= V_{DD} \times I_D = 0.8 \times 32.672$

$= 26.137\mu W = 0.0261mW\ (<5mW)$

For finding range of V_{bias1}, V_{bias2}, V_{bias3} & V_S voltages

Consider the circuit (Saturation region for all MOSFETs)



for M_1: $V_D = 0.2V$, $V_{Source} = 0V$, $V_{Th} = 0.3V$

$V_S = 0.2 + 0.3 = 0.5V$

$V_{DS} \geq V_{GS} - V_{Th} \Rightarrow$

for M_2: $V_D = 0.4V$, $V_S = 0.2V$

$V_{bias3} = 0.2 + 0.3 + 0.2$

$\leq 0.7V$

for M_3: $V_{GS} - V_{Th} \geq -0.2V \Rightarrow V_{bias2} + 0.3 - 0.6 \geq -0.2$

$V_{bias2} \geq 0.1V$

for M_4: $V_{GS} - V_{Th} \geq -0.2$

$V_{bias1} - 0.8 + 0.3 \geq -0.2 \Rightarrow V_{bias1} \geq 0.3V$

$L = 22nm$

$\left(\frac{W}{L}\right)_{NMOS} = 16.336 \Rightarrow W_{NMOS} = 359.39nm$

$\left(\frac{W}{L}\right)_{PMOS} = 32.67 \Rightarrow W_{PMOS} = 718.79nm$

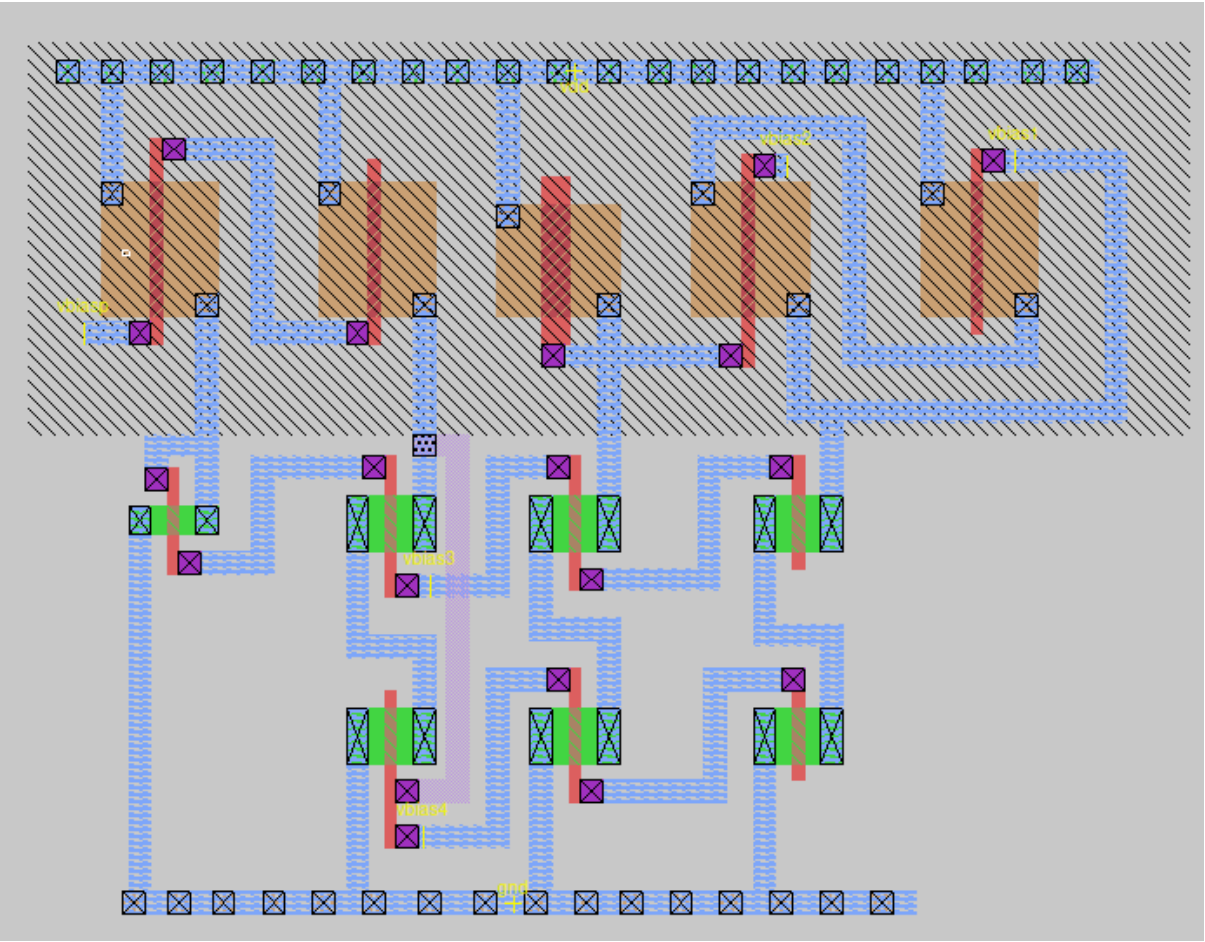
$A_V = 20 \log G_{bm}$

$= 20 \log 20$

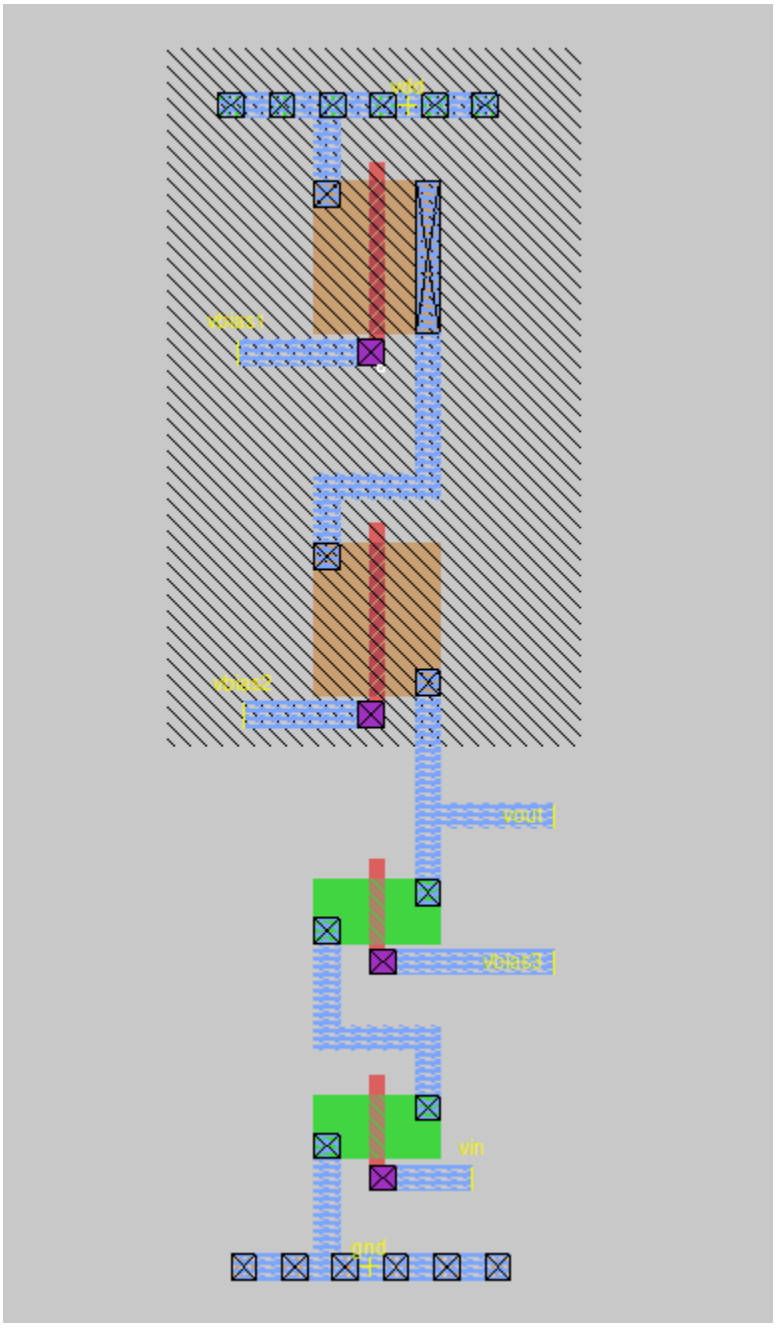
$= 26.02dB$

Comparing Both Simulation & Theoritical values for 22nm technology

		Theoritical Values	Simulation values
1.	V_{biasp}	—	248.47mV
2.	V_{bias1}	$\geq 0.3V$	243mV
3.	V_{bias2}	$\geq 0.1V$	274.5mV
4.	V_{bias3}	$\leq 0.7V$	604.5mV
5.	V_S	0.5V	0.45V
6.	UGB	> 500KHz	220MHz
7.	I_D	32.672μA	~~39.672μA~~ 24.9μA 28.85μA
8.	A_V	26.02dB	23.3dB
9.	P.D	<5mW 0.026mW	~~0.026~~ 28.85μ × 0.8 = 0.0231mW



Cascode Current Mirror



Cascode Amplifier

Specifications Summary:

- **Target Gain**: The required gain of 26.02 dB was achieved, with simulations showing gains of 21 dB for 180nm technology and 23.3 dB for 22nm technology.
- **Power Dissipation Requirement**: The power dissipation should be under 5mW, and simulations indicated values of 0.05121mW for 180nm and 0.0231mW for 22nm.

- **Unity Gain Bandwidth (UGB)**: A UGB of over 500kHz was required, with simulation results showing a UGB of 150 MHz for 180nm and 220 MHz for 22nm.
- **Frequency Response**: Both technologies demonstrated a low-pass filter frequency response, and all specifications were met.

Comparative Analysis: 180nm vs. 22nm Technology

- In 22nm technology, both Vbias values and current are lower, leading to significantly reduced power consumption compared to 180nm.
- The unity gain bandwidth and cutoff frequency are notably higher in 22nm technology.
- The smaller size of 22nm MOSFETs (approximately eight times smaller than 180nm MOSFETs) enables a denser layout, allowing for more transistors on a single chip, which enhances performance. However, the smaller scale also makes layout design more challenging, potentially increasing production costs.

Conclusion:

Simulations of the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier circuits were conducted for both 180nm and 22nm technologies in LTspice. Results aligned closely with theoretical expectations and met all performance specifications. Layouts for the Cascode Current Mirror and Cascode Amplifier were created using MAGIC for 180nm technology only. The comparison between 180nm and 22nm technologies was based on both LTspice simulation results and MAGIC layout designs.