
Evaluation Note

ADV7842 Evaluation

Board Rev. C

December 2010

Rev. 0

Contents

1.	Introduction.....	3
2.	Evaluation Kit.....	3
3.	DVP Evaluation Kit Overview	4
4.	DVP Video Evaluation System	5
5.	Initial Hardware Configuration.....	6
5.1	XRC Installation.....	6
5.2	Loading/Unloading Boards	7
5.2.1	Loading a Board.....	7
5.2.2	Unloading a Board.....	7
5.3	Running Scripts.....	7
5.4	Other XRC Features.....	9
5.4.1	Register Control.....	9
6.	The ADV7842 Evaluation Platform in Depth.....	10
6.1	Hardware Overview.....	10
6.1.1	Connectors	10
6.1.2	Jumpers	10
6.1.3	Miscellaneous	10
7.	Connecting an Input Video Source	11
8.	FPGA Configuration.....	12
	Appendix 1 – Schematics.....	13
	Appendix 2 – Downloading from FTP	19

Eval Note

1. Introduction

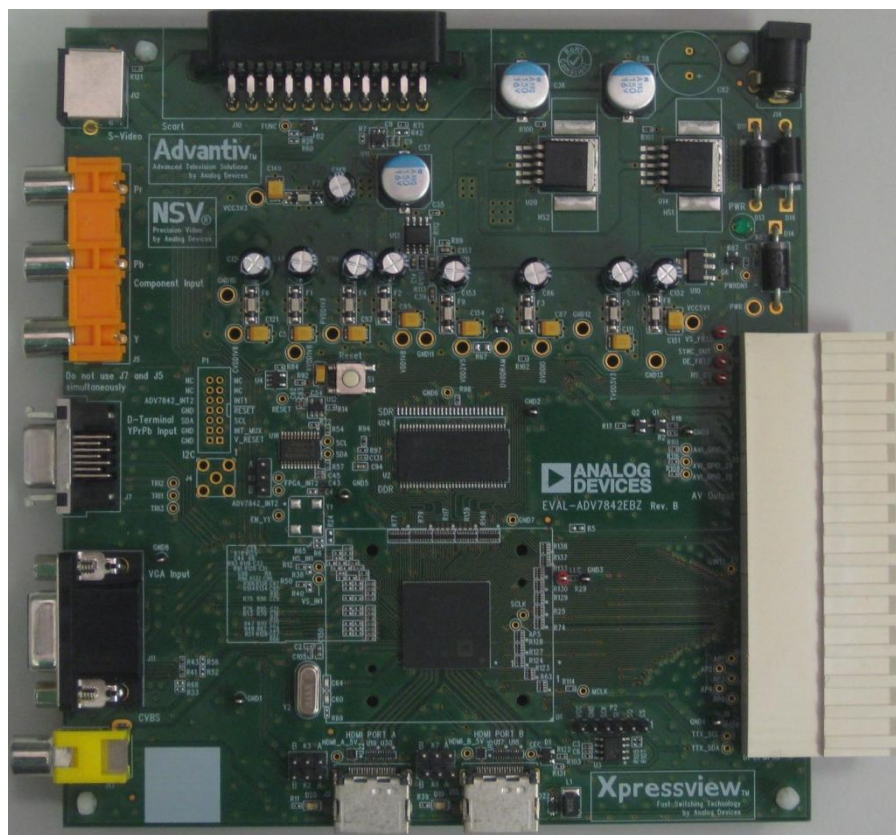
This evaluation note is intended to provide application support for the ADV7842 evaluation board. It also provides details on the set up and manual configuration of the evaluation board. Software drivers are available for this evaluation board - a separate user guide is available for these software drivers.

This note applies to board revision B & C.

2. Evaluation Kit

The ADV7842 evaluation board kit should consist of the following:

1. ADV7842 Evaluation Board
2. Directions to an FTP site for latest updates



ADV7842 Video Input Module

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The ADV7842 tools, evaluation software and documentation are kept on an FTP site. For access to the latest versions we recommend you to update with the latest files from the FTP site.

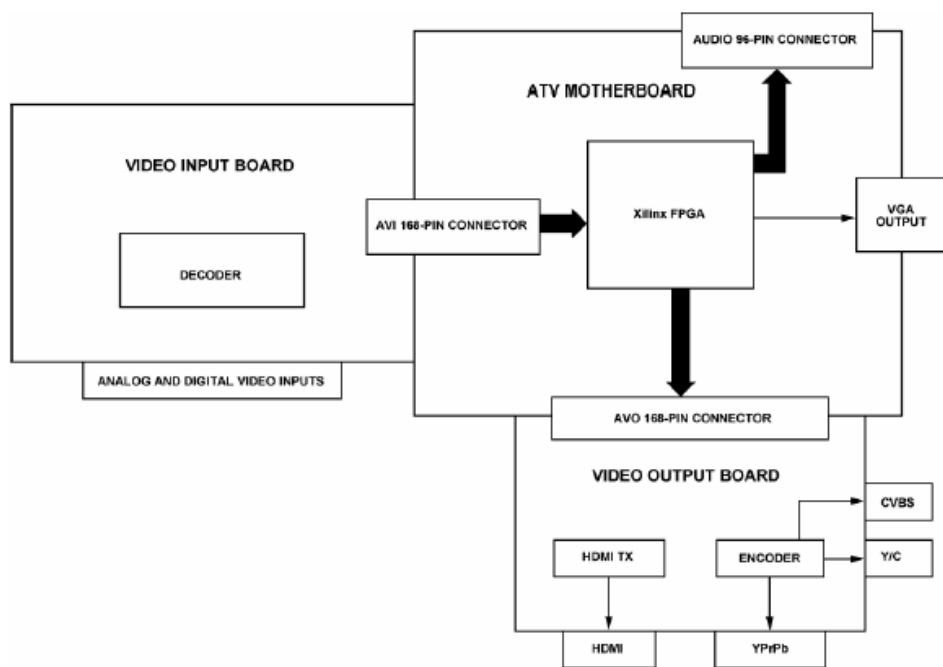
For details of how to log onto the FTP site, please see Appendix 2.

For the FTP password, please contact your local FAE.

3. DVP Evaluation Kit Overview

The complete evaluation platform consists of a Motherboard and two daughter boards. The Motherboard's core is a Xilinx FPGA, used for data routing functions. The Motherboard also features three AD9742s (12-bit DACs) from Analog Devices. This allows the user to drive a VGA monitor with just the motherboard and front-end board. The backend of the platform can be connected to the video output board from Analog Devices. This modular board features an ADV7341 encoder and ADV7511 HDMI transmitter.

The front end of the platform feeds the digital outputs from the ADV7842 to the FPGA on the motherboard. The ATV Motherboard FPGA firmware includes both the evaluation board software driver and the hardware multiplexing function that routes the data to the backend devices and to the Video Output Module.



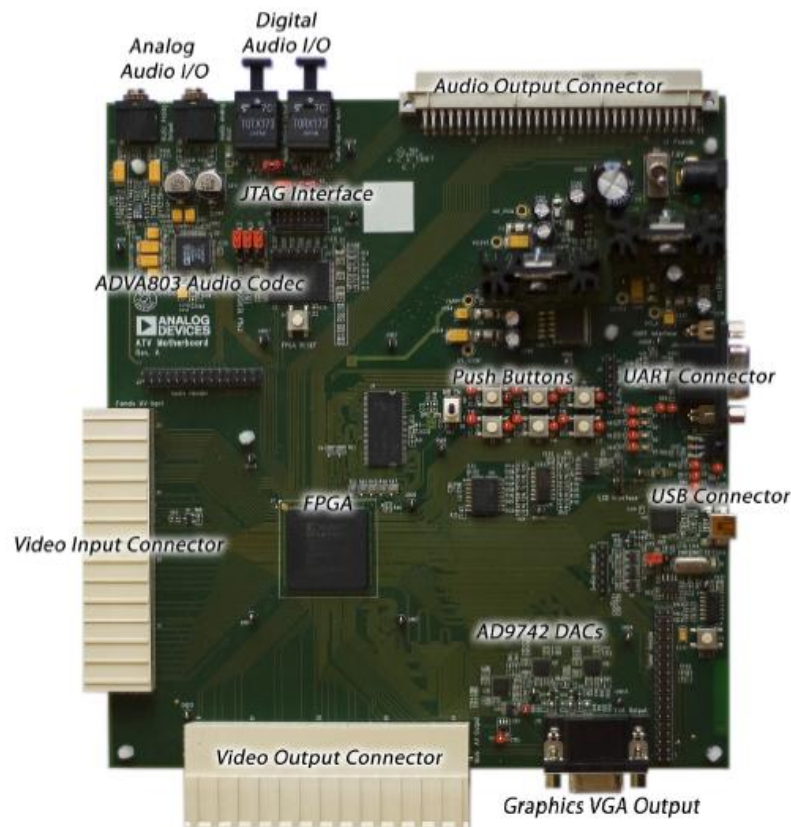
DVP Video Evaluation Platform

4. DVP Video Evaluation System

The ADV7842 evaluation board is a front end video input module of the DVP evaluation platform (see section 3) and is used to demonstrate all features of the ADV7842 HDMI receiver.

To assemble the platform, connect the male connector (J9) of the ADV7842 video input module to the female connector (J1) of the ATV motherboard. Connect the female connector (J1) of the video output module to the male connector (J2) of the ATV motherboard.

Connect the ATV motherboard power supply module supplied with the motherboard evaluation kit to the motherboard power connector, J18. To turn the evaluation platform on, flick the power switch (S10) to position "ON". The green power LED (D13) should light. Once the board is powered up, connect the USB cable supplied with the motherboard evaluation kit to USB connector, J12. The platform is now ready to use.

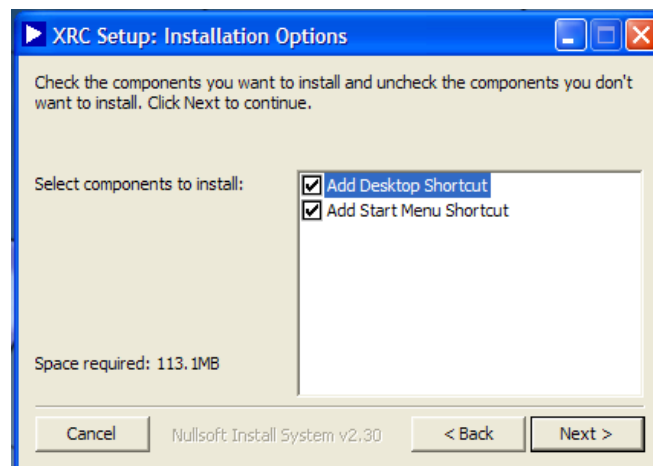


ATV Motherboard

5. Initial Hardware Configuration

5.1 XRC Installation

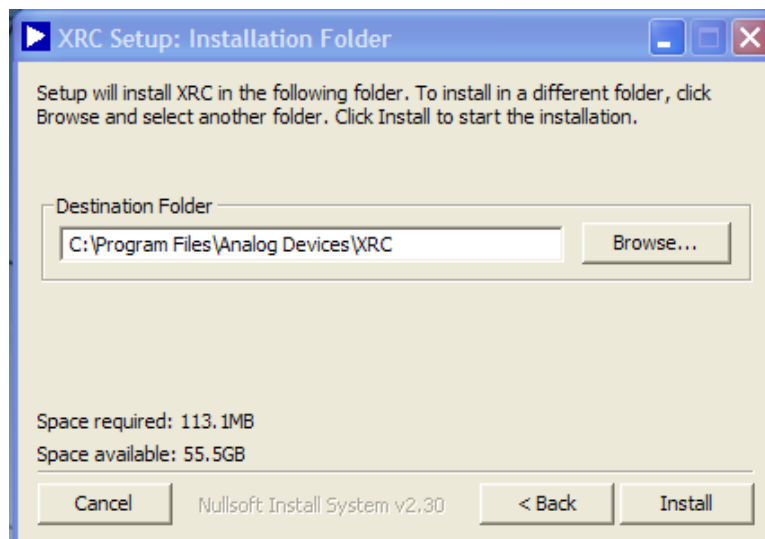
1. Run ADI_Install_XRC_x file (where x is the version number to be installed e.g. 1.4.8)
2. Review the license agreement and click “I Agree” if the terms of the agreement are acceptable
3. Select the desired access links – desktop shortcut and/or start menu shortcut



Installation Options

4. Press “Next>”

Select the desired installation folder **Error! Reference source not found.**



Installation Folder

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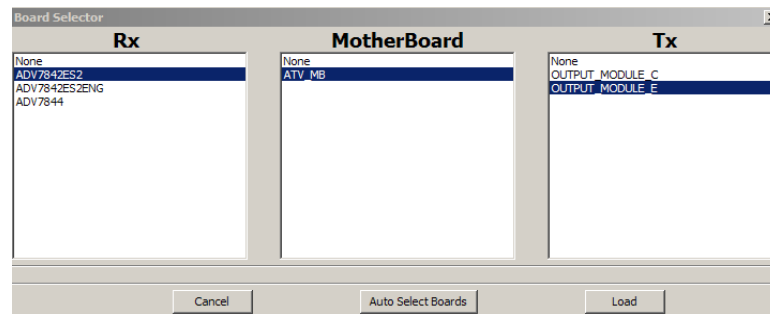
5. Press "Install"
6. When the install has completed, press "Close"

5.2 Loading/Unloading Boards

5.2.1 Loading a Board

The following steps must be performed to start a new XRC session by loading a new board.

1. Click "Choose Board..."
2. From the Board Selector window, select your attached system e.g. "ADV7842" as RX, "ATV_MB" from MotherBoard and "OUTPUT_MODULE_E" from TX.
3. Click "Load"



Board Selector

5.2.2 Unloading a Board

The following steps must be performed to end an XRC session by unloading the selected board.

1. Select Files -> Unload Boards

5.3 Running Scripts

Scripts can be run by either of the following options:

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1. Select Scripts -> ProjectName e.g. ADV7842
2. Follow the script tree as outlined in the expanding menus

1. Select Scripts -> Run Script
2. Open the script folder of the desired project
3. Select the desired script and click "Open"

Please be patient as the script may take several seconds to run. Successful download of the script is notified by the green light at the bottom of the screen flashing twice.

The screenshot displays the XRC Script Tree application. The 'Scripts' menu is open, showing a list of projects including ADV7604, ADV7842, and ADV7843. The 'ADV7842' project is selected, and its contents are displayed in the central pane. The 'HDMI' script is highlighted. The right pane shows the script content, which includes a list of video input and output configurations.

Script Content:

```
3_10_1440_x_480p60_RGB_444_in_RGB_444_out_Pixel_Repetition_2_VIC_14
3_10_1440_x_576p50_RGB_444_in_RGB_444_out_Pixel_Repetition_2_VIC_29
3_10_2880_x_480p60_RGB_444_in_RGB_444_out_Pixel_Repetition_4_VIC_35
3_10_2880_x_576p50_RGB_444_in_RGB_444_out_Pixel_Repetition_4_VIC_37
3_10_720_x_480p60_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_2
3_10_720_x_576p50_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_17
3_11_1280_x_720p50_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_19
3_11_1280_x_720p60_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_4
3_12_1280_x_720p50_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_19
3_12_1280_x_720p60_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_4
3_13_1280_x_720p50_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_19
3_13_1280_x_720p60_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_4
3_14_1280_x_720p50_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_19
3_14_1280_x_720p60_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_4
3_15_1280_x_720p50_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_19
3_15_1280_x_720p60_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_4
3_16_1920_x_1080i50_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_20
3_16_1920_x_1080i60_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_5
3_17_1920_x_1080i50_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_20
3_17_1920_x_1080i60_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_5
3_18_1920_x_1080i50_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_20
3_18_1920_x_1080i60_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_5
3_19_1920_x_1080i50_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_20
3_19_1920_x_1080i60_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_5
3_1_2880_x_480i60_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_4_VIC_10
3_1_2880_x_576i50_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_4_VIC_25
3_1_720_1440_x_480i60_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_2_VIC_6
3_1_720_1440_x_576i50_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_2_VIC_21
3_20_1920_x_1080i50_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_20
3_20_1920_x_1080i60_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_5
3_21_1920_x_1080p50_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_31
3_21_1920_x_1080p60_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_16
3_22_1920_x_1080p50_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_31
3_22_1920_x_1080p60_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_16
3_23_1920_x_1080p50_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_31
3_23_1920_x_1080p60_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_16
3_24_1920_x_1080p50_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_31
3_24_1920_x_1080p60_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_16
3_25_1920_x_1080p50_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_31
3_25_1920_x_1080p60_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_16
3_26_1920_x_1080p24_YPrPb_422_in_YPrPb_422_out_Pixel_Repetition_1_VIC_32
3_27_1920_x_1080p24_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_32
3_28_1920_x_1080p24_YPrPb_444_in_YPrPb_444_out_Pixel_Repetition_1_VIC_32
3_29_1920_x_1080p24_RGB_444_in_YPrPb_422_out_Pixel_Repetition_1_VIC_32
3_2_2880_x_480i60_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_4_VIC_10
3_2_2880_x_576i50_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_4_VIC_25
3_2_720_1440_x_480i60_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_2_VIC_6
3_2_720_1440_x_576i50_YPrPb_444_in_YPrPb_422_out_Pixel_Repetition_2_VIC_21
3_30_1920_x_1080p24_RGB_444_in_RGB_444_out_Pixel_Repetition_1_VIC_32
```

XRC Script Tree

Eval Note

5.4 Other XRC Features

5.4.1 Register Control

The following steps must be performed to use XRC Register Control:

1. Select Tools -> Register Control
2. Enter the Device Address in HEX
3. Ensure USB 1.4 from the drop down menu
4. Enter the desired register address in HEX
5. Press the "Write" button to write a value to the selected register
6. Press the "Read" button to read a value from the selected register

The screenshot shows a software window titled "Load / Read Register". It contains the following fields and controls:

- Device Address:** A text box containing "0x B2" and an "Add Register" button.
- Interface:** A dropdown menu currently set to "USB 1.4".
- Register Address:** A text box containing "0x 00".
- Write Data:** A row of eight input boxes containing the hexadecimal value "00110101" followed by a text box containing "53".
- Read Data:** A row of eight input boxes containing the hexadecimal value "00000000" followed by a text box containing "0".
- Buttons:** "Write" and "Read" buttons.
- Options:** Two checkboxes, "Load On Change" and "Constantly Read", both of which are unchecked.
- Address Size:** A text box containing the value "1".
- Register Size:** A text box containing the value "8".

Register Control Window

6. The ADV7842 Evaluation Platform in Depth

6.1 Hardware Overview

The following features of the ADV7842 evaluation board should be noted

6.1.1 Connectors

1. 2 x HDMI inputs (J2 & J15)
2. 1 x CVBS input (J13)
3. 1 x VGA input (J11)
4. 1 x D-Terminal input (J7)
5. 1 x Component input (J5)
6. 1 x S-video input (J12)
7. 1 x SCART input (J10)
8. 1 x 168 pin Male output (J9)

6.1.2 Jumpers

9. DDC Port A lines (K2, K3) – default position 'A'
10. DDC Port B lines (K7, K8) – default position 'A'

6.1.3 Miscellaneous

1. 2 x 512 Byte external EEPROM
2. 1 x SPI EEPROM
3. 256Mb DDR Memory Module

7. Connecting an Input Video Source

To connect an input video source to the ADV7842 evaluation board, select the required input cable (e.g. HDMI, VGA, Component, S-video, CVBS, SCART etc) and connect it to the corresponding input connector J2 or J15, J11, J5, J12, J13 or J10.

Do not use excessive force when connecting or disconnecting the cables as this may result in damage to the evaluation board.

8. FPGA Configuration

The ATV Mother Board FPGA firmware can be upgraded by programming the XCF16P Platform Flash via the JTAG interface. The firmware is available in the form of an *.mcs file. The ATV Mother Board FPGA firmware includes both the evaluation board software driver and the hardware multiplexing function that routes the data to the backend devices and to the Video Output Module.

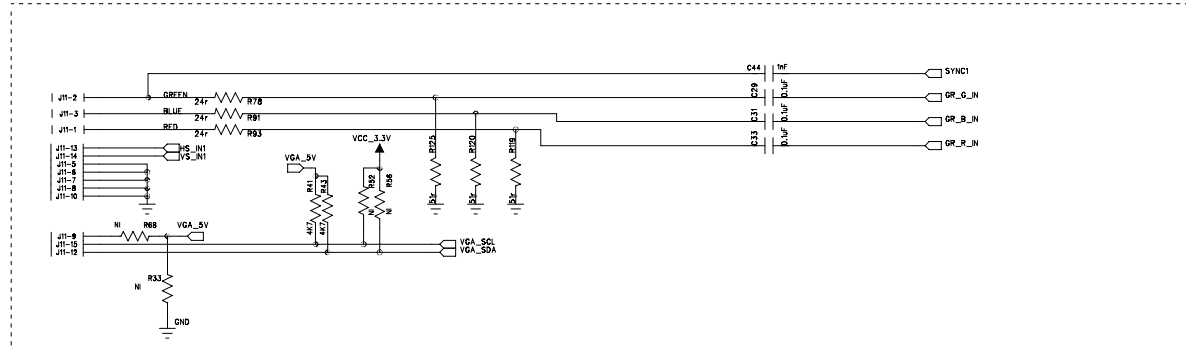
The following procedure must be followed:

- Ensure the Xilinx iMPACT software and the latest ISE service pack are installed on the PC (these are available from the Xilinx website, www.xilinx.com.)
- Connect the PC to the JTAG connector (J26) on the board via a Crossed Serial to JTAG cable.
- Ensure that the JTAG cable is connected in the correct orientation.
- Launch the iMPACT application and cancel the dialog box requesting to load a project.
- Power up the board and ensure that the JTAG cable is connected. Right click anywhere in the iMPACT window and select **Initialize Chain**. The XCF16P PROM and XC3S4000 FPGA will be detected in the JTAG chain. Bypass any request to configure the FPGA. This is automatically configured later by the PROM.
- When prompted to assign a configuration file to the PROM, select the new MCS file and click Open.
- Right click on the **PROM** icon and then click on **Program**. In the Program Options screen, check **Erase before programming** and **Verify**, and then click OK. After completion, the Programming Succeeded message appears in the iMPACT window.

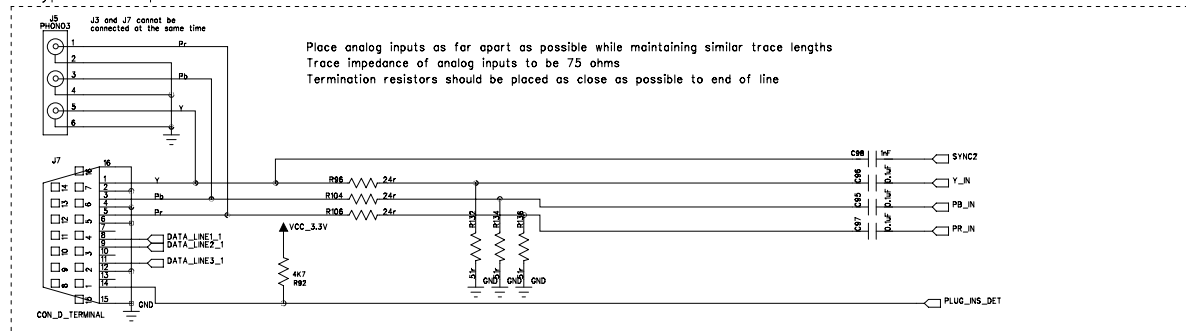
Eval Note

Appendix 1 – Schematics

VGA Connector

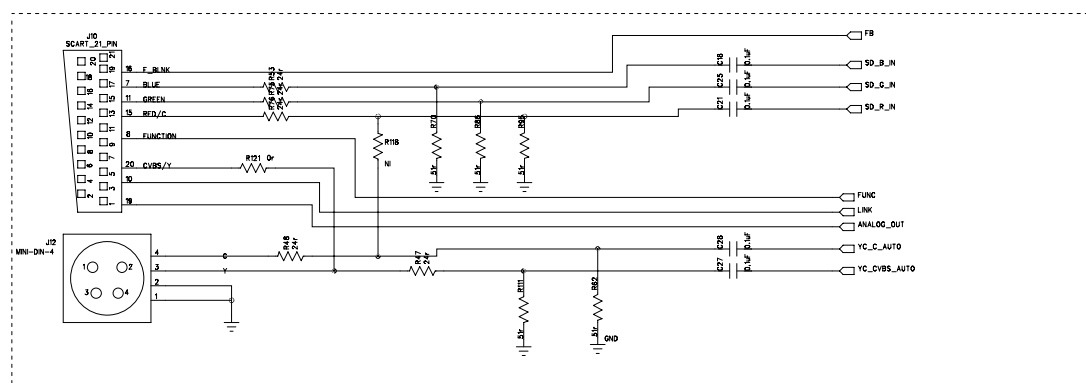


D-Type and Component Connectors

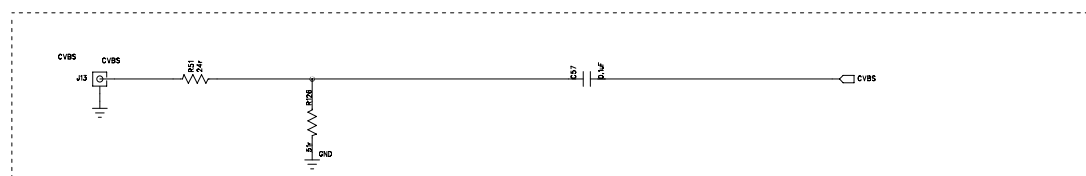


ADV7842 Analog Inputs (Graphics and Component)

SCART and S-VIDEO Connectors

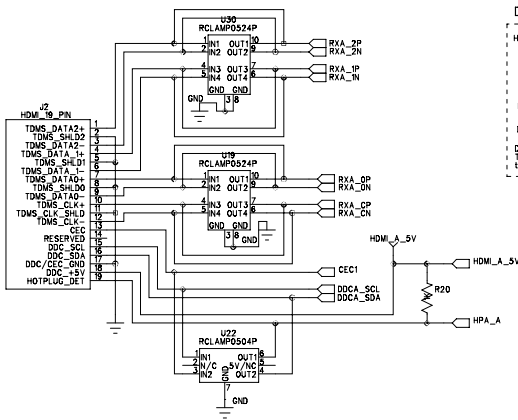


CVBS Connector

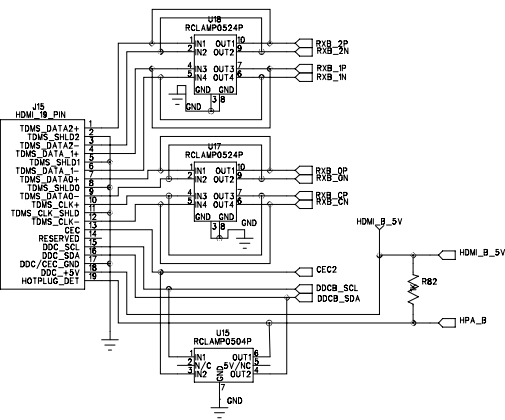


ADV7842 Analog Inputs (CVBS, S-Video and SCART)

Eval Note

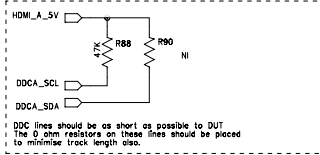


PCB Tracks for each differential pair must be tracked side by side
Each Diff pair should have 105R impedance between each other
PCB track lengths to connector should be minimum distance



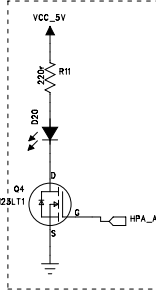
PCB Tracks for each differential pair must be tracked side by side
Each Diff pair should have 105R impedance between each other
PCB track lengths to connector should be minimum distance

DDC A Circuitry

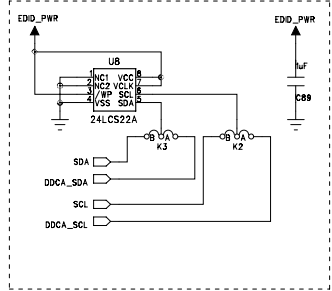


DDC lines should be as short as possible to DUT
The 0 ohm resistors on these lines should be placed to minimise track length also.

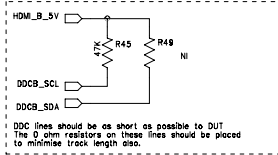
HPD A LED



EDID1

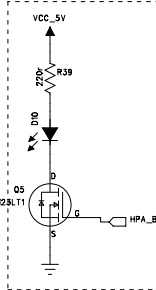


DDC B Circuitry

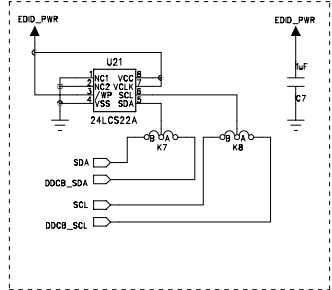


DDC lines should be as short as possible to DUT
The 0 ohm resistors on these lines should be placed to minimise track length also.

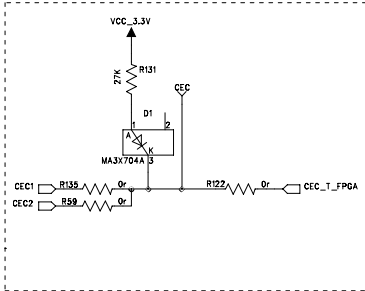
HPD B LED



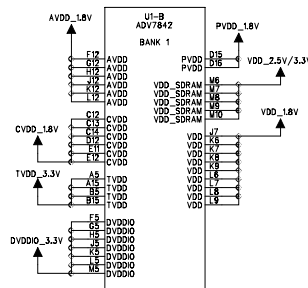
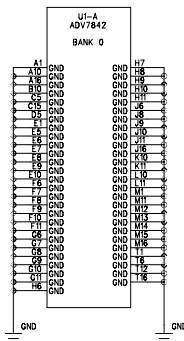
EDID2



CEC To 168-Pin Connector

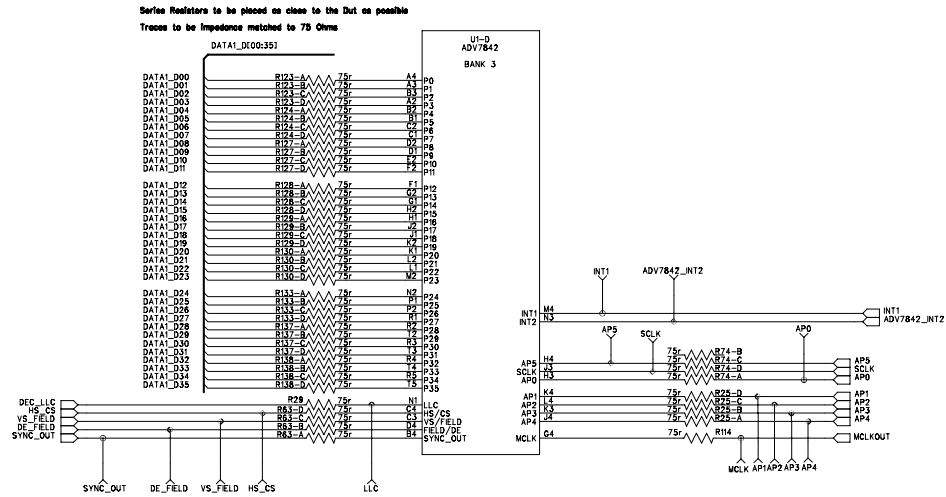


ADV7842 HDMI Inputs (Port A and Port B)

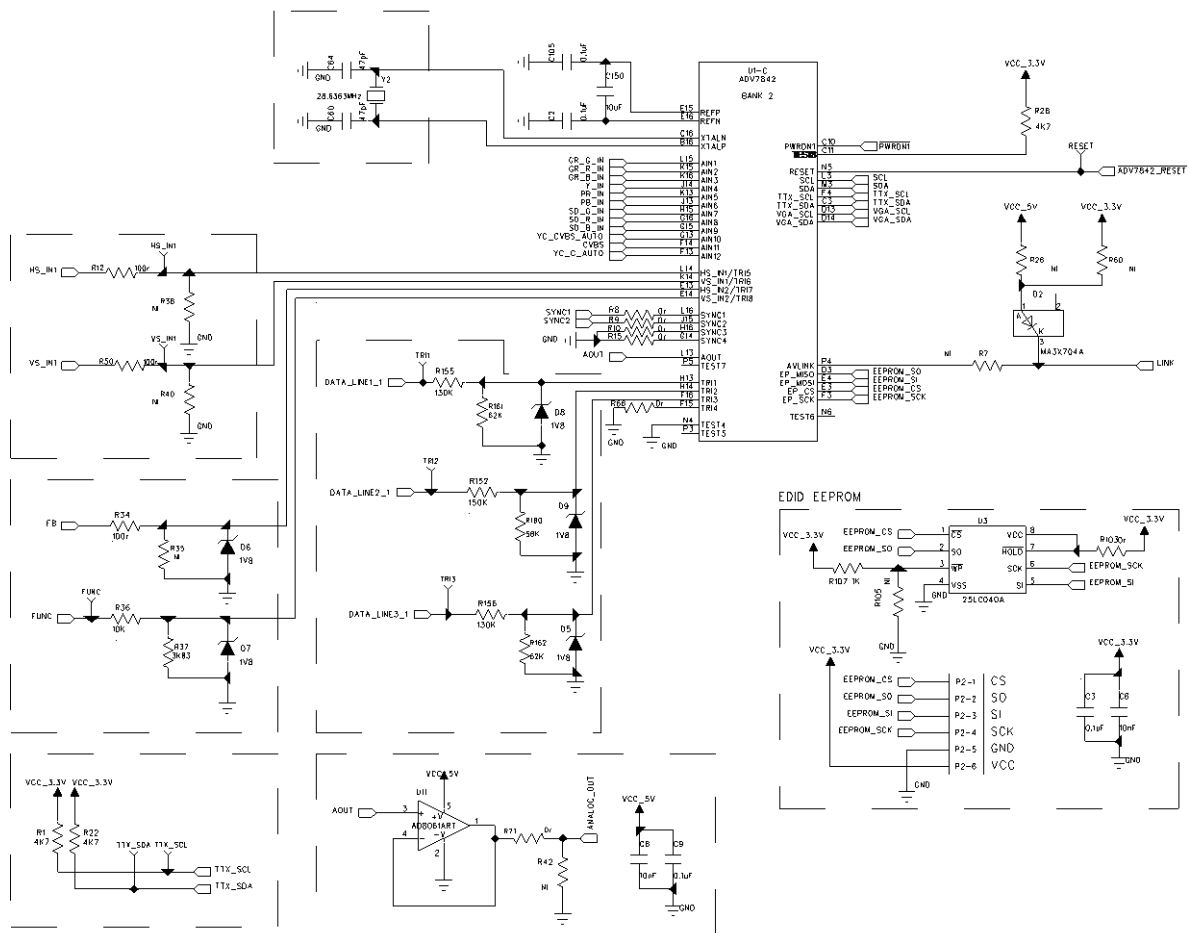


ADV7842 Power and Ground Connections

Eval Note

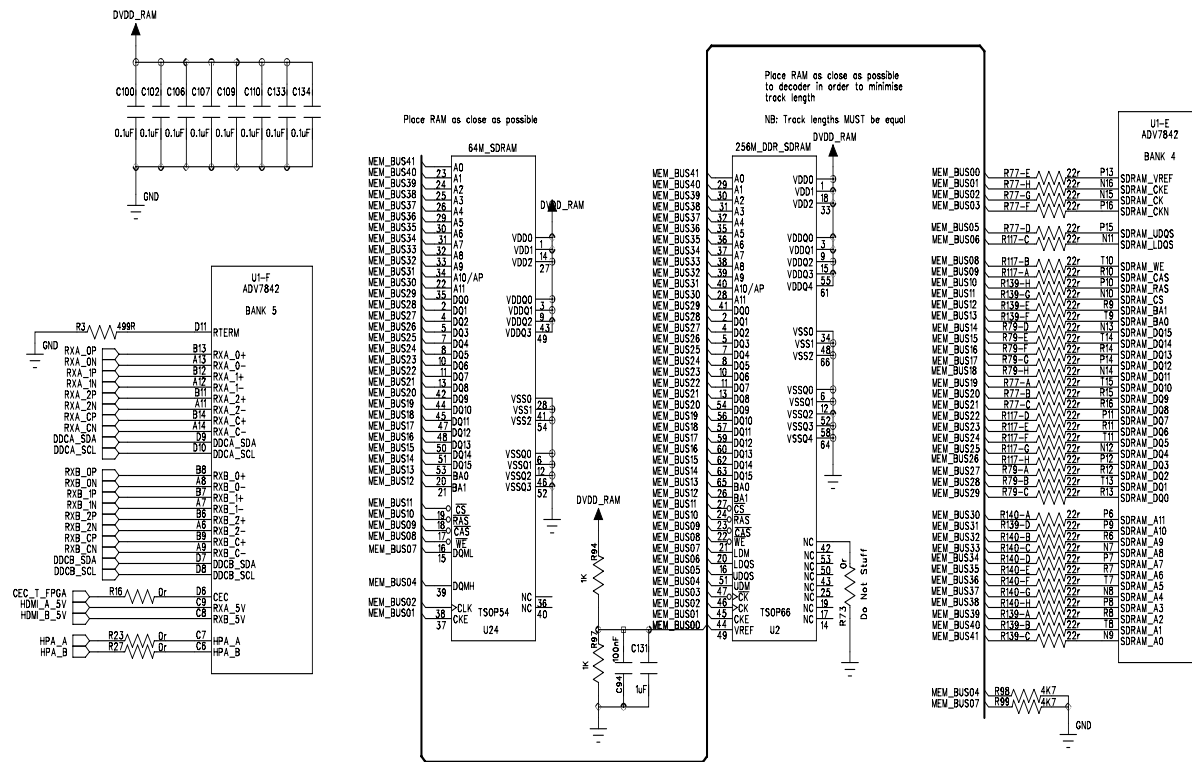


ADV7842 Pixel and Output Pins



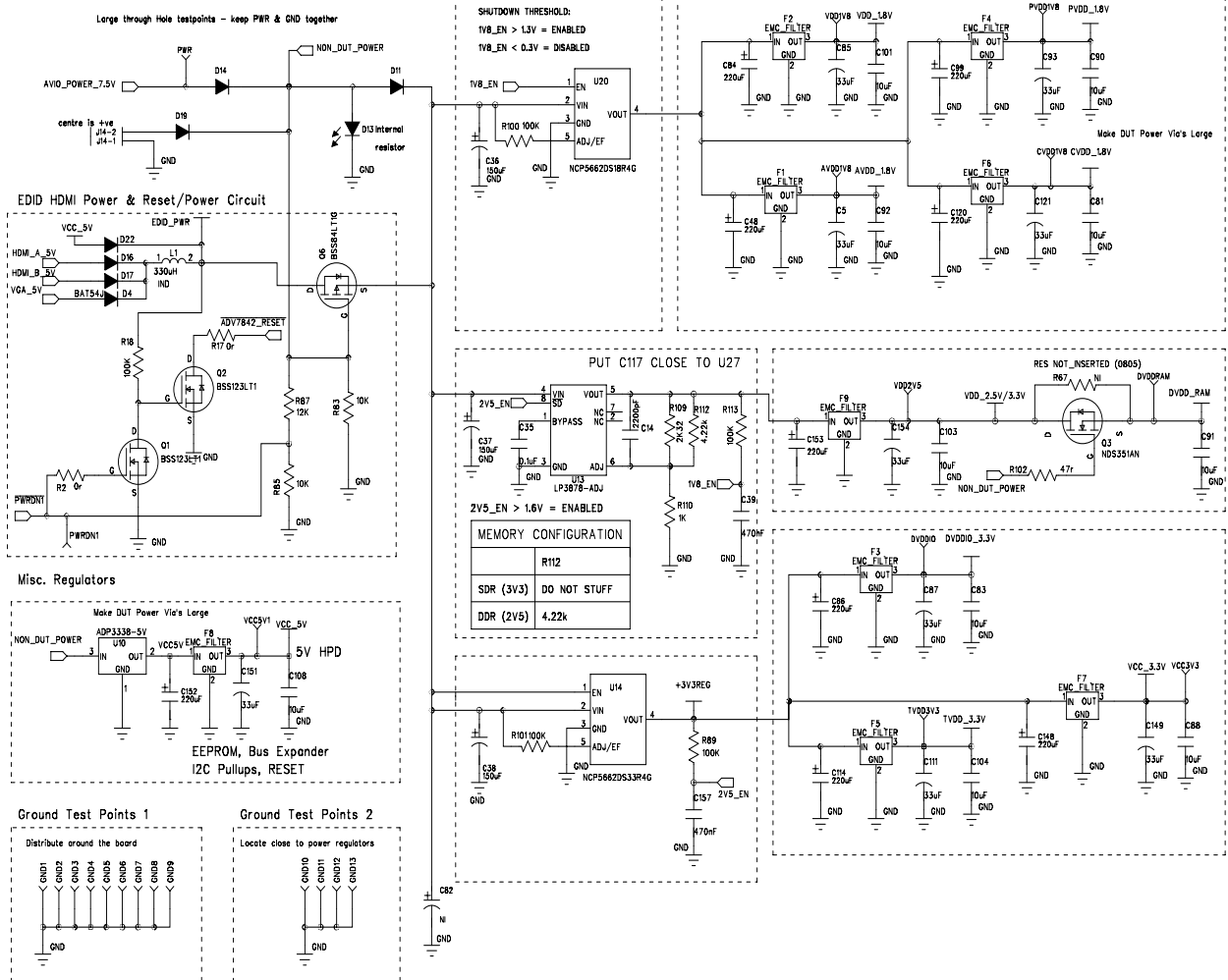
ADV7842 Input Pin Connections

Eval Note

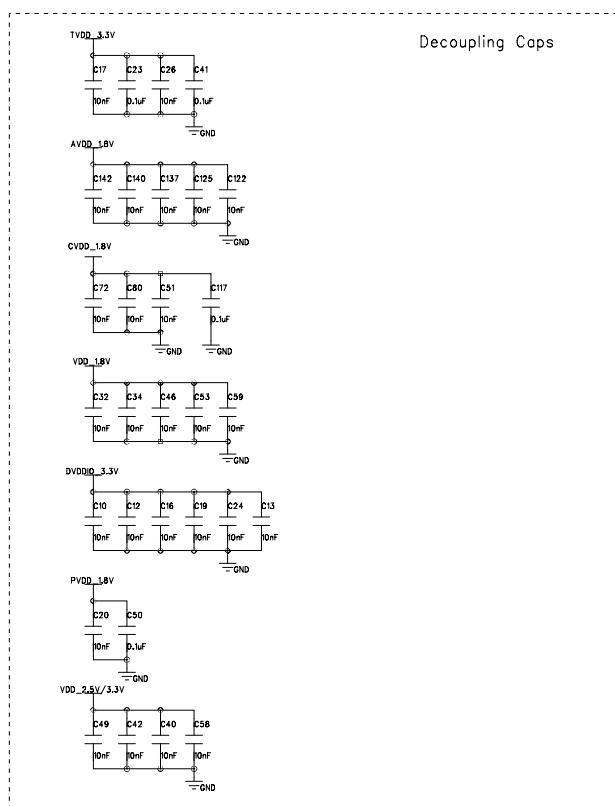
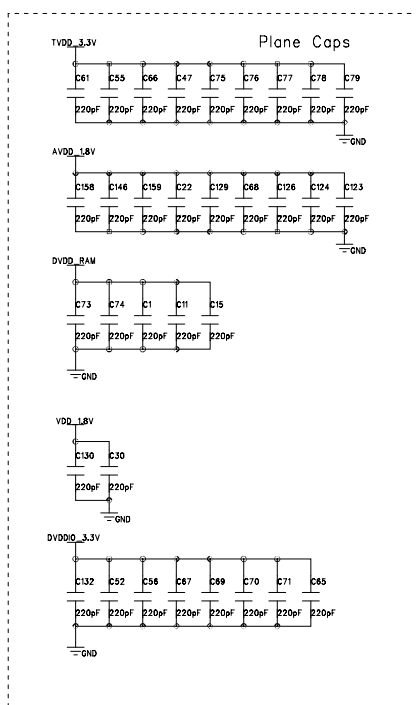


ADV7842 HDMI Input and Memory Connections

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Power Supply Circuitry for ADV7842



ADV7842 Power Supply decoupling Capacitors

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Appendix 2 – Downloading from FTP

Using an FTP client (e.g. Filezilla – <http://filezilla-project.org/download.php?type=client> - Analog Devices does not take responsibility for the content of any external sites), please log on to download the latest evaluation software.

Host: ftp.analog.com

Username: adv7842

Password: Supplied from FAE/product line

Port: leave empty (FTP client will automatically populate this)

