ADV7842/ADV7844
External Memory Test

INTRODUCTION

The ADV7842/ADV7844 contains a BIST (Built in Self-Test) for the external memory. This test can be used to test the operation of the external memory interface. It checks the connections between the ADV7842/ADV7844 and the external DDR memory. The test is controlled through I2C and the test results can be read back through registers within the ADV7842/ADV7844.

TEST OPERATION

The memory BIST test generates an LFSR sequence of numbers which is output to the external memory. This sequence is read back from the external memory and checked for errors. This test is internally generated and does not need any external inputs applied. It can also be carried out in circuit. It is recommended that a hardware reset is carried out before the memory BIST test is executed.

TEST SETUP

The following writes should be carried out in this order:

40 00 01	Program SDP 4x1
40 01 00	Program SDP mode
4C 80 92	SDP Recommended Write
4C 9B 01	SDP Recommended Write ADV784x
4C 9C 60	SDP Recommended Write ADV784x
4C 9E 02	SDP Recommended Write ADV784x
4C A0 0B	SDP Recommended Write ADV784x
4C C3 02	Memory BIST Initialisation
40 0C 40	Power up ADV784x
40 15 BA	Enable outputs
90 12 00	Disable 3D comb, Frame TBC & 3DNR
40 FF 04	Reset memory controller

Wait 5ms

90 12 00	Disable 3D Comb, Frame TBC & 3DNR
94 2A 01	Memory BIST Initialisation
94 7C 19	Memory BIST Initialisation
94 80 87	Memory BIST Initialisation
94 81 4a	Memory BIST Initialisation
94 82 2C	Memory BIST Initialisation
94 83 0E	Memory BIST Initialisation
94 84 94	Memory BIST Initialisation
94 85 62	Memory BIST Initialisation
94 7D 00	Memory BIST Initialisation
94 7E 1A	Memory BIST Initialisation

Wait 5ms

94 D9 D5	Enable BIST Test
90 12 05	Enable FRAME TBC & 3D COMB

Test Results

SDP_IO Map Register 0xDB [4] – Test has completed.
SDP_IO Map Register 0xDB [5] – Failed if this bit is 1

Once the memory test is initialized, the test will run continuously until the ADV7842/ADV7844 receives a hardware reset. The completed bit will be set once a single memory transaction has been completed, but the test will run continuously. It is recommended to run the test for at least 200ms. Once the test reports a failure, the pass/fail bit is latched high will not be reset until the ADV7842/ADV7844 is reset or the complete test is run again. It is recommended that a hardware reset is carried out after the memory BIST test is executed before the ADV7842/ADV7844 is configured in a standard mode.

REVISION HISTORY

09/09 – Revision 0 : Initial Version

LEGAL TERMS AND CONDITIONS