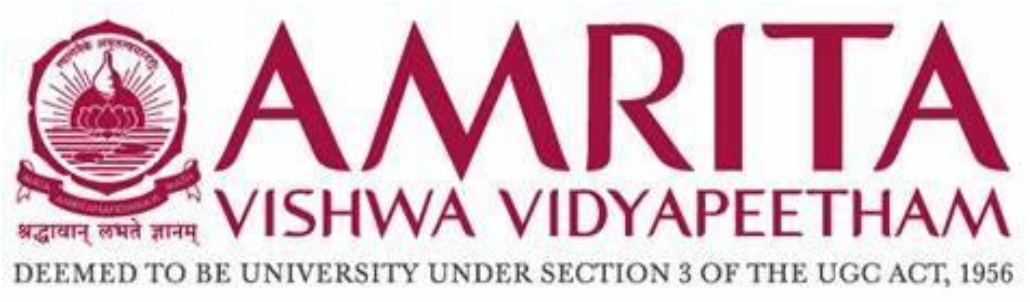

AMRITA SCHOOL OF ENGINEERING,

BENGALURU

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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Seminar

Project Report

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Introduction

In modern digital systems, balancing performance with power efficiency has become a key challenge. Approximate computing offers a promising solution by allowing small errors in computation to gain significant improvements in speed, area, and energy use. This project explores the design of approximate multipliers and adders using majority logic-based methods, aiming to enhance hardware efficiency while maintaining acceptable computational accuracy (80–90%). The approach is implemented and tested on FPGA hardware for real-time validation.

Problem Description:

Traditional multipliers and adders in digital circuits consume significant power and area. This project addresses the problem by designing approximate arithmetic units—specifically, adders and compressors using majority logic—that reduce circuit complexity and power usage without greatly affecting accuracy. Different configurations of majority logic-based full adders are analysed, and the best-performing designs (in terms of Mean Absolute Error and Normalized Mean Error Distance) are selected for multiplier implementation. The final design is verified through simulation and hardware testing on a Basys-3 FPGA board.

Motivation & Relevance:

With growing demand for efficient hardware in edge computing, majority logic enables low-power, high-speed approximate arithmetic. This project aligns with Goal 7 (Clean Energy) and Goal 9 (Industry, Innovation, and Infrastructure) by promoting sustainable and resource-efficient digital design, validated through FPGA implementation.

Alignment with UN SDGs:

- SDG 07 - Affordable and Clean Energy
- SDG 09- Industry, Innovation, and Infrastructure
- SDG 12- Responsible Consumption and Production

Literature Survey

Title	Problem Addressed	Current State of Art	Gaps Addressed
[1] W. Liu et al., "Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers," *IEEE Transactions on Emerging Topics in Computing*, vol. 9, no. 3, pp. 1609–1624, 2021. DOI: 10.1109/TETC.2019.2929100	Reduce power consumption and improve computational efficiency in nanoscale technologies.	Proposed majority logic-based arithmetic circuits. Defined an "influence factor" to optimize complement bit selection. Demonstrated enhanced performance in hardware metrics and error resilience.	Requires exploration of advanced design schemes for better accuracy-power balance in future nanoscale applications.
[2] M. Pokharia et al., "Power-Efficient Approximate Multipliers Leveraging Hybrid CMOS-Memristor Paradigm," *APCCAS 2023*, Hyderabad, India. DOI: 10.1109/APCCAS60141.2023.00032	Develop power-efficient approximate multipliers suitable for edge computing.	Designed approximate 4-2 compressors and multipliers using hybrid CMOS-memristor logic. Achieved ~90% power and 50% area savings. Emphasized accuracy-performance trade-offs.	Potential for scaling to higher-order multipliers for complex tasks like image processing remains unexplored.
[3] A. Singh et al., "Design of a 4–2 Compressor based Approach for Efficient Approximate Multiplier Design," *ICITEICS 2024*, Bangalore, India. DOI: 10.1109/ICITEICS61368.2024.10625587	Enhance multiplier efficiency by reducing energy and delay.	Introduced novel 4-2 compressors within Wallace tree architecture. Reported ~68.84% delay and ~40.34% area reduction.	Further optimization by integrating memory elements or shifters for complete arithmetic units is suggested.

Breadth of the Literature Survey:

1. Approximate Computing in Arithmetic Circuits

- Explores the application of approximate logic in adders and multipliers to reduce hardware complexity and energy consumption.
- Majority logic-based arithmetic and approximate 4–2 compressor designs are covered as strategies to achieve trade-offs between accuracy and efficiency.

2. Emerging Technologies: Memristors & Hybrid Approaches

- Investigation into hybrid CMOS-memristor implementations for logic gates and arithmetic units tailored to energy-constrained environments.
- Studies show memristor-aided logic can drastically reduce area and power, paving the way for edge-oriented designs.

3. Compressor-Based Multiplier Design

- Focus on 4–2 compressor designs embedded in Wallace tree multipliers to minimize critical path delays.
- Novel compressor logic strategies that optimize performance while maintaining acceptable approximation error levels are emphasized.

4. Power and Area Optimization

- Analysis of power-efficient design choices across multiplier architectures, including quantification of savings (up to 90% power and 50% area).
- Targeted primarily at low-power hardware like IoT and edge AI platforms.

5. Application Contexts and Future Scope

- Broad coverage of applications in nanotechnology, image processing, and edge computing.
- Suggestions for future enhancements include scaling designs to higher-order multipliers and integrating memory or shifting elements to complete processing pipelines.

Depth of the Literature Survey:

1. Technical Depth in Logic Design

- Compared traditional CMOS-based designs with approximate computing techniques leveraging majority logic or hybrid CMOS-memristor structures.
- Explored bit-level error resilience and influence factor optimization to reduce redundant toggles and boost efficiency.

2. Architectural Analysis of Multipliers

- Dissected architectural improvements in Wallace tree multipliers using approximate compressors.
- Analysed trade-offs in timing (delay reductions up to 68.84%) and chip area (savings over 40%) while preserving core computation integrity

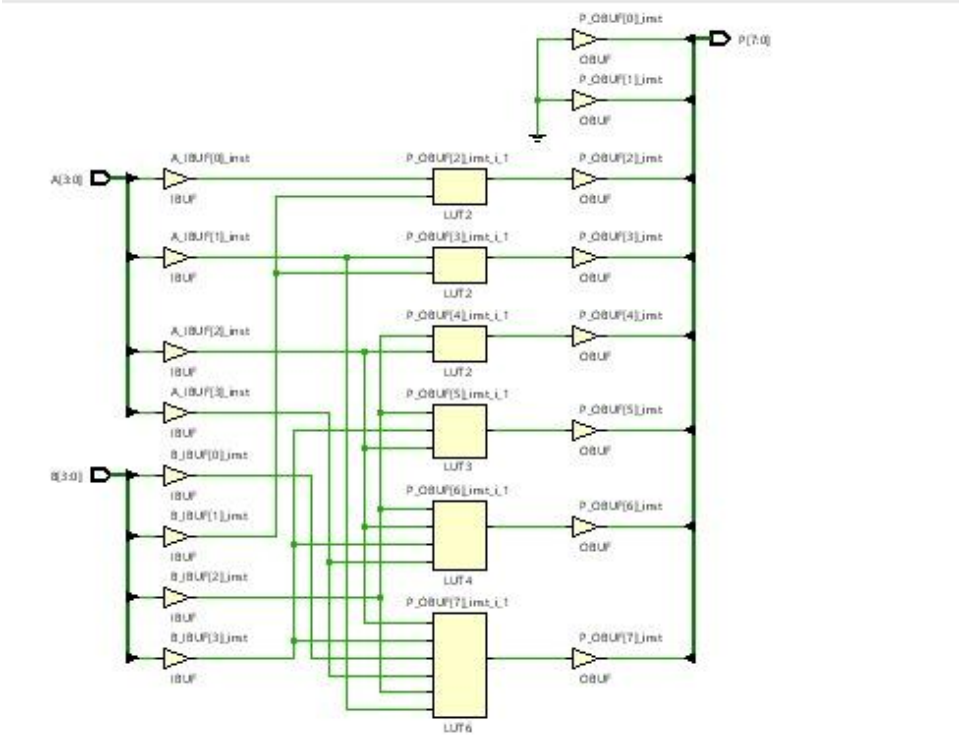
3. Algorithm-Level Innovations

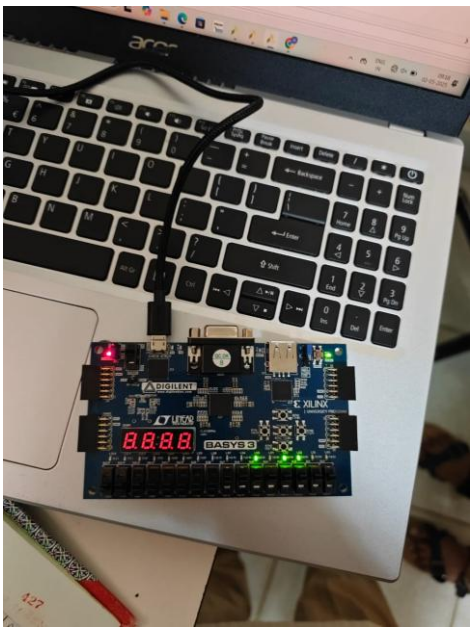
- Evaluated how logic-level innovations such as the influence factor (Liu et al.) and hybrid logic (Pokharia et al.) improve error-tolerant designs.
- Studied compressor output approximation control mechanisms and their effect on final multiplier fidelity.

4. Toolchain and Hardware Metrics Evaluation

- Metrics such as delay, power, area, and hardware resilience were compared quantitatively across designs.
- Realistic simulation results were considered to measure impact on edge-computing suitability, providing a hardware-aware perspective.

Available Methodologies:





System Overview:

The proposed system focuses on designing an energy-efficient approximate multiplier using majority logic, aimed at reducing hardware complexity and power consumption in digital systems. By integrating optimized majority-based adders and compressors, the multiplier is suitable for low-power applications such as IoT devices, portable electronics, and edge computing platforms. The design is verified using simulation tools and is intended for real-time deployment using FPGA hardware.

Key Components:

- FPGA Board

Control Logic:

The multiplier design begins with selecting the best-performing approximate adder (MLAFA21) and compressor (MLAC11) based on error metrics like MAE and NMED. These components are integrated into a structured multiplier circuit and coded in Verilog. Using Xilinx Vivado, the logic is synthesized, simulated, and debugged to ensure correct arithmetic behaviour and low power usage. The control flow includes input processing, parallel multiplication using majority logic units, and final output generation with reduced switching activity.

Energy Efficiency and Scalability:

Energy efficiency is achieved through the use of simplified majority logic circuits, which reduce gate count and delay. This not only lowers power consumption but also enhances speed. The design is scalable, allowing it to be extended for higher-order multiplication or embedded in larger VLSI systems. The hardware implementation using FPGA ensures reconfigurability and real-time performance, supporting a wide range of applications in modern digital and embedded systems.

Results

- Among the tested designs, MLAFA21 (adder) and MLAC11 (compressor) provided the best balance between accuracy and efficiency.
- Optimized components were integrated to design an energy-efficient approximate multiplier.
- Simulation using Xilinx Vivado confirmed its correct operation and reduced hardware complexity.
- The final design maintained 80–90% accuracy, suitable for low-power digital applications.

Conclusion:

- The project proved that majority logic-based approximate multipliers can effectively balance performance and power efficiency.
- Through analysis, the best-performing adder (MLAFA21) and compressor (MLAC11) were selected based on their accuracy and hardware efficiency.
- The final design is both resource-efficient and accurate, making it suitable for various real-world digital applications.

References:

[1] W. Liu, T. Zhang, E. McLarnon, M. O'Neill, P. Montuschi and F. Lombardi, "Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers, " in IEEE Transactions on Emerging Topics in Computing, vol. 9, no. 3, pp. 1609-1624, 1 July-Sept. 2021, doi: 10.1109/TETC.2019.2929100.

[2] M. Pokharia, R. S. Hegde and J. Mekie, "Power-Efficient Approximate Multipliers Leveraging Hybrid CMOS-Memristor Paradigm, " 2023 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Hyderabad, India, 2023, pp. 95-99, doi: 10.1109/APCCAS60141.2023.00032.

[3] A. Singh, A. V. Reddy, M. U. Kumar, E. Chitra, V. Marudhai and R. Mishra, "Design of a 4–2 Compressor-based Approach for Efficient Approximate Multiplier Design, " 2024 IEEE International Conference on Information Technology, Electronics and Intelligent Communication Systems (ICITEICS), Bangalore, India, 2024, pp. 1-7, doi: 10.1109/ICITEICS61368.2024.10625587.

[4] Li, Z., Zhang, Z., Yang, J., Cao, R., & Chen, J. (2023, November). Method for FPGA-based Real-time Simulation Hardware Implementation. In 2023 10th International Forum on Electrical Engineering and Automation (IFEEA) (pp. 1226-1230). IEEE

[5] Guo, Y., Chen, X., Zhou, Q., & Sun, H. (2024, May). Power-Efficient and Small-Area Approximate Multiplier Design with FPGA-Based Compressors. In 2024 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1-5). IEEE.