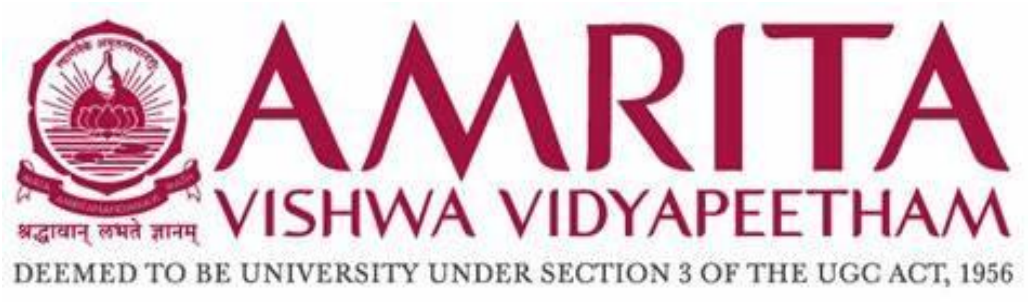


AMRITA SCHOOL OF ENGINEERING, BENGALURU

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

# B. TECH. VI SEMESTER AY 2024-2025

## 19ECE384

## Open Lab

## Project Report

***Submitted by***

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## Introduction:

In modern digital systems, balancing performance with power efficiency has become a key challenge. Approximate computing offers a promising solution by allowing small errors in computation to gain significant improvements in speed, area, and energy use. This project explores the design of approximate multipliers and adders using majority logic-based methods, aiming to enhance hardware efficiency while maintaining acceptable computational accuracy (80–90%). The approach is implemented and tested on FPGA hardware for real-time validation.

## Motivation & Relevance:

With growing demand for efficient hardware in edge computing, majority logic enables low-power, high-speed approximate arithmetic. This project aligns with Goal 7 (Clean Energy) and Goal 9 (Industry, Innovation, and Infrastructure) by promoting sustainable and resource-efficient digital design, validated through FPGA implementation.

## Problem Description:

Traditional multipliers and adders in digital circuits consume significant power and area. This project addresses the problem by designing approximate arithmetic units—specifically, adders and compressors using majority logic—that reduce circuit complexity and power usage without greatly affecting accuracy. Different configurations of majority logic-based full adders are analysed, and the best-performing designs (in terms of Mean Absolute Error and Normalized Mean Error Distance) are selected for multiplier implementation. The final design is verified through simulation and hardware testing on a Basys-3 FPGA board.

## Sub-Objective:

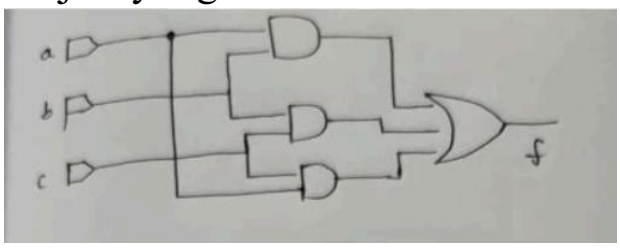
- Design of Approximate Adders
- Development of Approximate compressor
- Development of multiplier Factor Analysis with Simulation
- Hardware Implementation on FPGA board and Report

# Literature Survey:

| Title | Problem Addressed | Current State of Art | Gaps Addressed |
|---|---|---|---|
| [1] W. Liu et al., "Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers," *IEEE Transactions on Emerging Topics in Computing*, vol. 9, no. 3, pp. 1609–1624, 2021. DOI: 10.1109/TETC.2019.2929100 | Reduce power consumption and improve computational efficiency in nanoscale technologies. | Proposed majority logic-based arithmetic circuits. Defined an "influence factor" to optimize complement bit selection. Demonstrated enhanced performance in hardware metrics and error resilience. | Requires exploration of advanced design schemes for better accuracy-power balance in future nanoscale applications. |
| [2] M. Pokharia et al., "Power-Efficient Approximate Multipliers Leveraging Hybrid CMOS-Memristor Paradigm," *APCCAS 2023*, Hyderabad, India. DOI: 10.1109/APCCAS60141.2023.00032 | Develop power-efficient approximate multipliers suitable for edge computing. | Designed approximate 4-2 compressors and multipliers using hybrid CMOS-memristor logic. Achieved ~90% power and 50% area savings. Emphasized accuracy-performance trade-offs. | Potential for scaling to higher-order multipliers for complex tasks like image processing remains unexplored. |
| [3] A. Singh et al., "Design of a 4–2 Compressor based Approach for Efficient Approximate Multiplier Design," *ICITEICS 2024*, Bangalore, India. DOI: 10.1109/ICITEICS61368.2024.10625587 | Enhance multiplier efficiency by reducing energy and delay | Introduced novel 4-2 compressors within Wallace tree architecture. Reported ~68.84% delay and ~40.34% area reduction. | Further optimization by integrating memory elements or shifters for complete arithmetic units is suggested. |

## Methodology:

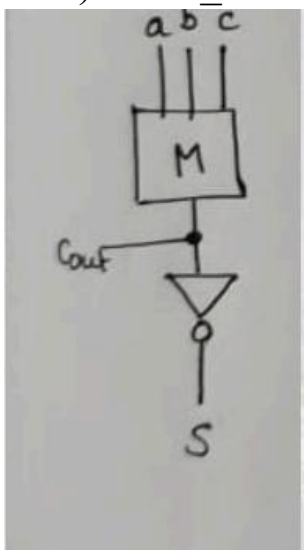
Majority logic circuit



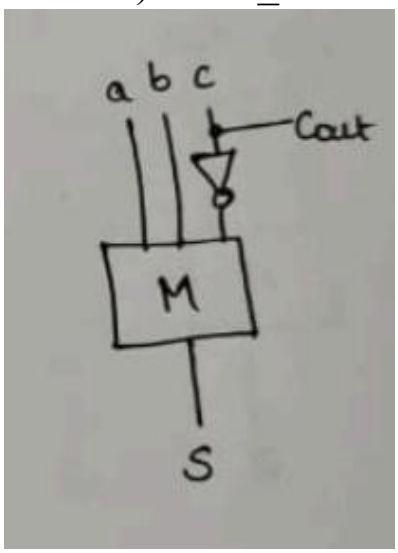

f=ab+bc+ca

We are creating two types of full adders with output complemented model and input(carry) complemented model to design adder and compressor using majority logic.

1) mlafa_1



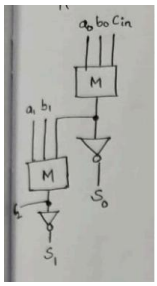

2) mlafa_2

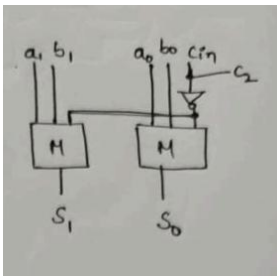


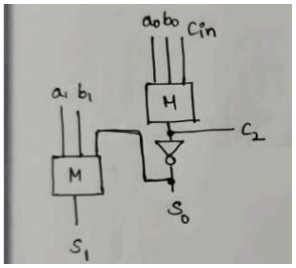

## Design of Adders Using Majority Logic

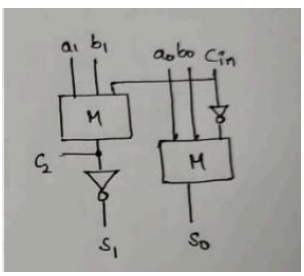
In this work, two individual majority logic-based full adders-mlafa1 and mlafa2 are developed. These full adders serve as building blocks for constructing approximate arithmetic circuits. By combining these units in different configurations, four distinct majority logic-based adders are generated:

1. mlafa11 2. mlafa22 3. mlafa12 4. mlafa21



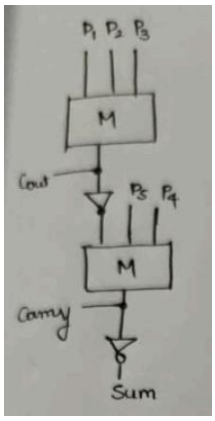



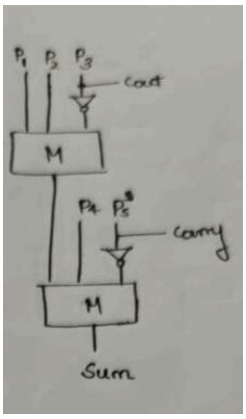
## Design of Compressors Using Majority Logic

In this work, two individual majority logic-based full adders-mlafa1 and mlafa2 are developed. These full adders serve as building blocks for constructing approximate arithmetic circuits. By combining these units in different configurations, four distinct majority logic-based compressors are generated:

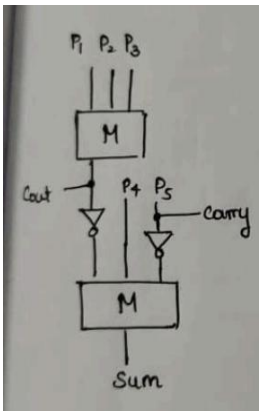
1. mlac11



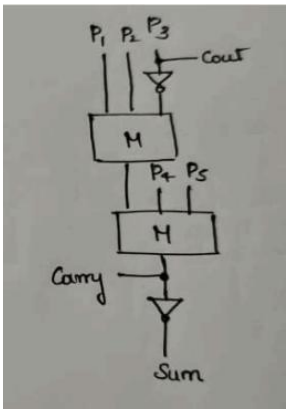

2. mlac22




3. mlac12




4. mlac21




## Design of Approximate Multiplier Using Majority Logic

The approximate multiplier is designed by integrating optimized majority logic-based components—specifically, the selected MLAFA21 adder and MLAFA11 compressor. These components were chosen based on their favourable error metrics (lower MAE and NMED), ensuring a good trade-off between accuracy and hardware efficiency. The architecture leverages the simplicity of majority logic to reduce power consumption and circuit complexity, making it well-suited for low-power applications. The overall multiplier structure was verified through simulation and is prepared for FPGA-based hardware implementation.

# Feasibility and Novelty:

- **Majority Logic for Efficient Design:**
  The project introduces majority logic (ML) into the design of approximate multipliers, which reduces circuit complexity and power consumption while maintaining acceptable accuracy.
- **Optimized Accuracy vs Efficiency:**
  The design balances accuracy and resource usage, achieving good enough results for many applications while saving energy and reducing hardware complexity.

# Simulation

### Simulation Setup:

- Xilinx Vivado is used for simulating the design of approximate multipliers and adders using majority logic.
- The tool supports design synthesis, timing analysis, and functional verification of Verilog code.
- This simulation ensures correctness and performance analysis before moving to FPGA hardware implementation.

### Adder Analysis:

| Types Of Adders | MAE | NMED |
|---|---|---|
| MLAFA11 | 3 | 0.107 |
| MLAFA22 | 3 | 0.107 |
| MLAFA12 | 2 | 0.089 |
| MLAFA21 | 2 | 0.089 |

From the above analysis, it is observed that MLAFA12 and MLAFA21 outperform the other two configurations by achieving lower MAE and NMED values, indicating better approximation accuracy.

Hence, MLAFA21 was selected for the next stage of design, i.e., integration into the compressor and multiplier modules, as it provides a good balance between simplicity and accuracy

### Compressor Analysis:

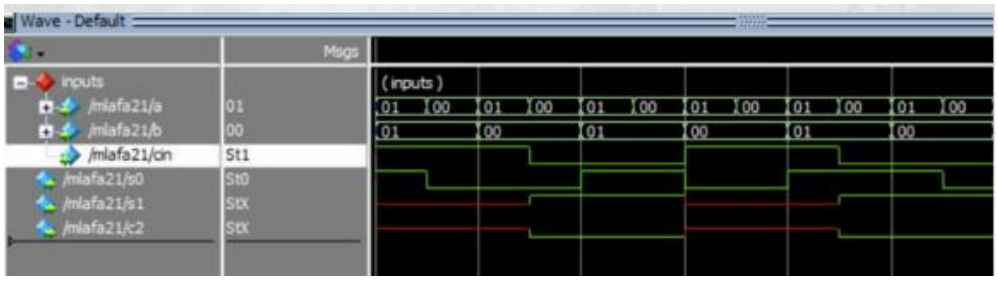
| Types of Compressors | MAE | NMED |
|---|---|---|
| MLAFA11 | 1 | 0.075 |
| MLAFA22 | 2 | 0.1 |
| MLAFA12 | 1 | 0.075 |
| MLAFA21 | 2 | 0.1 |

From the analysis, both MLAFA11 and MLAFA12 demonstrate better performance with lower error values, making them more suitable for approximate designs.

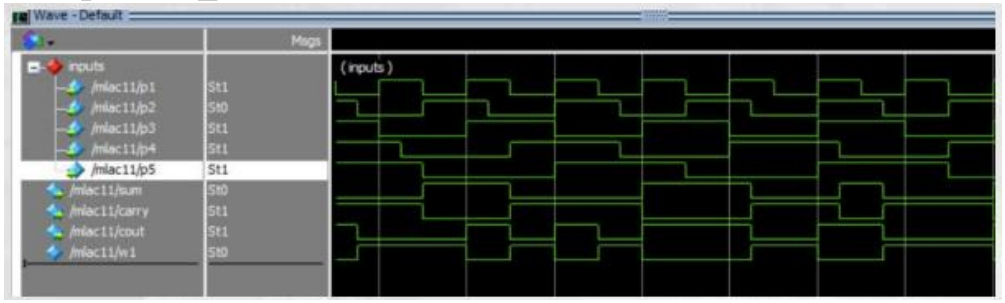
Considering overall design compatibility and optimization, MLAFA11 was selected as the compressor configuration to be used in the final multiplier architecture.

## Simulation Output:

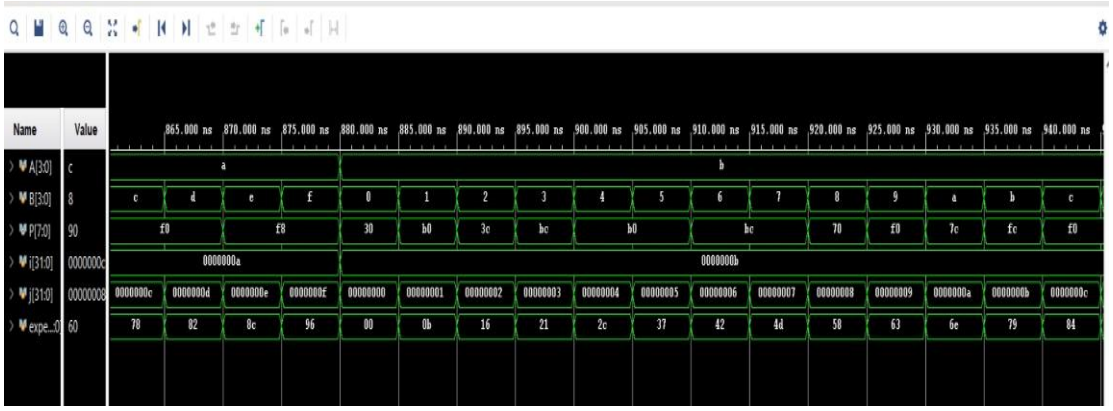
### Adder_MLAFA21:




### Compressor_MLAFA11:




### Output:



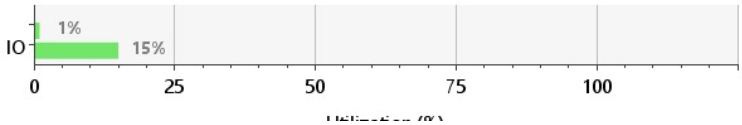

```
11    6   188        66      NO
11    7   188        77      NO
11    8   112        88      NO
11    9   240        99      NO
11   10   124       110      NO
11   11   252       121      NO
11   12   240       132      NO
11   13   240       143      NO
11   14   252       154      NO
11   15   252       165      NO
12    0    48         0      NO
12    1   176        12      NO
12    2    48        24      NO
```

In most cases, the approximate multiplier produces outputs close to the accurate results. Since majority logic is used for 2–3 of the partial products, the final output often matches the accurate result. As a result, the observed accuracy is approximately 72.5%, and the output comparison may not show significant differences due to this consistency in approximate values.

## Synthesis:

### Area

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 4 | 20800 | 0.02 |
| IO | 16 | 106 | 15.09 |

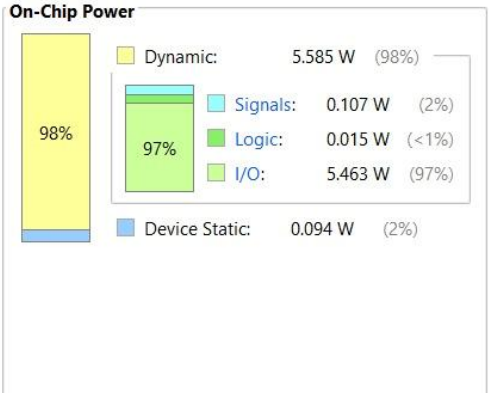



### Power

**Summary**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **5.679 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **53.4°C** |
| Thermal Margin: | 31.6°C (6.3 W) |
| Effective ϑJA: | 5.0°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |




### Timing

**Design Timing Summary**

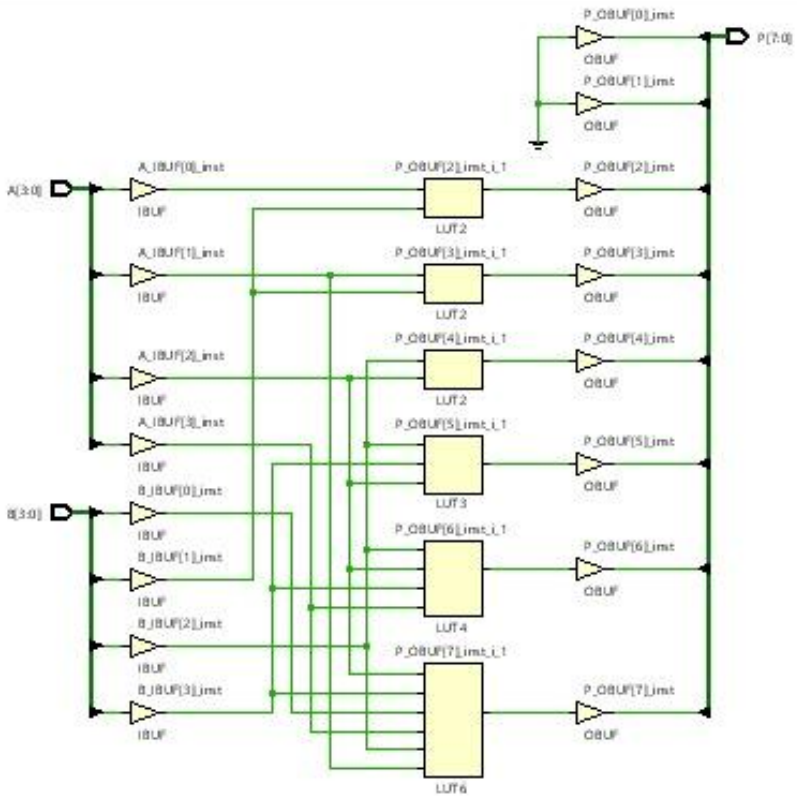
| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | inf | Worst Hold Slack (WHS): | inf | Worst Pulse Width Slack (WPWS): | NA |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | NA |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | NA |
| Total Number of Endpoints: | 6 | Total Number of Endpoints: | 6 | Total Number of Endpoints: | NA |

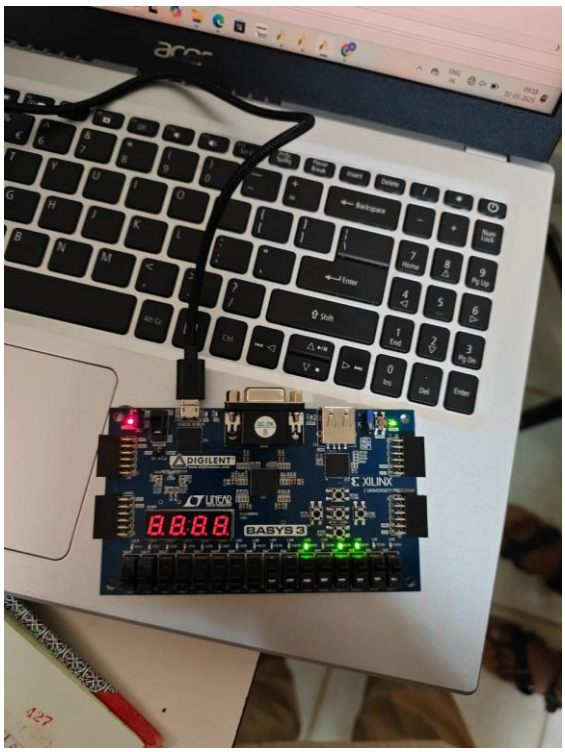
**There are no user specified timing constraints.**

### Hardware Cost:

| S. No | Component | Quantity | Unit Cost (INR) | Total Cost (INR) |
|---|---|---|---|---|
| 1 | FPGA (Basys-3) | 1 | 9200 | 9200 |
| Total | | | | 9200 |

# Hardware Implementation:



## Results

- Among the tested designs, MLAFA21 (adder) and MLAC11 (compressor) provided the best balance between accuracy and efficiency.
- Optimized components were integrated to design an energy-efficient approximate multiplier.
- Simulation using Xilinx Vivado confirmed its correct operation and reduced hardware complexity.
- The final design maintained 80–90% accuracy, suitable for low-power digital applications.

## Analysis / Interpretation:

- MAE and NMED were used as primary error metrics.
- MLAFA21 and MLAC11 had the lowest error rates compared to other configurations.
- Majority logic circuits significantly reduced gate count and delay, making them suitable for energy-efficient systems.
- The FPGA simulation confirmed hardware feasibility and resource optimization.

## Conclusion:

- The project proved that majority logic-based approximate multipliers can effectively balance performance and power efficiency.
- Through analysis, the best-performing adder (MLAFA21) and compressor (MLAC11) were selected based on their accuracy and hardware efficiency.
- The final design is both resource-efficient and accurate, making it suitable for various real-world digital applications.

## Challenges:

- Selecting optimal logic configurations required trial and error with multiple simulations.
- Ensuring accuracy within acceptable limits while still achieving hardware efficiency was challenging.
- Integrating the design into FPGA needed careful timing and debugging

## Future Scope:

- Advanced Multiplier Architectures for High-Precision Applications
- Real-Time Processing in Edge Devices
- Scalable Hardware for Next-Gen Digital Systems

## References:

[1] W. Liu, T. Zhang, E. McLarnon, M. O'Neill, P. Montuschi and F. Lombardi, "Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers, " in IEEE Transactions on Emerging Topics in Computing, vol. 9, no. 3, pp. 1609-1624, 1 July-Sept. 2021, doi: 10.1109/TETC.2019.2929100.

[2] M. Pokharia, R. S. Hegde and J. Mekie, "Power-Efficient Approximate Multipliers Leveraging Hybrid CMOS-Memristor Paradigm, " 2023 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Hyderabad, India, 2023, pp. 95-99, doi: 10.1109/APCCAS60141.2023.00032.

[3] A. Singh, A. V. Reddy, M. U. Kumar, E. Chitra, V. Marudhai and R. Mishra, "Design of a 4–2 Compressor-based Approach for Efficient Approximate Multiplier Design, " 2024 IEEE International Conference on Information Technology, Electronics and Intelligent Communication Systems (ICITEICS), Bangalore, India, 2024, pp. 1-7, doi: 10.1109/ICITEICS61368.2024.10625587.

[4] Li, Z., Zhang, Z., Yang, J., Cao, R., & Chen, J. (2023, November). Method for FPGA-based Real-time Simulation Hardware Implementation. In 2023 10th International Forum on Electrical Engineering and Automation (IFEEA) (pp. 1226-1230). IEEE.

[5] Guo, Y., Chen, X., Zhou, Q., & Sun, H. (2024, May). Power-Efficient and Small-Area Approximate Multiplier Design with FPGA-Based Compressors. In 2024 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1-5). IEEE.