Study of Via Optimization Problem Based on Estimation of Distribution Algorithm

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***Abstract*-Optimizing the number of vias is an important approach for improving the performance and the yield of printed circuit boards (PCBs). To optimize the vias of multi-layer PCBs, first, we converted the circuit routing diagram into an undirected weighted topology. Then, the mathematical model of the via optimization problem was established on the basis of the topological weight segmentation method. Finally, it was solved using estimation of distribution algorithm (EDA). Compared with the traditional methods, the proposed method was intuitive and easy to implement with no invalid solution existing in the intermediate process and with high operation efficiency. The simulation experiments demonstrated that the proposed algorithm could effectively solve the via optimization problem, and EDA had faster convergence and better effectiveness than the genetic algorithm (GA).**

Keywords-via optimization; topological graph; estimation of distribution algorithm（EDA）; genetic algorithm（GA）

I. INTRODUCTION

As the number of nodes per unit area on a chip continues to increase, the fabrication of large-scale integrated circuits becomes increasingly challenging[1]. Most of the problems encountered in integrated circuit routing are double-layer or multi-layer routing problems. Most of the routing algorithms restrict each layer with only one direction; that is, all the horizontal segments are placed on one layer, and all the vertical segments are placed on the adjacent layer. The necessary electrical connections between the two layers are implemented with vias, as shown in Fig.1, where the solid lines indicate the segments on the horizontal layer, the dotted lines indicate the segments on the vertical layer, and the small black dots are the vias.

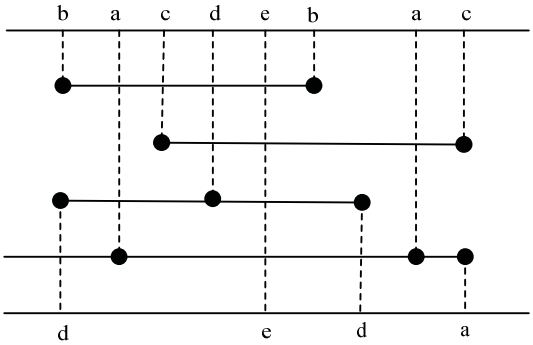

Fig. 1 Circuit routing diagram with the horizontal and vertical layering rule

It has been proven that this horizontal and vertical layering rule is very effective in improving the completion rate and the uniformity of routing. As the segments of different nets cannot intersect on the same layer (as shown in Fig.1, the segments connected to net a and the segments connected to net b cannot intersect on the same layer), many nets need to be routed on both layers. A large number of vias are thereby introduced. However, the existence of a large number of vias has the following effects: First, the wiring resistance and capacitance are increased, which reduce the circuit performance; second, as the sizes of the vias are relatively large, more routing resources are consumed; third, excessive vias reduce the robustness of the circuit and the yield of the PCB. Therefore, it is necessary to optimize the vias after finishing the routing. For a circuit design with the completed routing, the via optimization problem is as follows: how can we obtain a reasonable layering approach (without limiting the routing direction on each layer of the circuit) without changing the plane position of all the segments, which minimizes the number of vias?

The via optimization problem was first proposed by A. Hashimoto and J. Stevens in 1977[2]. As the via optimization problem is an NP-hard problem[3], many researchers have used heuristic algorithms such as GA and simulated annealing algorithm to solve it. In [4], the transposition matrix was used to map the problem to the corresponding neural network, and thus, the via optimization in multilayer routing was solved using the Hopfield network. In [5], GA was adopted to investigate the via optimization problem, and better results than those of the deterministic constraint algorithm were obtained. In [6], the researchers proposed a multiple graphing method to optimize the vias.

In this paper, a new method for solving the via optimization problem is proposed. The basic process is as follows: first, convert the circuit routing diagram into an undirected weighted topology, and then, build a mathematical model for the via optimization problem on the basis of the topological weight segmentation method. Finally, the via optimization problem is solved using EDA. Compared with the existing algorithms, the main advantages of the proposed algorithm are as follows: (1) The method is intuitive, easy to understand, and easy to implement. (2) All of the individuals in the group generated by the algorithm are valid solutions, there is no invalid solution, and hence, the operation efficiency is high. (3) EDA-based solution of the via optimization problem has faster convergence and better effectiveness than GA.

978-1-7281-4653-9/19/$31.00 ©2019 IEEE
DOI 10.1109/ISCID.2019.10102

The rest of this paper is organized as follows: Section 2 establishes the mathematical model for the via optimization problem on the basis of the topological model. Section 3 discusses the simulation experiments of the via optimization problem based on EDA and compares the results with those obtained using the traditional GA. Finally, the conclusions are presented in Section 4.

II. Mathematical Model of Via Optimization Problem

For the convenience of discussion, several key terminologies are defined first.

1) Via: lead hole connecting the segments on different layers of the circuit board belonging to the same net.

2) Segment: whole or a part of a net, whose two end points are vias or end nodes.

3) Intersection point: intersection of segments belonging to different nets (the segments are on different layers).

A. Topological graph of Via Optimization Problem

For the convenience of establishing a mathematical model for the via optimization problem, the circuit routing diagram was first converted to an undirected weighted topological model. For the circuit routing diagram shown in Fig.1, the topological graph was built as follows:

1) Eliminate non-essential vias

Some vias that were non-essential after the horizontal and vertical layering restrictions were removed. The segments connecting b in Fig. 1 could be placed on the same layer when the horizontal and vertical layering restrictions were removed. Thus, the two vias on the net became non-essential. After eliminating non-essential vias, we converted the routing diagram in Fig. 1 into the one shown in Fig. 2.

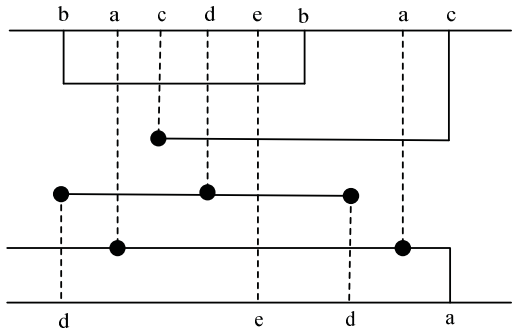

Fig. 2 Circuit routing diagram after eliminating non-essential vias

2) Mark the intersection points

All the intersection points in the circuit routing diagram shown in Fig. 2 were sequentially marked (12 intersection points in all), and the circuit routing diagram with the marked intersection points is shown in Fig. 3.

3) Establish the topological graph

A topological graph of the via optimization problem (undirected weighted map) was established on the basis of Fig. 3. Assume that the topological graph that was required to be established was $G=(V,E)$, where $V=\{1,2,\cdots,n\}$ denotes

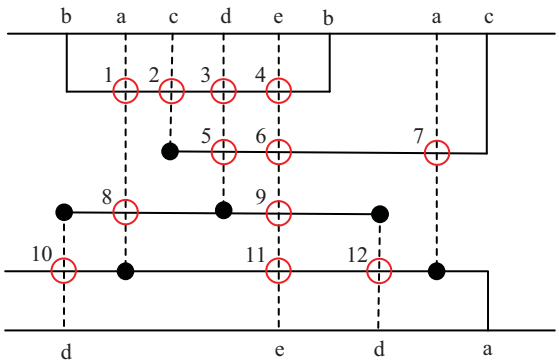

Fig. 3 Circuit routing diagram with marked intersection points

the set of the largest vertices, $E\subseteq V\times V$ represents the set of edges. Further, $w_{i,j}$ indicates the weight of the edge connecting vertex i and vertex j. The establishment rules of the topological graph $G=(V,E)$ were as follows:

a) The vertices set of the topological graph $V=\{1,2,\cdots,n\}$ is the set of intersection points in the circuit routing diagram. For Fig. 3, $n=12$.

b) The edges set of the topological graph $E\subseteq V\times V$ characterizes the connections among the intersection points in the circuit routing diagram.If there is a direct connection between intersection point i and intersection point j, then there is a weighted edge between the corresponding vertex i and vertex j. Otherwise, there is no weighted edge (or the edge has a weight of 0). As shown in Fig. 3, there is a direct connection between intersection point 1 and intersection point2, and thus, there is a weighted edge between the corresponding vertices 1 and 2. In contrast, there is no direct connection between intersection point 1 and intersection point3, and thus, there is no weighted edge between the corresponding vertices 1 and 3.

c) The weight of edge $w_{i,j}$ represents the number of vias on the direct connection between the intersection points. If there is no via on the direct connection between intersection point i and intersection point j, then the weight between the corresponding vertices i and j, $w_{i,j}=-1$. If there is one via on the direct connection between intersection point i and intersection point j, then $w_{i,j}=1$.

d) For a "T"-shaped circuit with a via in the middle, if the direct connection between intersection point i and intersection point j is on the same layer of the board, then the weight between the corresponding vertices $w_{i,j}=-1/2$. If the direct connection between intersection point i and intersection point j is on different layers of the board, then the weight between the corresponding vertices, $w_{i,j}=1/2$. In Fig. 3, as intersection points 5, 8, and 9 forma "T"-shaped

circuit with one via in the middle, the weights between the corresponding vertices $w_{5,8} = w_{5,9} = 1/2$, $w_{8,9} = -1/2$.

According to the above rules, the topological graph of the via optimization problem established from Fig. 3, $G = (V, E)$, is shown in Fig. 4.

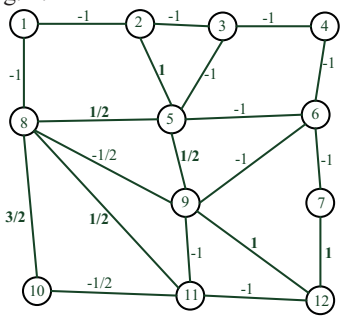

Fig. 4 Topological graph of the via optimization problem

B. Mathematical Model of Via Optimization Problem

As known by comparing Figs. 3 and 4, the negative weight between the vertices in the topological graph shown in Fig. 4 indicates that there is no via between the corresponding intersection points, and the positive weight between the vertices indicates that there are vias between the corresponding intersection points. The sum of the positive weights is equal to the number of vias in Fig. 3 (six). In contrast, without changing the topology shown in Fig. 4, the sum of the positive weights in the topological graph can be reduced with appropriate segmentation methods. Thus, the number of vias in the original circuit diagram can be optimized. Fig.5 shows the segmentation illustration of the via topology. Assume that the split line segments the topology into two parts, S and $V-S$, vertices $(1,2,\cdots,11) \in S$, $(12) \in V-S$,as shown in the left figure of Fig. 5.Then, the weight of the edge segmented by the split line is taken as the opposite number; that is, on the segmented topological graph, $w_{7,12} = w_{9,12} = -1$, as shown in the right figure of Fig. 5.

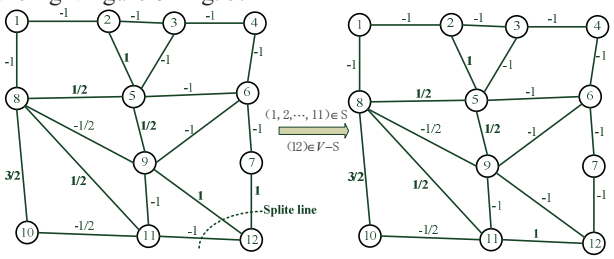

Fig. 5 Segmentation illustration of the via topology

The circuit routing diagram generated from the segmented topological graph, that is, the right figure of Fig. 5, is shown in Fig. 6.

An analysis of Figs. 5 and 6 revealed that the weight of the segmented edge was $Cut(S) = 1+1+(-1) = 1$. After the segmentation, the sum of the positive weights in the topological graph reduced from 6 to 5, and the number of

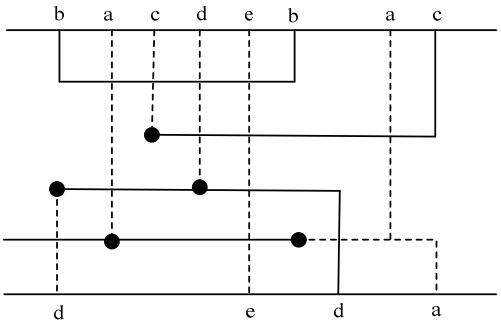

Fig. 6 Circuit routing diagram corresponding to the segmented topology

vias in the corresponding circuit routing diagram also reduced from 6 to 5.Therefore, for a given topology, a segmentation method to obtain the maximum segmented weights on the topological graph needs to be found, which results in the maximum reduction of the number of vias in the corresponding circuit diagram. Therefore, on the basis of the topological weight segmentation method, the solution of the via optimization problem is equivalent to the following:

$$\max \quad Cut(S) = \sum_{i<j} w_{i,j}(1 - x_i x_j)/2 \tag{1}$$

$$s.t. \quad x \in [-1,1]^n$$

where x is the segmentation vector, and

$$x_i = \begin{cases} 1 & i \in S \\ -1 & i \in V - S \end{cases}$$

III. Simulation Experiment and Analysis

The via optimization problem is a typical combinatorial optimization problem, and the most significant feature of the combinatorial optimization problem is that the candidate solution set explodes with an increase in the problem size. Therefore, the heuristic algorithm is mostly used for the combinatorial optimization problem. As mentioned above, to solve the via optimization problem, Hopfield neural network and GA were adopted in prior research[4] [5], and good results were obtained. However, as the Lyapunov function of the network is only reduced in a single direction, the Hopfield neural network makes it easy for the network to fall into the local extremum. GA has low efficiency because of the existence of a large number of individual crossovers and mutations. To overcome the shortcomings of these algorithms, in this study, we adopted EDA to solve the via optimization problem.

A. Basic flow of EDA

EDA is a new type of optimization algorithm emerging in the field of evolutionary computation, which combines GA and statistical learning. It establishes a probability model of an individual distribution in the solution space through a statistical learning method and then, randomly samples the probability model to generate the new group[7] [8]. This flow keeps repeating to achieve the evolution of the group. The basic flow is shown in Fig. 7.

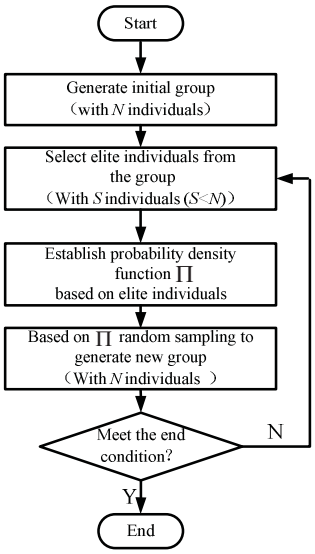

Fig. 7 Basic flow of EDA

Compared with GA, EDA does not have crossover operators or mutation operators and instead, uses the probabilistic model to learn and sample. In the evolution process, the whole group gets optimized, rather than the individuals. Thus, relatively high search efficiency is achieved. More details on EDA can be found in [9] [10].

B. Solution Steps of Via Optimization Problem

Combining the mathematical model of the via optimization problem with the flow of EDA, we designed the following steps for solving the via optimization problem on the basis of EDA:

(a) Generate the initial group P_0 randomly by following the uniform distribution (the segmentation vector has a probability of 50% to be valued as either 1 or −1.). The group size is N.

(b) Calculate the adaptive value of each individual, f_i, $i=1,2,\cdots,N$, in the group according to equation (1).

(c) Sort individuals according to the adaptive values f_i, and select S $(S<N)$ individuals with large adaptive values as the dominant groups P_k^S (k is the evolution generation).

(d) Establish the probability density function Π on the basis if the dominant group P_k^S, that is, the probability that the segmentation vector x_i takes the value of 1 in all the individuals of the dominant group P_k^S: $\Pi_i = p\left(x_i = 1 \mid P_k^S\right)$.

(e) Generate a new generation of group P_{k+1} by random sampling according to the probability density function Π, where the probability that the segmentation vector x_i takes the value of 1 is Π_i, and −1 is 1-Π_i.

(f) Determine whether the end condition is met. If so, end the program; otherwise, return to step (b).

In the group generated in this algorithm flow, all the individuals are valid solutions, and there is no invalid solution; that is, each individual $\mathrm{X}_j = (x_1, x_2, \cdots, x_i, \cdots, x_n)$, $x_i \in [-1,1]^n$ corresponds to a segmentation form of the topological graph and can be finally reverted to a feasible circuit routing diagram.

C. Simulation Experiment

On the basis of the algorithm flow described in Section B, the topological graph of the via optimization problem shown in Fig. 4 was solved and compared with GA.

The algorithm parameters were set as follows: group size N=200, evolution pool size S=100, evolution generation G=100, GA crossover probability p_c=0.9, and GA mutation probability p_m=0.05. Meanwhile, to accelerate the convergence, both algorithms adopted the elite retention strategy; that is, the optimal individuals in the parent generation were retained in the descendant group during the evolution process.

The experimental results demonstrated that both the algorithms could find the optimal weight segmentation of the topological graph shown in Fig. 4, i.e.:

$MaxCut1$：（1, 2, 3, 4, 5, 6, 7, 8, 9）$\in S$, （10, 11, 12）$\in V-S$

$MaxCut2$：（3, 4, 5, 6, 7, 9, 10, 11）$\in S$, （1, 2, 8, 12）$\in V-S$

The segmented weight obtained from both segmentation results was as follows:

$$Cut(S)=3$$

The circuit routing diagrams corresponding to $MaxCut1$ and $MaxCut2$ are shown in Figs. 8 and 9, respectively.

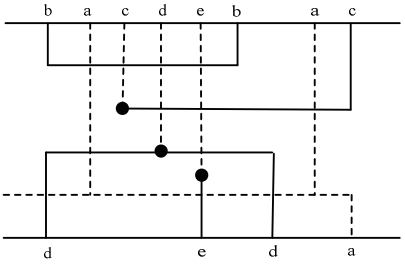

Fig. 8 Circuit routing diagram corresponding to $MaxCut1$

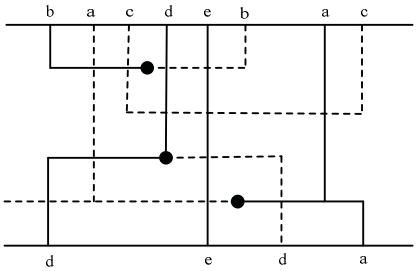

Fig. 9 Circuit routing diagram corresponding to $MaxCut2$

Compared with the circuit routing diagram shown in Fig. 2, with the number of vias was 6, the number of vias in the circuit routing diagram shown in Figs. 8 and 9 was 3; that is, the number of vias was reduced by 3. The reduction of vias was equal to the segmented weight $Cut(S)=3$ obtained from

the two segmentation results, $MaxCut1$ and $MaxCut2$. The effectiveness of the algorithm was thus verified.

In order to compare the performance of EDA and GA on the via optimization problem, the variations of the averaging group adaptive values of the two algorithms during the evolution process were analyzed experimentally, under the premise that both the algorithms could find the optimal value. At the same time, to improve the reliability of the experimental results, the two algorithms were repeatedly run for 20 times under the same conditions and then averaged. The experimental results obtained are shown in Fig. 10.

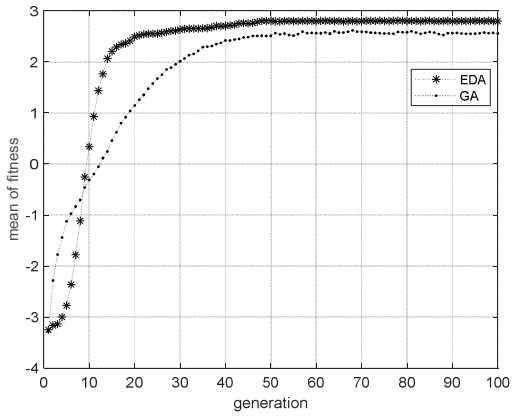

Fig. 10 Variation of average group adaptive values of the two algorithms

Fig. 10 shows that under the same conditions of group size, evolution generation, evolution strategy, etc., EDA converged faster than GA, and the overall adaptive value was better. Furthermore, for the simulations on the same computer, it took EDA around 0.5 s to repeat solving the via optimization problem shown in Fig. 4 for 20 times, while GA required around 2.0 s. This demonstrated that EDA had better operation efficiency than GA.

IV. CONCLUSION

In this paper, we proposed a new method for solving the via optimization problem in integrated circuit routing. First, the circuit routing diagram was converted to an undirected weighted topological graph. Then, the mathematical model of the via optimization problem was established on the basis of the topological weight segmentation method. Finally, the via optimization problem was solved using EDA, and a comparative experiment was conducted with GA.

Compared with the existing methods, the method proposed in this paper was more intuitive. In the constructed topological model, the sum of all the positive weights was the number of vias in the circuit. The number of vias could be reduced by segmenting the topological graph to reduce the sum of positive weights. The sum of the weights of the segmented edge was the number of reduced vias. The final experimental results also demonstrated the effectiveness of the proposed method. Meanwhile, in the algorithm flow designed in this study, all the individuals were valid solutions, and there was no invalid solution in the group, which improved the efficiency of the algorithm. Finally, EDA-based solution of the via optimization problem had faster convergence and better effectiveness than GA-based one.

ACKNOWLEDGMENT

This research was funded by the national natural science foundation of China (grant number: 61401470), and by the foundation of Shaanxi Key Laboratory of Integrated and Intelligent Navigation (grant number: SKLIIN-20180206).

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