Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_



Section: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_



Net-ID: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**CS/ECE 252 Introduction to Computer Engineering**

Spring 2018

Instructor: Adil Ibrahim

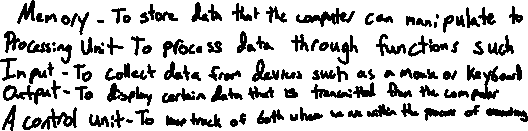
**Homework 4**

**Deadline: March 2nd 2018**

For each question below you need to show the complete working to receive full points. Please utilize the space provided under each question. Please upload a PDF version on canvas.

**Problem 1 (5 pts)**

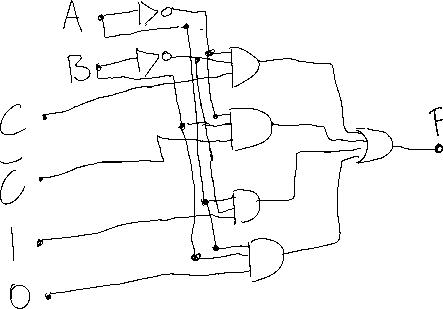
Briefly describe the function of each part of Von Neumann Model



**Problem 2 (8 pts)**

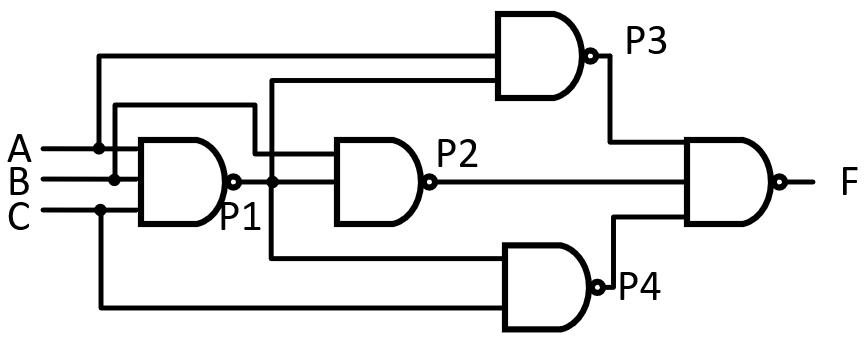
Implement the function using a 4:1 mux. (The input signal is A,B,C, 1/0 is also available)

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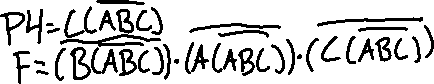


**Problem 3 (12 pts)**

Consider the logic circuit in figure below:



1) Express the P1, P2, P3, P4, F in terms of A B, and C



2) Finish the truth table

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | F |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

3) Analyse the function of the circuit



**Problem 4 (12 pts)**

Using NAND gate to design a combinational logical circuit. There are 3 binary inputs (A,B,C) and one output (F). When there are odd 1s in the inputs, the output is 1, otherwise 0. (You need to show your steps)

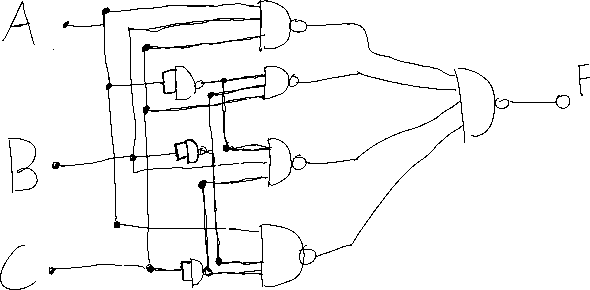
1) Complete the truth table of the circuit

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | F |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
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|  |  |  |  |

2) Express F in terms of A B, and C



3) Draw this logical circuit using NAND gates



**Problem 5: (12 pts)**

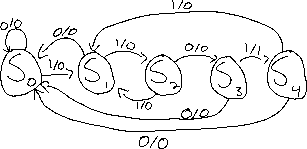
Consider a finite state machine (FSM) that recognizes the pattern "1101". The input to the FSM is a sequence of binary bits, one after the other. When the FSM receives 1101 as inputs in successive bits, it should output 1. Otherwise, the output should be 0.

For example

Input sequence: 11011011001101

FSM output: 00010010000001

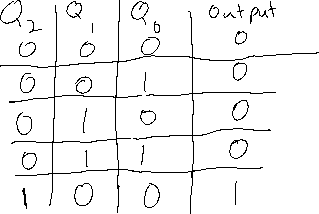
1) Draw the state diagram for this FSM and describe what each state represents



2) How many bits are required to represent all the states?



3) Draw the output truth table for this FSM (e.g. if you need 2 bits (Q1, Q0) to represent all the states, then the truth table has 3 columns (Q1, Q0|output))



4) Draw the next state logic truth table for this FSM (e.g. if you need 2 bits (Q1, Q0) to represent all the states, then the truth table has 5 columns (input, Q1, Q0|Q1, Q0))

