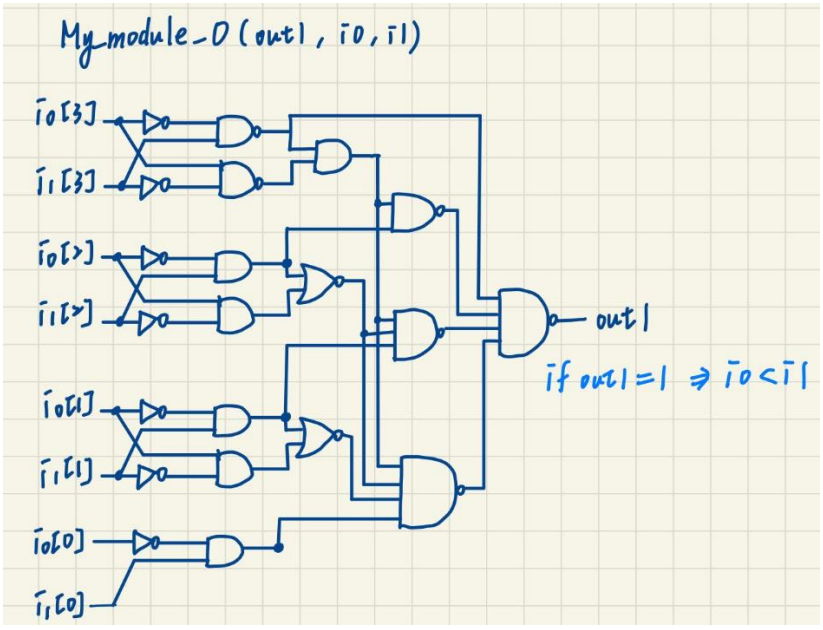
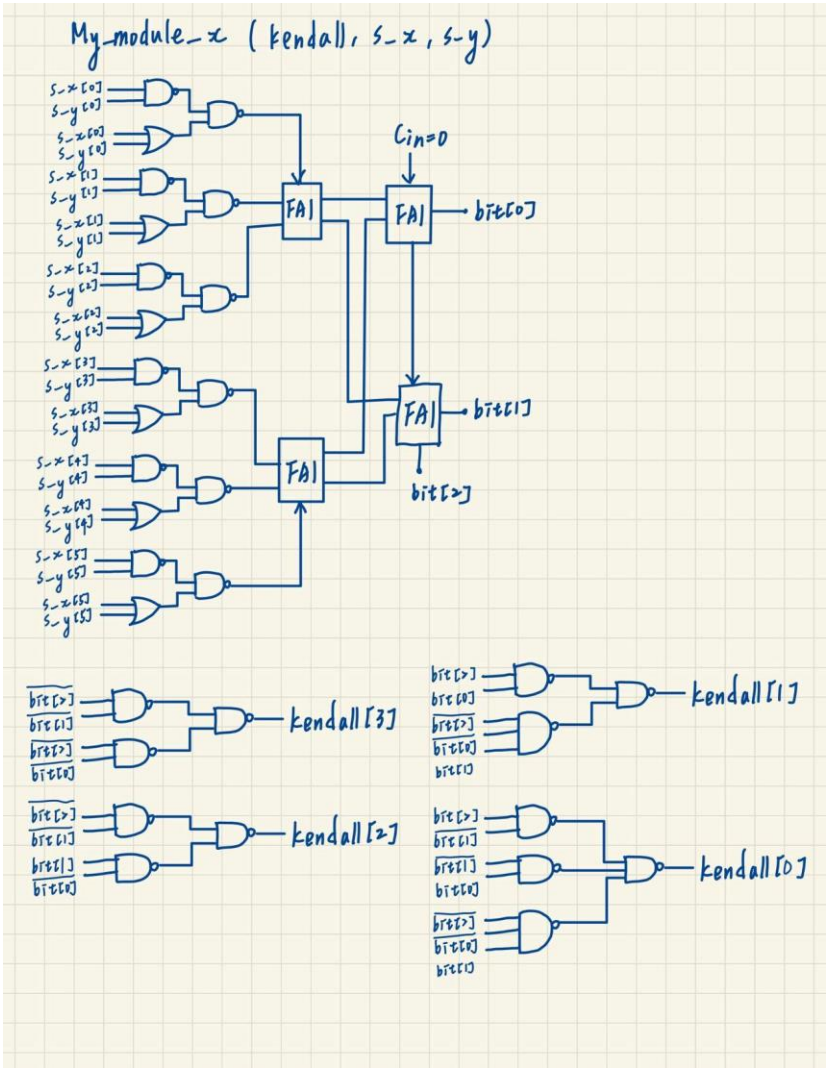
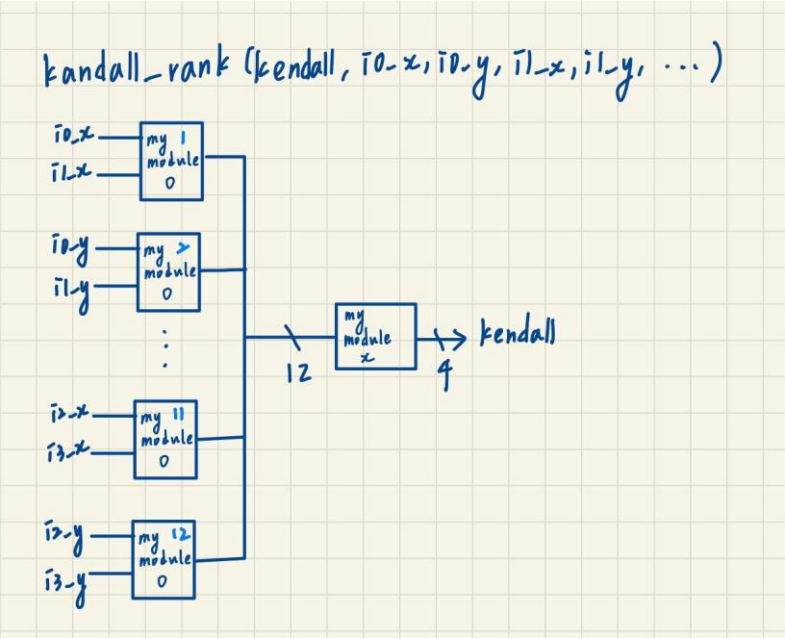
IC design hw3 report

1. Circuit diagram







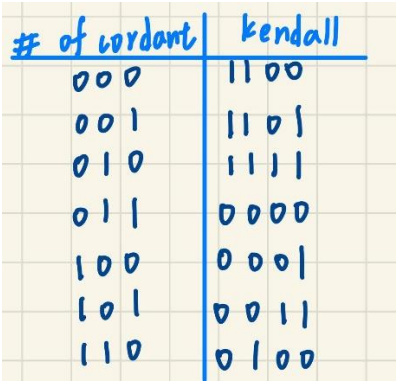
2. Discussion

Firstly, My_module_0 use four-bit comparator to get whether input A is smaller than input B. The initial four-bit comparator use OR4 as output, which will induce large delay. Therefor I change OR4 into ND4, and also change some of the AN gate into ND gate. In addition, the initial comparator has three output, however, we don't need to consider that many possible outputs, so I only preserve the output that represent A<B (if out1=1, A<B. else, A>B).

Secondly, execute My_module_0 twelves times to get the relation between each pair of input.

Then, My_module_x receives the twelves outputs from above. My_module_x first use six EN gates to check whether the pair is concordant. I replace EN with two ND2 and one OR2 since EN has large propagation delay. Now we have six output need summed up to get the number of total concordant pairs. I use two FA1 to sum up three inputs respectively. Then use two FA1 construct a two-bit ripple carry adder to sum up the two summation of three inputs.

With the total number of concordant pairs, we can generate the circuit of divide formula by truth table shown as below.



# of concordant	kendall
000	1100
001	1101
010	1111
011	0000
100	0001
101	0011
110	0100