IC design hw1

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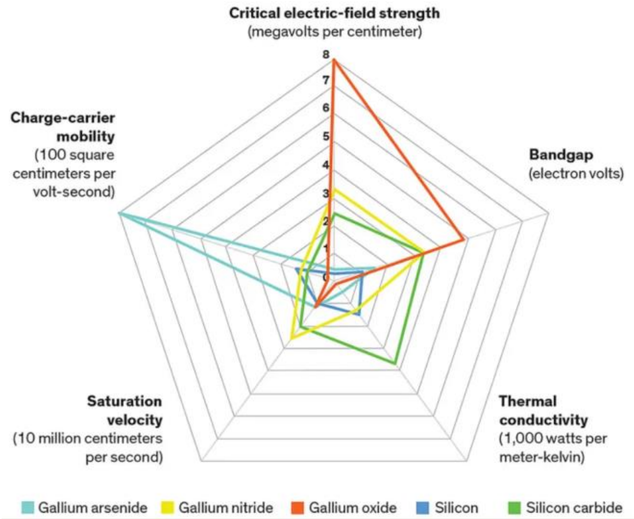
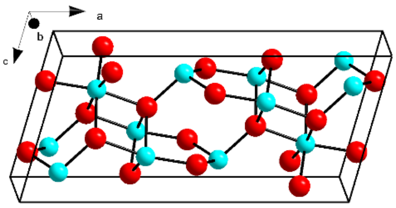
1. Gallium trioxide is an inorganic compound with the formula Ga2O3. Ga2O3 is an intermediate in the purification of gallium, which is consumed almost exclusively as gallium arsenide. β-Ga2O3, with a melting point of 1900 ℃, is the most stable crystalline modification. The oxide ions are in a distorted cubic closest packing arrangement, and the gallium (III) ions occupy distorted tetrahedral and octahedral sites, with Ga-O bond distances of 1.83 and 2.00 Å respectively.

Gallium trioxide is amphoteric. In Ga2O3, you can dope the crystal with silicon in the same way to add electrons. Gallium oxide's amenability to dopants added by a standard process called ion-implantation and during epitaxial growth—depositing additional crystal—allows us to borrow a wide range of established commercial lithography and processing techniques.

It is superior to other materials with larger bandgaps that still conduct electricity. At nearly 5 electron volts, this crystal's bandgap has GaN (3.4 eV) beat by a mile and silicon (1.1 eV) by a marathon. Diamond and aluminum nitride have larger bandgaps, but they don't have what Ga2O3 has—a fortunate set of characteristics that lend themselves to making inexpensive but very powerful devices. It is further reduced for related nanostructures which are usually used in electronic devices.

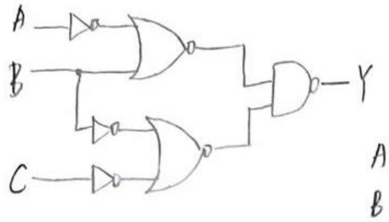




Gallium(III) oxide has been studied in the use of lasers, phosphors, and luminescent materials. It has also been used as an insulating barrier in tight junctions. Monoclinic β-Ga2O3 is used in gas sensors and luminescent phosphors and can be applied to dielectric coatings for solar cells. This stable oxide has also shown potential for deep-ultraviolet transparent conductive oxides, and transistor applications. Gallium(III) oxide could make RF amplifiers more powerful and efficient and could shrink power electronics even more, dropping precious kilograms and cubic centimeters of electronics from airplanes and automobiles.

2.

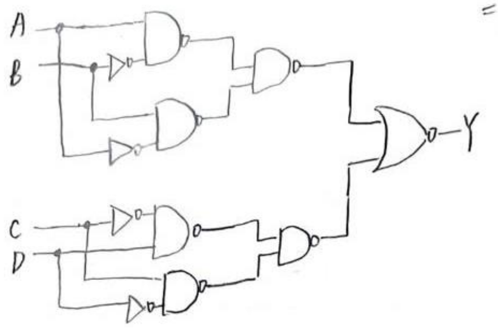
(a) $Y=\overline{(A\cdot\bar{B})}+\overline{(\bar{B}\cdot C)}$



(b) $Y=\overline{(A\oplus B)}\cdot\overline{(C\oplus D)}$

$=\overline{(A\bar{B}+\bar{A}B)}\cdot\overline{(C\bar{D}+\bar{C}D)}$

$=((\overline{\bar{A}+B})+(\overline{A+\bar{B}}))((\overline{\bar{C}+D})+(\overline{C+\bar{D}}))$



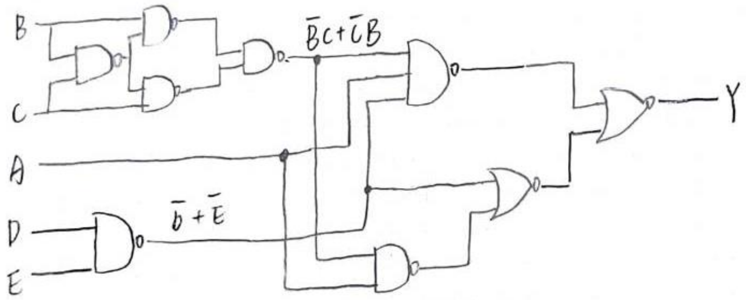
(c) $Y=\overline{(A\cdot(B\oplus C))\oplus(DE))}$

$=\overline{A(B\oplus C)\,\overline{DE}+\overline{A(B\oplus C)}\,DE}$

$=\overline{(A(B\oplus C)\,\overline{DE})}\cdot\overline{(\overline{A(B\oplus C)}\,DE)}$

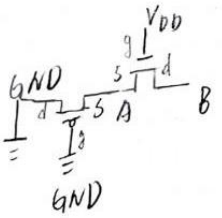
$=\overline{(A(B\oplus C)(\bar{D}+\bar{E})}\,\overline{(\overline{A(B\oplus C)}\,(\bar{D}+\bar{E}))}$

(c)



3、

(a)

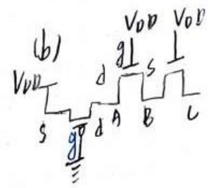


$V_{sg}=V_A-GND=V_{tp}$

$\therefore V_A=|V_{tp}|+GND$

$V_B=|V_{tp}|+GND$

(b)

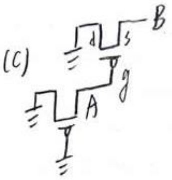


$V_B=V_{DD}-V_{tn}$

$V_C=V_{DD}-V_{tn}$

$V_A=V_{DD}$

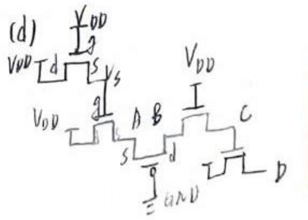
(c)



$V_A=|V_{tp}|+GND$

$V_B=>|V_{tp}|+GND$

(d)



$V_S=V_{DD}-V_{tn}$

$V_S-V_A=V_{tn}$

$V_A=V_{DD}->V_{tn}$

$V_B=V_{DD}->V_{tn}$

$V_C=V_{DD}-2V_{tn}$

$V_D=V_{DD}-3V_{tn}$

4.

(a)

a	b	c	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

b = 0 : pass a

b = 1 : pass c

2-to-1 multiplexer

$Y = \bar{b} \cdot a + bc$

(b) no,

when b = 1, the below CMOS on,

(and both PMOS and NMOS on),

so can pass both strong 1 and strong 0.

when b = 0, the upper CMOS on,

can pass both strong 1 and strong 0.

5. linear region

$I_{ds} = \beta(V_{gs} - V_t - \frac{1}{2}V_{ds})V_{ds}$

$= (-\frac{1}{2}V_{ds}^2 - V_{ds}V_t + V_{ds}V_{gs})\beta$

slope = dI_{ds}/dV_{ds}

$= (-V_{ds} - V_t + V_{gs})\beta$

when $V_{gs} = 1$, $V_{ds} = 0$, slope = 336

$$\begin{cases} \beta(-V_t + 1) = 336 \\ \beta(-V_t + 0.8) = 252 \\ \beta(-V_t + 0.6) = 168 \end{cases}$$

$$\begin{cases} -V_t + 1 = \frac{4}{3}(-V_t + 0.8) \Rightarrow V_t = 0.2 \\ -V_t + 0.8 = \frac{3}{2}(-V_t + 0.6) \Rightarrow V_t = 0.2 \end{cases}$$

$V_t + 3 = 3.2 \quad V_t = 0.2$

$\therefore V_t = 0.20V$

$Y = \overline{(\bar{B}+\bar{C})(\bar{B}+\bar{A})(\bar{C}+\bar{A})}$

6.

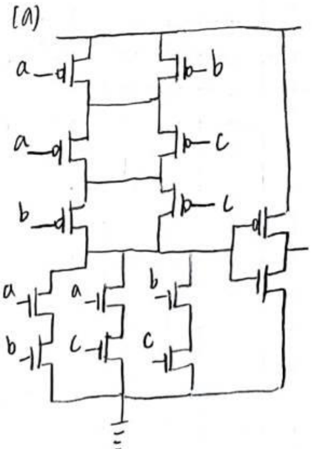
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$Y = BC + AC + AB + ABC$

$= BC + AC + AB$

$\bar{Y} = \overline{(BC + AC + AB)} \quad Y = \bar{\bar{Y}}$

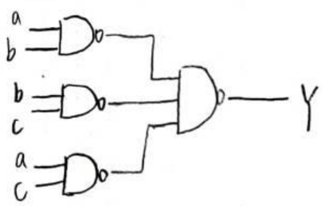
(a)



14 transistors

$\bar{Y} = (\bar{B}+\bar{C})(\bar{A}+\bar{C})(\bar{A}+\bar{B})$

(b)



3 Nand × 4 + 1 Nand × 6

= 18 transistors,

more than 14

transistors needed in (a)