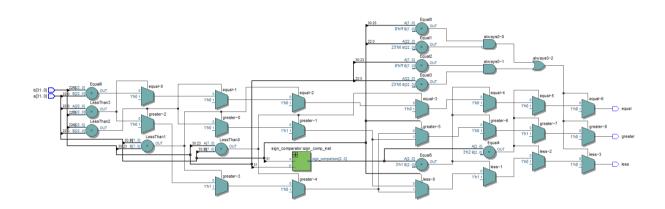
## DISEÑO EN VERILOG DE UN COMPARADOR DE NÚMEROS CON PUNTO FLOTANTE

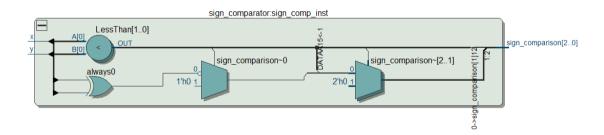
## Diagrama de bloques:

Circuito general del comparador en coma flotante:

Este circuito compara el signo de dos números en el estándar IEEE 754. Primero se analiza si el circuito no corresponde a un NaN o número no existente. Los NaN no representan números en este estándar, solo sirven para representar errores u otros, por lo que no cuentan con un valor numérico para la evaluación. Luego se compara el bit más significativo para determinar si los números son positivos o negativos, posteriormente se analiza el exponente y la fracción o también llamada matinsa. Finalmente, se determina si el primer número es mayor, menor o igual al segundo número ingresado. Si la trama de bits no es un número o corresponde a un NaN se obtiene el valor de cero para todas las salidas.



## Circuito comparador de signo:



### RTL del circuito:

```
parameter wIDTH = 32 )(
input wire [WIDTH - 1:0]a,b,
output reg greater, less, equal
);
        1456789011233456678990112333333333333344123445678990112222222222222223333333333344123445678990112334566789971
                                                             wire sign_a, sign_b;
wire [WIDTH - 2: FRACTION_WIDTH + 1] exponent_a, exponent_b;
wire [FRACTION_WIDTH: 0] fraction_a, fraction_b;
                                                           assign sign_a = a[WIDTH -1];
assign sign_b = b[WIDTH -1];
assign exponent_a = a[WIDTH -2:FRACTION_WIDTH + 1];
assign exponent_b = b[WIDTH -2:FRACTION_WIDTH + 1];
assign exponent_b = b[WIDTH -2:FRACTION_WIDTH + 1];
assign fraction_a = a[FRACTION_WIDTH:0];
assign fraction_b = b[FRACTION_WIDTH:0];
                                                     wire [2:0] sign_comparison;
                                                Esign_comparator sign_comp_inst (
    .x(sign_a),
    .y(sign_b),
    .sign_comparison(sign_comparison)
);
                                              Balways@(*) begin
                                                                                  if (((exponent_a == 8'hFF) && (fraction_a != ZERO_FRACTION)) || ((exponent_b == 8'hFF) && (fraction_b == ZERO_FRACTION))) begin |/If a or b is a NAN number greater = 0; | less = 0; | equal = 0; equal = 0; end else begin | or b is a NAN number greater = 0; | else begin | or b is a NAN number greater = 0; | else begin | or b is a NAN number | o
                                                                                                            equal = 0;
i else begin
if (sign_comparison == 3'b010) begin
//starting to compare sign
greater = 1;
less = 0;
equal = 0;
end else if (sign_comparison == 3'b001) begin
greater = 0;
less = 1;
equal = 0;
end else begin
if (sign_a = 0) begin
if (sign_a = 0) begin
if (exponent_a > exponent_b) begin
greater = 0;
equal = 0;
end else begin
if (exponent_a > exponent_b) begin
greater = 1;
equal = 0;
end else if (exponent_a < exponent_b) begin
greater = 0;
                                                                                                                                                                         equal = 0;

nd else begin

//Equal sgn 0, equal exponent, starting to compare fraction if (real sgn 0, equal exponent, starting to compare fraction if (real section if (real section is equal edge);

equal = 0;

end else if (fraction < fraction b) begin

greater = 0;

less = 1;

end disc if (fraction = = fraction b) begin

greater = 0;

less = 0;

equal = 1;

end else begin

greater = 0;

less = 0;

end else begin

greater = 0;

less = 0;

end

end
    end
d else begin

//cqual sign 1, starting to compare exponent
if (exponent_a > exponent_b) begin
    greater = 0;
    less = 1;
    equal = 0;
    end else if (exponent_a < exponent_b) begin
    greater = 1;
    less = 0;
    end else if (exponent_a < exponent_b) begin
    greater = 1;
    less = 0;
    end else begin
    //cqual sign 0, equal exponent, starting to compare fraction
    if (fraction_a > fraction_b) begin
    if (fraction_a > fraction_b) begin
    greater = 0;
    less = 1;
    equal = 0;
    end else if (fraction_a < fraction_b) begin
    greater = 0;
    equal = 0;
    end else if (fraction_a == fraction_b) begin
    greater = 0;
    less = 0;
    equal = 0;
    end else if (fraction_a == fraction_b) begin
    greater = 0;
    less = 0;
    equal = 0;

                                                end
end
endmodule
Bmodule sign_comparator(
   input wire x,y,
   output reg [2:0] sign_comparison);
                                              Balways@(*) begin

|//1 is negative sign, 0 is positive sign in IEEE 754

| if (x < y) begin

| sign_comparison = 3'b010;

| end else if (x > y) begin

| sign_comparison = 3'b011;

| end else if (x == y) begin

| sign_comparison = 3'b100;

| end else begin

| sign_comparison = 3'b100;

| end else begin

| sign_comparison = 3'b000;

| end end
```

#### Simulación del circuito:



```
# run 200 ns
# Starting testbench
Running testbench
Comparing 0.15625 with 0.15624
Comparing 2.25 with 2.14748365
TEST PASSED
At time 20 ns a = 010000000001000000000000000000 b = 010000000001011111000001011111 result =010
Comparing -3.14 with -2
Comparing 4 with 2.25 TEST PASSED
Comparing 2.25 with -3.14 TEST PASSED
At time 50 ns a = 01000000000100000000000000000 b = 1100000010010111010111000100 result =010
Comparing 2.25 with 2.5 TEST PASSED
Comparing 8235 with 422
TEST PASSED
Comparing -742 with 754 TEST PASSED
Comparing 17.17 with 17.17 TEST PASSED
At time 90 ns a = 010000011000100101110000101000 b = 010000011000100101110000101000 result =100
Comparing -1 with 1 TEST PASSED
Comparing -300 with -400
Comparing a NaN values TEST PASSED
TEST COMPLETED
```

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Material del curso Verilog – Módulo 1- Maelpro.