Q1)

1)

The motivation of memory hierarchy in modern computers is to optimize memory access time and reduce costs. Faster memory technologies, such as registers and cache, are expensive and have limited capacity, while slower memory technologies, such as hard disk drives, are less expensive and have larger capacity. By arranging memory technologies in a hierarchy, modern computers can achieve both fast access times and large capacities at a reasonable cost.

2)Registers> ON-Chip Cache> Second Level Cache> Main Memory> Secondary Storage

3)

(a) Speed: SRAM is faster than DRAM

(b) Principle: SRAM can retain the state as long as power is applied, while DRAM stores data as the electric charge on a capacitor and must be refreshed.

(c) Cost: SRAM (6 transistors) is more expensive than DRAM (1 transistor)

(d) Usage: SRAM for cache, DRAM for main memory.

Q2)

1)64K/32 = 64X1024/32 = 2048 Blocks

2)

Tag= 32-11-5 = 16 bits

Block= 2048= 2^11 = 11 bits

Byte offset= 32 = 2^5 = 5 bits

3)

Total bits per cache block = 1+ 16 +256=273 bits

Total bits = 273 × 2 ^11 bits

4)

Tag= 32-10-5 = 17 bits

Block= 2048/2=1024= 2^10 = 10 bits

Byte offset= 32 = 2^5 = 5 bits

Q3)

A0= 10100000, F1= 11110001, FF= 11111111, 35= 00110101, C8= 11001000, 89= 10001001,

FE= 11111110, 88= 10001000, A1= 10100001, A2= 10100010, A3= 10100011, A9= 10101001

99= 10011001, 80= 10000000, 83= 10000011

1)

Set 00:

|  |  |  |
| --- | --- | --- |
| A0 | A1 | 3 |
| A9 |  | 2 |
| 99 |  | 1 |
| 80 |  | 0 |

Set 01:

|  |  |  |
| --- | --- | --- |
| A2 | A3 | 1 |
| 83 |  | 0 |
|  |  |  |
|  |  |  |

Set 10:

|  |  |  |
| --- | --- | --- |
| 35 |  | 0 |
|  |  |  |
|  |  |  |
|  |  |  |

Set 11:

|  |  |  |
| --- | --- | --- |
| FF | FE | 0 |
|  |  |  |
|  |  |  |
|  |  |  |

2)

A0= 10100000, F1= 11110001, FF= 11111111, 35= 00110101, C8= 11001000, 89= 10001001,

FE= 11111110, 88= 10001000, A1= 10100001, A2= 10100010, A3= 10100011, A9= 10101001

99= 10011001, 80= 10000000, 83= 10000011

00:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A0 | A1 | A2 | A3 | 0 |
| ~~F1~~ 80 |  |  | 83 | 1 |

01:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 |  |  |  | 0 |
|  |  |  |  |  |

10:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ~~C8~~ A9 |  |  |  | 0 |
| ~~89~~ 99 | ~~88~~ |  |  | 1 |

11:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FF | FE |  |  | 0 |
|  |  |  |  |  |

Q4)

Miss penalty = 50ns+200ns+50ns =300ns

Hit rate: h=(2000-50)/2000 =0.974

Average memory access time = 0.974x50 +(1-0.974)x300ns = 56.5ns

Access efficiency= 50/ 56.5 =0.89

Q5)

16KB page size = 2^14 = 14 bit

32 – 14 =18bit = 2^18 pages

Q6)

1a) Virtual pages numbers = 2 32/2 16 = 216.

b. The number of pages × address bit= ,2 16 ∗ 4 =256K bytes

2) 2^(32-4)= 268435456 = 256MB

3)

The tag bit of page index: 16 bits, the memory offset 16 bit. While the tag bit of cache is 64KB=2^16, so it is possible to make a 64KB direct-mapped cache.