1. Open file gscl45nm.lib using a text editor and find cell MUX2X1.

(a) What are the input pins of the cell?

A,B,S

(b) What is the output pin of the cell?

Y

(c) What is the Boolean function of the cell?

(!((S A) + (!S B)))

(d) What is the cell leakage power?

18.5503

2. Open file gscl45nm.lef using a text editor.

(a) What are the width and height of cell NAND2X1 in micron?

0.76 BY 2.47

(b) What are the width and height of cell MUX2X1 in micron?

1.52 BY 2.47

(c) What are the routing directions of layer metal1 and metal2?

Metal1 : HORIZONTAL

Metal2: VERTICAL

1. Follow the above instructions to do the synthesis. What is the slack and total cell area of the design?

Slack:-0.07 cell area:338.834592

2. To minimize area, set the max area as 300 and replace compile with compile -area effort high. What is the total cell area now?

Cell area: 301.759893

3. Try different clock periods. What is the shortest clock period without a negative slack? What frequency (GHz) does the clock period correspond to? What is the cell area of this design?

0.21 nanosecond. Frequency is 4.76Ghz , cell area is 297.066893.

4. Can we achieve smaller area in 3 by setting set max area as 200, 100, or even 0? What does the command set max area 0 mean? (see User Guide) 5. Attach the .tcl you used to achieve the clock period in 3.

Set to 200: 297.066893

Set to 100: 297.066893

Set to 0: 297.066893

No, it cant.

The command set\_max\_area 0 is telling the synthesis tool to minimize the area as much as possible without regard for other constraints like performance or power.