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Dear Tenstorrent Team,

I want to grow at the boundary where models, compilers, runtime, and custom RISC-V hardware meet—exactly what your rotational role offers. I am Toronto-based and fully available on-site.

Beyond RTL, I bring a balanced software + ML foundation: C/C++ performance work (pathfinding engine with multiple algorithms and cache-aware data structures), current Operating Systems & Data Structures coursework (memory layout, synchronization, asymptotic trade-offs), and applied ML projects (CRNN handwriting recognition, vector-search powered apps). This helps me reason how batching, locality, and algorithm structure translate into latency, bandwidth pressure, or accelerator utilization.

In hardware-oriented courses I self-taught structured testbenches, parameterized stimulus, and scripted ModelSim runs instead of relying only on manual waveform poking—now extending that discipline toward SystemVerilog assertions and UVM concepts. My approach is: prototype in software, measure, then define clean RTL boundaries.

Day one I can implement readable Verilog control/datapath blocks, write Python/C microbenchmarks (e.g. vector add, small GEMV) to expose bottlenecks, script regression + log diff flows, and add lightweight firmware hooks (counters / diagnostic reads) for faster bring-up. In parallel I am ramping on synthesis + timing (slack, critical path intuition) and simple roofline-style operator profiling.

I aim to contribute to concise RTL, reproducible verification scaffolding, and data-backed architectural exploration while accelerating my formal verification depth.

Thank you for your consideration.

Sincerely,

Yongkang Cheng