

Yongkang Cheng

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EDUCATION

University of Toronto, Toronto, ON

Sep 2023 – May 2028 (expected)

BASc Computer Engineering + PEY Co-op, cGPA: 3.87/4.0 (88.6%)

Relevant: Digital Systems, Computer Organization, (In progress) Digital Electronics, Operating Systems

EXPERIENCES

Research Assistant, Spiking Neural Network FPGA Deployment

Sep 2025 - Present

Research Intern, X-Lab, University of Toronto

Toronto, ON

- Took over Verilog implementation of an SNN from a teammate; verified modules with ModelSim testbenches.
- Prototyping FPGA deployment flow with Vivado, validated initial design on Nexys board, preparing SNN integration.

Research Assistant, Ultra-Wideband Receiver Design

May 2025 - Jul 2025

Research Intern, X-Lab, University of Toronto

Toronto, ON

- Collaborated in a 2-person team, verified a hybrid 4-PPM + 8-PSK TX chip pre-tapeout; built Python/Simulink pipelines for 2 ns symbol sync and carrier recovery under discontinuous 4.6 GHz.
 - Built pulse-position detection and K-means phase calibration for constellation stabilization and PPM demodulation.
 - Achieved error-free demodulation across 2,500 symbols under ≥ 16 dB SNR (AWGN) and $\pi/16$ phase jitter.
 - Presented at Undergraduate Engineering Research Day with a poster and an interactive demo, engaged 50+ attendees.
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PROJECTS

FPGA Polyphonic Synthesizer

Mar 2025

- Developed a 20-voice soft-core audio engine (C on Nios-V) streaming 8 kHz Q15 samples via audio FIFO; optimized kernels by replacing floating-point with fixed-point arithmetic.
- Designed and integrated interrupt service routines for PS/2 input and a double-buffered 320×240 VGA display pipeline, ensuring synchronized graphics rendering with deterministic latency.
- Developed simple graphics primitives and interrupt-driven APIs for responsive, low-latency user interaction.

Verilog Pac-Man Game (DE1-SoC)

Nov 2024

- Created a Pac-Man-style FPGA game using Verilog on DE1-SoC supporting PS/2 keyboard input and VGA output.
- Debugged signal sync and FSM logic issues using ModelSim, automated the debug process with customized testbenches and .do files, ensured smooth and bug-free gameplay.
- Prototyped the game using Pygame for agile development, automated image conversion using Python + OpenCV.

City Mapify (C++ Performance Engine)

Jan 2025 – Apr 2025

- Implemented QuadTree spatial index and pathfinding (Dijkstra/A*/metaheuristics) with cache-friendly adjacency layout enabling 60 FPS rendering on 2GB map data.
 - Designed modular pathfinding kernel with templated weight/heuristic for fast extensibility.
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SKILLS

- **Programming:** C/C++, Python, Verilog, Assembly (RISC-V), MATLAB/Simulink, JavaScript, Java
 - **Systems:** Linux system programming, multithreading, process control, memory management, device drivers
 - **EDA Tools:** Quartus, Vivado, ModelSim, LTSpice, Ansys HFSS, Altium Designer, Rhinoceros, Blender, 3Ds Max
 - **Tools & Libraries:** I2C, SPI, OpenCV, PyTorch, Pandas, FastAPI, Nginx, Git, Linux
 - **Hardware:** Raspberry Pi (5, zero, pico), STM32, Soldering, 3D Printing, Oscilloscope, Logic Analyzer, Multimeter
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AWARDS

• **University of Toronto Excellence Award (UTEA)**

Apr 2025

\$7,500 scholarship for 6 students among 2nd to 4th ECE for research potential.

• **ECE Awards**

Sep 2024

Awarded to top 30 students in the first-year ECE program out of 300+ students.