Yongkang Cheng

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EDUCATION

University of Toronto (St. George), Toronto, ON Sep 2023 – May 2028 (expected)
BASc in Computer Engineering + PEY Co-op, cGPA: 3.87/4.0 (88.6%)
Relevant Coursework: Digital Electronics (in progress), Operating Systems (in progress), Digital Systems, Computer Organization

TECHNICAL SKILLS

- **Programming:** Python, C/C++, Verilog, Assembly (RISC-V), MATLAB/Simulink
- **EDA Tools:** Quartus, ModelSim, LTSpice, Ansys HFSS, Altium Designer, SUE, MAX
- **Hardware Tools:** PCB Design, Oscilloscope, Soldering, 3D Printing, Vector Network Analyzer
- **3D Modeling:** Rhinoceros, Blender, 3Ds Max

EXPERIENCE

Research Assistant, Wireless Power Transfer Coil Design Jul 2025 - Aug 2025
Research Intern, X-Lab, University of Toronto *Toronto, ON*

- Designed a resonant 13.56 MHz wireless power transfer coil pair enabling reliable power delivery to a brain-computer interface implant across a 20 mm separation.
- Ran HFSS sweeps (turns, trace width, TX diameter) to optimize coupling ($k > 0.01$) and quality factor ($Q > 28$).
- Performed electromagnetic field simulations and resonant frequency tuning to improve link efficiency under load.
- Designed PCB layouts incorporating capacitive tuning networks; fabricated and tested 3 TX and 11 RX prototype boards to validate coupling efficiency.

Research Assistant, Ultra-Wideband Receiver Design May 2025 - Jul 2025
Research Intern, X-Lab, University of Toronto *Toronto, ON*

- Verified a hybrid 2-PPM + 8-PSK TX chip pre-tapeout; built Python/Simulink pipelines for 2 ns symbol sync and carrier recovery under discontinuous 4 GHz.
- Built pulse-position detection and K-means timing/phase calibration for constellation stabilization and PPM demodulation.
- Achieved zero-BER demodulation across 2,500 symbols under $\geq 13\,\text{dB}$ SNR (AWGN) and $\pi/16$ phase jitter.
- Presented at Undergraduate Engineering Research Day with a poster and an interactive demo site.

PROJECTS

FPGA Polyphonic Synthesizer Mar 2025

- Built (with one collaborator) a 20-voice synthesizer in C on a Nios-V (RISC-V) soft-core on DE1-SoC; streamed 8 kHz Q15 audio via on-chip Audio FIFO.
- Replaced floats with 32-bit phase accumulators and fixed-point DSP; realized real-time mixing and ADSR envelope.
- Implemented PS/2 interrupt-driven input with a double-buffered 320×240 VGA UI.

Verilog Pac-Man Game Nov 2024

- Built (with one collaborator) an FPGA Pac-Man in Verilog with PS/2 input and VGA output on DE1-SoC.
- Implemented hierarchical FSM game logic (movement, ghost AI, collision detection) and a custom VGA controller with cycle-accurate 320×240 scan timing.
- Resolved signal synchronization and state logic issues using ModelSim; automated asset conversion via OpenCV.

AWARDS

- **University of Toronto Excellence Award (UTEA)** Apr 2025
  $7,500 scholarship for 6 students among 2nd to 4th ECE for research potential.
- **ECE Awards** Sep 2024
  Awarded to top 30 students in the first-year ECE program out of 300+ students.