Yongkang Cheng

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EDUCATION

University of Toronto (St. George Campus), Toronto, ON Sep 2023 - May 2028 (expected)
Bachelor of Applied Science in Computer Engineering + PEY Co-op (cGPA: 3.87/4.0)
Relevant Courses: Digital Logic Design, Circuit Analysis, Signal Processing, Computer Architecture

TECHNICAL SKILLS

- **Hardware Design:** Verilog, VHDL, SystemVerilog, Digital Circuit Design, ASIC Design Flow
- **EDA Tools:** Quartus, ModelSim, LTSpice, HFSS, Cadence, Synopsys (familiar)
- **FPGA & Processors:** Intel DE1-SoC, Nios-V, Altera/Intel FPGAs, ARM Cortex
- **Programming:** C/C++, Python, Assembly (RISC-V), MATLAB/Simulink
- **Hardware Tools:** Oscilloscope, Logic Analyzer, PCB Design, RF Testing Equipment

EXPERIENCE

Research Assistant, Ultra-Wideband Receiver Design (University of Toronto) Jun 2025 - Jul 2025
Research Intern, X-Lab, University of Toronto *Toronto, ON*

- Verified hybrid PPM+PSK TX chip pre tape-out; built Python/Simulink pipelines for 2ns symbol sync and carrier recovery under discontinuous 4GHz.
- Built pulse-position detection and K-means cluster calibration to mitigate cross-modulation 100ps timing shifts.
- Developed comprehensive verification testbenches and signal integrity analysis for high-speed digital communications.
- Presented at Undergraduate Engineering Research Day with an interactive hybrid-modulation demo site.

Research Assistant, Wireless Power Transfer Coil Design (University of Toronto) Jul 2025 - Aug 2025
Research Intern, X-Lab, University of Toronto *Toronto, ON*

- Designed 13.56MHz WPT coils for a BCI implant (3mm×8mm RX, ˜20mm link).
- Ran HFSS sweeps (turns, trace size, TX diameter) to quantify impacts on coupling (k) and quality factor (Q).
- Produced PCB layouts with tuning plan; distilled design rules and prepared prototypes for validation.
- Performed electromagnetic field simulations and impedance matching optimization for maximum power transfer efficiency.

PROJECTS

FPGA Polyphonic Synthesizer (DE1-SoC) Mar 2025

- Implemented a 20-voice digital synthesizer in C for a Nios-V soft-core, streaming **8 kHz Q15 audio** through the on-chip Audio FIFO.
- Replaced all floating-point math with **32-bit phase accumulators** and fixed-point kernels for sine, square, triangle, and sawtooth waves, enabling real-time mixing and envelope processing.
- Designed an **ADSR envelope engine** driven by slide-switch "knobs" and pushbuttons; state changes are visualized on a double-buffered 320 × 240 VGA UI.
- Integrated PS/2 keyboard interrupts for sub-µs latency note-on/off events; on-screen piano keys light up in sync with hardware playback.
- Built modular drawing primitives (Bresenham, bitmap blits) to render live waveforms and icons; architecture supports future effects or MIDI input with minimal refactor.

Verilog Pac-Man Game (University of Toronto) Nov 2024

- Created a Pac-Man-style FPGA game using Verilog supporting PS/2 keyboard input and VGA output.
- Implemented complex finite state machines for game logic, sprite rendering, and collision detection.
- Debugged signal synchronization issues and state-machine logic, boosting overall stability and playability.
- Designed custom VGA controller with pixel-perfect timing and double-buffering for smooth animation.
- Automated image conversion using Python + OpenCV for seamless integration of game graphics.

Photogate Speed Measurement System High School Project

- Designed and built 10 laser-based speed measurement units with 7-segment displays for high school physics education.
- Achieved sub-150us measurement precision using Arduino microcontrollers and custom PCB design.
- Developed custom infrared communication protocol supporting 32-byte data transmission for wireless control.
- Implemented precise timing circuits with crystal oscillators and interrupt-driven measurement algorithms.
- Integrated 3D printed components and aluminum framework for durable classroom-ready construction.

Digital Signal Processing on FPGA Academic Project

- Implemented real-time FIR and IIR filters in Verilog for audio signal processing applications.
- Designed pipelined multiplier architectures to achieve high-throughput signal processing at 100MHz+.
- Developed comprehensive testbenches with automated verification using SystemVerilog assertions.
- Optimized resource utilization achieving 85% LUT efficiency while meeting timing constraints.

RF Circuit Analysis and Design Academic Project

- Designed and simulated low-noise amplifiers and voltage-controlled oscillators using LTSpice.
- Performed S-parameter analysis and stability analysis for multi-stage amplifier designs.
- Implemented impedance matching networks for maximum power transfer in RF applications.
- Conducted Monte Carlo analysis for process variation tolerance and yield optimization.

Core AI Developer, Wrong-Tree Unity Game Dec 2024 - Jan 2025

- Designed 9-state finite state machine (Idle, Wander, Share, Steal, Flee) for intelligent NPC behaviors in Unity.
- Implemented AI decision-making algorithms with proximity detection and dynamic reputation scoring.
- Created multi-NPC interaction framework supporting simultaneous share/steal operations with visual feedback animations.
- Built modular utility systems including random walk algorithms and distance-based targeting for scalable codebase.

City Mapify – Interactive City Mapping Application (University of Toronto) Jan 2025 - Apr 2025

- Developed a high-performance mapping engine in C++ to process OpenStreetMap data and render city maps.
- Designed efficient spatial data structures (**quadtrees**) for dynamic querying and smooth zoom-based rendering.
- Implemented advanced pathfinding algorithms (**Dijkstra, A***) for route planning and optimization.
- Enhanced performance with multithreading (OpenMP) for parallel processing of large datasets.

AWARDS & ACCOMPLISHMENTS

University of Toronto Excellence Award (UTEA) Apr 2025

- Awarded UTEA for top academic performance and research potential.
- Completed a 14-week full-time research project with faculty supervision.
- Received $7,500 scholarship for research excellence and inclusion.

ECE Awards & Dean's List Scholar (UofT) Sep 2024

- Recognized for outstanding academic performance in Electrical and Computer Engineering.