

# Yongkang Cheng

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## EDUCATION

University of Toronto, Toronto, ON

Sep 2023 – May 2028 (expected)

BASc Computer Engineering + PEY Co-op, cGPA: 3.87/4.0 (88.6%)

Relevant: Digital Systems, Computer Organization, (In progress) Digital Electronics, Operating Systems

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## TECHNICAL SKILLS

- **Programming:** C/C++, Python, Verilog, Assembly (RISC-V), MATLAB/Simulink, JavaScript, Java
  - **Systems:** Operating Systems, Multithreading, Memory Management, Synchronization, Drivers (FPGA/Embedded)
  - **EDA Tools:** Quartus, Vivado, ModelSim, LTSpice, Ansys HFSS, Altium Designer, Rhinoceros, Blender, 3Ds Max
  - **Tools & Libraries:** I2C, SPI, OpenCV, PyTorch, Pandas, FastAPI, Nginx, Git, Linux
  - **Hardware:** Raspberry Pi (5, zero, pico), STM32, Soldering, 3D Printing, Oscilloscope, Logic Analyzer, Multimeter
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## EXPERIENCE

Research Assistant, Ultra-Wideband Receiver Design

May 2025 - Jul 2025

Research Intern, X-Lab, University of Toronto

Toronto, ON

- Collaborated in a 2-person team, verified a hybrid 2-PPM + 8-PSK TX chip pre-tapeout; built Python/Simulink pipelines for 2 ns symbol sync and carrier recovery under discontinuous 4 GHz.
  - Built pulse-position detection and K-means phase calibration for constellation stabilization and PPM demodulation.
  - Achieved error-free demodulation across 2,500 symbols under  $\geq 13$  dB SNR (AWGN) and  $\pi/16$  phase jitter.
  - Automated simulation/test flows with Python scripts for waveform analysis and regression testing.
  - Presented at Undergraduate Engineering Research Day with a [poster](#) and an interactive demo [site](#).
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## PROJECTS

FPGA Polyphonic Synthesizer (DE1-SoC, RISC-V)

Mar 2025

- Developed a 20-voice soft-core audio engine (C on Nios-V) streaming 8 kHz Q15 samples via audio FIFO; optimized kernels by replacing floating-point with fixed-point arithmetic.
- Designed and integrated interrupt service routines for PS/2 input and a double-buffered 320×240 VGA display pipeline, ensuring synchronized graphics rendering with deterministic latency.
- Built modular graphics primitives and interface APIs to enable scalable user interaction under real-time performance constraints.

Verilog Pac-Man (Custom VGA Controller)

Nov 2024

- Implemented low-level VGA timing and synchronization logic, similar to display controller driver design.
- Synchronized pixel timing with PS/2 input; scripted ModelSim stimuli to resolve metastability and timing issues.

WillPower (Distributed Embedded Monitoring)

Jan 2025 – Feb 2025

- Built Raspberry Pi capture node → FastAPI/Nginx pipeline (libcurl + structured endpoints) for continuous image telemetry.
- Added resiliency (retries, time-stamped storage) and modular hooks for on-device filtering / future inference.

City Mapify (C++ Performance Engine)

Jan 2025 – Apr 2025

- Implemented QuadTree spatial index and pathfinding (Dijkstra/A\*/metaheuristics) with cache-friendly adjacency layout enabling fast rendering (60 FPS) on 2GB map data.
  - Designed modular pathfinding kernel (templated weight + heuristic policy) allowing rapid addition of new optimization heuristics.
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## AWARDS

• **University of Toronto Excellence Award (UTEA)**

Apr 2025

\$7,500 scholarship for 6 students among 2nd to 4th ECE for research potential.

• **ECE Awards**

Sep 2024

Awarded to top 30 students in the first-year ECE program out of 300+ students.