Yongkang Cheng
chengyongkang.me | 437-663-2855 | iwmain@outlook.com | github.com/Ken-2511

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Dear Hiring Team,

I'm applying because I like the exact moment when a line of code becomes a timing edge or a measurable signal—and I want more of that. I've gone deep in software (C++ performance work, Python/ML projects), but real silicon / firmware chances have been fewer; I want to bring strong software habits while growing fast on the hardware side.

Briefly: I've built enough FPGA / embedded pieces (PS/2 path, VGA timing, fixed-point audio on a Nios-V RISC-V soft core) to learn to think in clocks, resource trade-offs, and clean reset/state contracts. I also self-studied basic wireless/digital comms while building a hybrid 2-PPM + 8-PSK demod pipeline that I calibrated to zero-BER at $\geq$ 13 dB SNR—giving me a taste for adaptation and link-style tuning.

I like turning manual steps into tiny scripts (Makefile builds, vector generators, quick log diffs). Day one I can write clear Verilog/SystemVerilog control logic, add lightweight counters/status, and build Python/C harnesses to exercise registers and capture metrics—while actively leveling up in SerDes concepts, assertions/coverage, and structured lab bring-up.

Your focus on high-performance connectivity and reusable internal kits matches exactly how I like to work: make behavior observable, automate the boring parts, keep code readable. I'd love to contribute useful tooling and clean firmware while strengthening my hardware intuition.

Thank you for your consideration.

Sincerely,

Yongkang Cheng