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Dear Tenstorrent Hiring Team,

I am a Computer Engineering PEY student at the University of Toronto (cGPA 3.87/4.0) and I am applying for the AI SoC Design Verification PEY role in Toronto. Tenstorrent's vision of unifying RISC-V compute, AI software, and verification rigor is exactly where I want to grow. I am available full-time on-site and eager to help verify the next generation of AI/CPU chiplets before they hit silicon.

My current research in X-Lab has me taking over a teammate's spiking neural network accelerator, refactoring the Verilog, and building ModelSim testbenches that inject parameterized stimuli, assertions, and randomized corner cases. I scripted tests and validated the design on a Nexys Video board, plumbing observability hooks for upcoming system integration. This experience sharpened my ability to reason about clock-domain boundaries, reset contracts, and functional coverage in a fast-moving academic environment.

Earlier this year I co-led pre-tapeout verification of an ultra-wideband 4-PPM + 8-PSK transceiver. We constructed Python/Simulink pipelines to stress timing, jitter, and SNR sensitivities, achieving error-free demodulation across 2,500 symbols at ≥ 16 dB SNR. Translating algorithmic insights into directed and randomized tests taught me how to trace bugs across mixed-signal models, correlate lab measurements with simulation, and communicate results to a small multi-disciplinary team.

I back this with project work that blends RTL, tooling, and performance intuition: a 20-voice FPGA synthesizer (C on Nios-V) where I automated interrupt-driven testbenches and VGA diagnostics; a Verilog Pac-Man game whose FSMs I debugged via scripted ModelSim runs; and a C++ mapping engine with cache-aware data layouts, reinforcing how microarchitectural behavior surfaces at the software layer. Across these efforts I default to writing harnesses, coverage trackers, and log-diff scripts so verification stays reproducible.

I am excited to bring disciplined test planning, readable RTL, and automation habits to Tenstorrent while deepening my SystemVerilog, UVM, and coverage expertise under your mentorship. Thank you for considering my application; I would love to discuss how I can contribute to Tenstorrent's AI SoC verification pipeline.

Sincerely,

Yongkang Cheng