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Dear Hiring Team,

I'm writing to express my strong interest in the ASIC/FPGA Intern position at Alphawave. The blend of RTL design, functional verification, and scripting-driven workflow improvement matches exactly what I've been building toward. I'm drawn to environments that prize engineering rigor, reproducibility, and automation—and everything I've learned about Alphawave signals that culture.

Over the past two years I've combined digital design with disciplined software practice: implementing FSMs, fixed-point datapaths, pipelined audio/graphics subsystems, and self-checking ModelSim testbenches (wave.do iteration, scripted runs). These projects trained me to think in cycles, timing margins, reset/handshake contracts—beyond pure algorithms.

At X-Lab I recently initiated an FPGA acceleration effort for a quantized spiking neural network, scoping a parameterizable compute fabric (LUT/BRAM tradeoffs) while evaluating accuracy vs. latency under fixed-point quantization. Standing it up required fast, clean RTL, a stubbed verification harness, and a Python regression plan for iterative synthesis—an automation-first mindset I'd bring to your team.

Earlier this summer I helped verify a hybrid ultra-wideband (2-PPM + 8-PSK) modulation chain pre-tapeout by building Python + Simulink co-simulation pipelines, adding clustering-based phase/timing calibration, and driving zero-BER test vectors under injected SNR and phase jitter. That reinforced habits of targeted test case design, traceable issue logging, and rapid closure.

I differentiate myself through: care for RTL readability and naming discipline; turning ad-hoc flows into reusable Python/Bash/Tcl scripts; a strong C/C++ & Python background that complements hardware intuition; and fast, rigorous debugging.

Alphawave's focus on high-performance connectivity IP aligns with my long-term goal of building efficient, verifiable interface blocks—and proximity enables full on-site commitment. I'd welcome the chance to contribute to standards-compliant, well-verified IP while streamlining internal flows.

Thank you for your consideration; I look forward to the possibility of speaking with you.

Sincerely,

Yongkang Cheng