Main features of MIPSfpga+ external interrupt controller:

* very simple;
* up to 64 interrupts with independent interrupt vectors;
* the count of interrupts can be customized;
* two types of interrupt channels: direct channel and sense channel. The second type can be tuned to take only the low signal value, any logical change of input signal, the falling edge of input signal, or the rising edge of input signal.
* up to 32 sense channel interrupts;
* full supports of microAptiv™ external interrupt controller operation options: 'Explicit Vector Number' and 'Explicit Vector Offset' - the interrupt handler offset can be directly transmitted to the CPU. For details see the chapter 5.3.1.3 in 'MIPS32® microAptiv™ UP Processor Core Family Software User’s Manual, Revision 01.02';
* merged to MIPSfpga+ github project: <https://github.com/MIPSfpga/mipsfpga-plus>
* EIC usage example was included (MIPSfpga+/programs/07\_iec);
* there is a standalone github project for controller debug: <https://github.com/zhelnio/ahb_lite_eic>
* to enable EIC uncomment option 'MFP\_USE\_IRQ\_EIC' in **mfp\_ahb\_lite\_matrix\_config.vh** to set other setting use **mfp\_eic\_core.vh**

Files

mfp\_eic\_core.v IEC core;

mfp\_eic\_core.vh main configuration file (see comments inside);

mfp\_eic\_handler.v contains the logic to convert interrupt number to calling handler parameters: priority, vector number, offset;

mfp\_eic\_priority\_encoder.v tree structure of priority encoders;

mfp\_ahb\_lite\_eic.v top-level module, contains the interface to the system bus