Lab 8
pipeline

Simple operation with pipeline

- Mode0: in_1 * in_2
- Mode1: in_3 + in_4
- Mode2: in_1 * in_2 * in_3 * in_4
- Think twice before writing code

pipe.sv

Input Signal	Bit Width	Definition
clk	1	4 ns
rst_n	1	Asynchronous reset when reset negedge, all output should be zero
in_1	6	Value:0~63, won’t stop until pattern over.
in_2	6	Value:0~63, won’t stop until pattern over.
in_3	6	Value:0~63, won’t stop until pattern over.
in_4	6	Value:0~63, won’t stop until pattern over.
mode	2	0 or 1 or 2, choose calculate mode
in_valid	1	High until all inputs are given

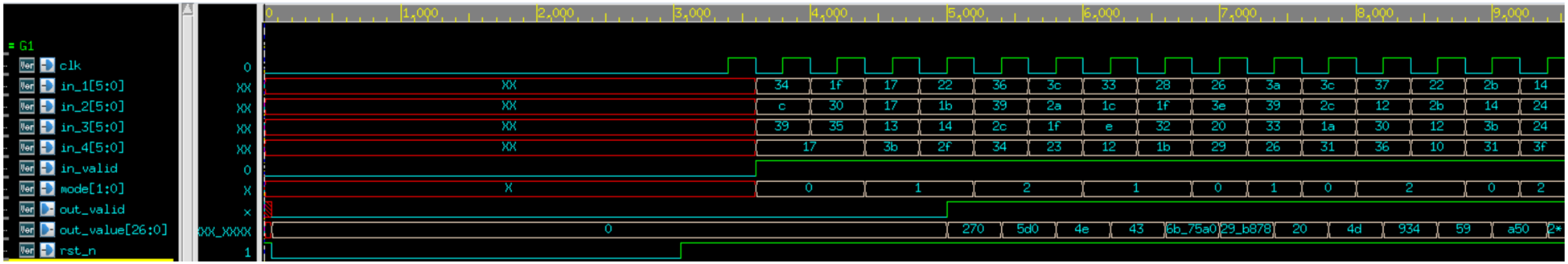
Output Signal	Bit Width	Definition
out_valid	1	High until all answers are done.
out_value	27	Output answer

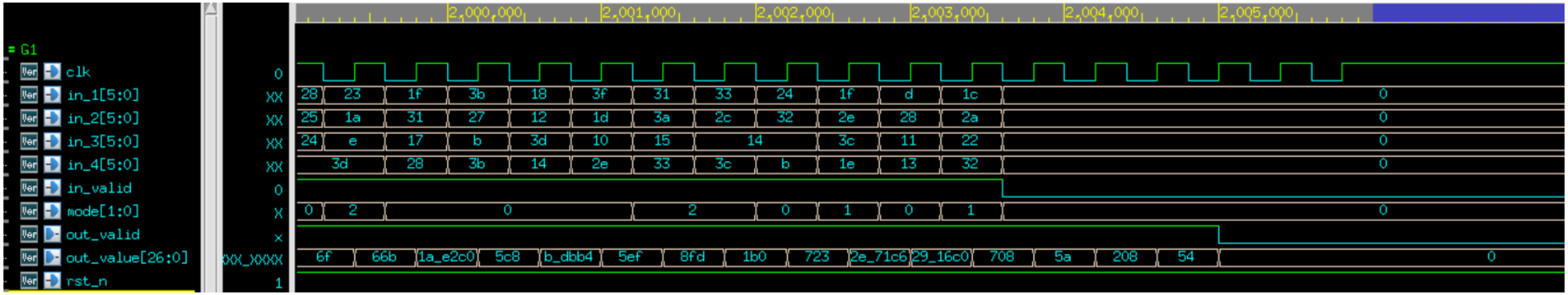
Spec

- Top module name : PIPE (File name: PIPE.sv)
- All output signal should be reset (=0) after the reset signal is asserted.
- 01_RTL PASS
- 02_SYN result cannot include any error and latches.
- After synthesis, your slack in timing report should be MET
- 03_GATE PASS
- You must use pipeline. Since clock is 4ns.
- After output done , output signal should be zero.

Output & Waveform

- Waveform


G1
clk 0
in_1[5:0] XX
in_2[5:0] XX
in_3[5:0] XX
in_4[5:0] XX
in_valid 0
mode[1:0] X
out_valid x
out_value[26:0] XX_XXXX
rst_n 1
0
1,000
2,000
3,000
4,000
5,000
6,000
7,000
8,000
9,000
XX 34 1f 17 22 36 3c 33 28 26 3a 3c 37 22 2b 14
XX c 30 17 1b 39 2a 1c 1f 3e 39 2c 12 2b 14 24
XX 39 35 13 14 2c 1f e 32 20 33 1a 30 12 3b 24
XX 17 3b 2f 34 23 12 1b 29 26 31 36 10 31 3f
X 0 1 2 1 0 1 0 2 0 2
0 270 5d0 4e 43 6b_75a0 29_b878 20 4d 934 59 a50 2*


G1
clk 0
in_1[5:0] XX
in_2[5:0] XX
in_3[5:0] XX
in_4[5:0] XX
in_valid 0
mode[1:0] X
out_valid x
out_value[26:0] XX_XXXX
rst_n 1
2,000,000
2,001,000
2,002,000
2,003,000
2,004,000
2,005,000
28 23 1f 3b 18 3f 31 33 24 1f d 1c 0
25 1a 31 27 12 1d 3a 2c 32 2e 28 2a 0
24 e 17 b 3d 10 15 14 3c 11 22 0
3d 28 3b 14 2e 33 3c b 1e 13 32 0
0 2 0 2 0 1 0 1 0
6f 66b 1a_e2c0 5c8 b_dbb4 5ef 8fd 1b0 723 2e_71c6 29_16c0 708 5a 208 54 0

In_valid and out_valid pull high continuously

Command

- tar -xvf ~dcsTA01/Lab08.tar
- Upload
  - cd 09_upload
  - ./01_upload
  - ./02_download demoX

DEMO1 : 5/2 17:30:00

DEMO2 : 5/3 23:59:59