Lab Report 3
Multiplexer and Decoder
ECE 238L

Kenneth Cox

March 27, 2021

Date Performed:	Mar 26, 2021
Instructor:	Professor Hamke

1 Items

Gates

Multiplexer

7 Segment Display

Top Level Module

2 Feedback

Initially, on my first attempt at this lab it was, at least the Decoder, somewhat confusing.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Gates is
    Port ( A, B : in STD_LOGIC;
           G_Out : out STD_LOGIC_VECTOR (7 downto 0));
end Gates;

architecture Behavioral of Gates is

begin
   g_out(0) <= A;
   g_out(1) <= not B;
   g_out(2) <= A and B;
   g_out(3) <= A or B;
   g_out(4) <= A nand B;
   g_out(5) <= A nor B;
   g_out(6) <= A xor B;
   g_out(7) <= A xnor B;


end Behavioral;
```

Figure 1: source

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity gates_tb is
end gates_tb;

architecture bench of gates_tb is

component Gates
  Port (a, b: in std_logic;
        g_out: out std_logic_vector(7 downto 0));
end component;

signal a_tb, b_tb :std_logic;
signal g_out_tb : std_logic_vector(7 downto 0);

begin
  uut:Gates port map ( A => a_tb,
                       B => b_tb,
                       G_out => g_out_tb);

stimulus:process
  begin
    a_tb <= '0'; b_tb <= '0'; wait for 100 ns;
    a_tb <= '0'; b_tb <= '1'; wait for 100 ns;
    a_tb <= '1'; b_tb <= '0'; wait for 100 ns;
    a_tb <= '1'; b_tb <= '1'; wait for 100 ns;
    wait;
  end process;
end bench;
```

Figure 2: test bench

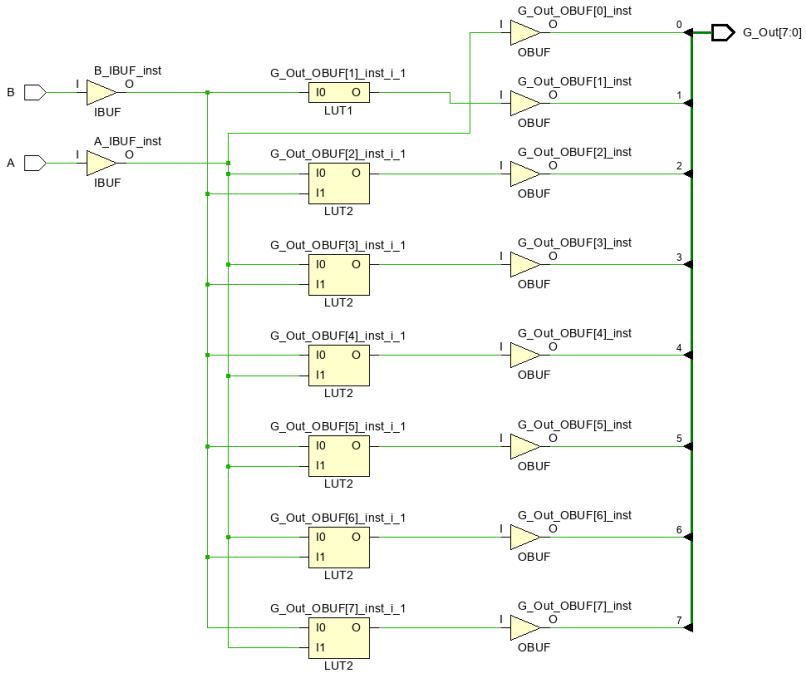

Figure 3: Schematic

G_Out_OBUF[1]_inst_i_1

I0	O=!I0
0	1
1	0

Figure 4: Truth Table

G_Out_OBUF[2]_inst_i_1

I1	I0	O=I0 & I1
0	0	0
0	1	0
1	0	0
1	1	1

Figure 5: Truth Table

G_Out_OBUF[3]_inst_i_1

I1	I0	O=I0 + I1
0	0	0
0	1	1
1	0	1
1	1	1

Figure 6: Truth Table

G_Out_OBUF[4]_inst_i_1

I1	I0	O=!I0 + !I1
0	0	1
0	1	1
1	0	1
1	1	0

Figure 7: Truth Table

G_Out_OBUF[5]_inst_i_1

I1	I0	O=!I0 & !I1
0	0	1
0	1	0
1	0	0
1	1	0

Figure 8: Truth Table

G_Out_OBUF[6]_inst_i_1

I1	I0	O=I0 & !I1 + !I0 & I1
0	0	0
0	1	1
1	0	1
1	1	0

Figure 9: Truth Table

G_Out_OBUF[7]_inst_i_1

I1	I0	O=!I0 & !I1 + I0 & I1
0	0	1
0	1	0
1	0	0
1	1	1

Figure 10: Truth Table

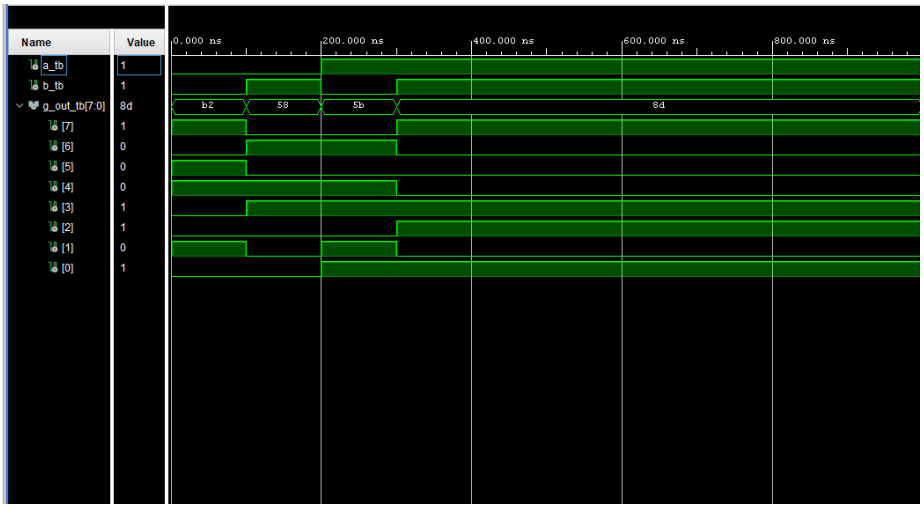

Figure 11: Truth Table

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Multiplexer_8_1 is
    Port ( mux_in : in STD_LOGIC_VECTOR (7 downto 0);
           Selector : in STD_LOGIC_VECTOR (2 downto 0);
           mux_out : out STD_LOGIC);
end Multiplexer_8_1;

architecture Behavioral of Multiplexer_8_1 is

begin

    mux_out <= mux_in(0) when Selector = "000" else
               mux_in(1) when Selector = "001" else
               mux_in(2) when Selector = "010" else
               mux_in(3) when Selector = "011" else
               mux_in(4) when Selector = "100" else
               mux_in(5) when Selector = "101" else
               mux_in(6) when Selector = "110" else
               mux_in(7) when Selector = "111";

end Behavioral;
```

Figure 12: source

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Multiplexer_tb is
--  Port ( );
end Multiplexer_tb;

architecture bench of Multiplexer_tb is

component Multiplexer_8_1
  Port (Selector: in std_logic_vector(2 downto 0);
        mux_in:in std_logic_vector(7 downto 0);
        mux_out: out std_logic);
end component;

signal selector_tb : std_logic_vector(2 downto 0);
signal g_out_tb : std_logic_vector(7 downto 0);
signal mux_out_tb : std_logic;

begin

  uut: Multiplexer_8_1 port map(Selector => selector_tb,
                           mux_in => g_out_tb,
                           mux_out => mux_out_tb);
  stimulus: process
    begin
      Selector_tb <= "000"; g_out_tb <= "00000001"; wait for 100 ns;
      Selector_tb <= "001"; g_out_tb <= "00000010"; wait for 100 ns;
      Selector_tb <= "010"; g_out_tb <= "00000100"; wait for 100 ns;
      Selector_tb <= "011"; g_out_tb <= "00001000"; wait for 100 ns;
      Selector_tb <= "100"; g_out_tb <= "00010000"; wait for 100 ns;
      Selector_tb <= "101"; g_out_tb <= "00100000"; wait for 100 ns;
      Selector_tb <= "110"; g_out_tb <= "01000000"; wait for 100 ns;
      Selector_tb <= "111"; g_out_tb <= "10000000"; wait for 100 ns;
      wait;
  end process;
end bench;
```

Figure 13: test bench

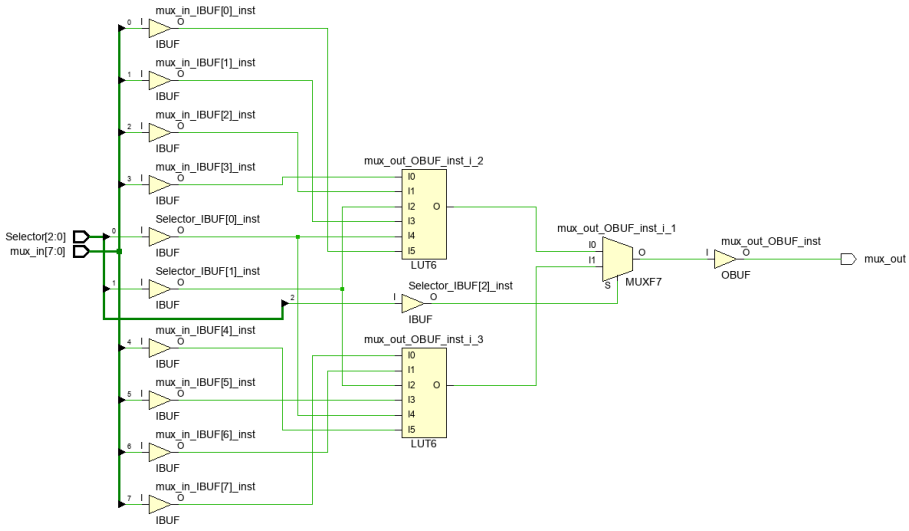

Figure 14: Schematic

mux_out_OBUF_inst_i_3

I5	I4	I3	I2	I1	I0	O=I1 & I2 & !I4 + I0 & I2 & I4 + !I2 & I3 & I4 + !I2 & !I4 & I5
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	0
0	0	1	1	0	1	0
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	1
0	1	0	1	1	0	0
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	1
0	1	1	1	1	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	0	0	0	1	1
1	0	0	0	1	0	1
1	0	0	0	1	1	1
1	0	0	1	0	0	0
1	0	0	1	0	1	0

mux_out_OBUF_inst_i_2

I5	I4	I3	I2	I1	I0	O=I1 & I2 & !I4 + I0 & I2 & I4 + !I2 & I3 & I4 + !I2 & !I4 & I5
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	0
0	0	1	1	0	1	0
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	1
0	1	0	1	1	0	0
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	1
0	1	1	1	1	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	0	0	0	1	1
1	0	0	0	1	0	1
1	0	0	0	1	1	1
1	0	0	1	0	0	0
1	0	0	1	0	1	0

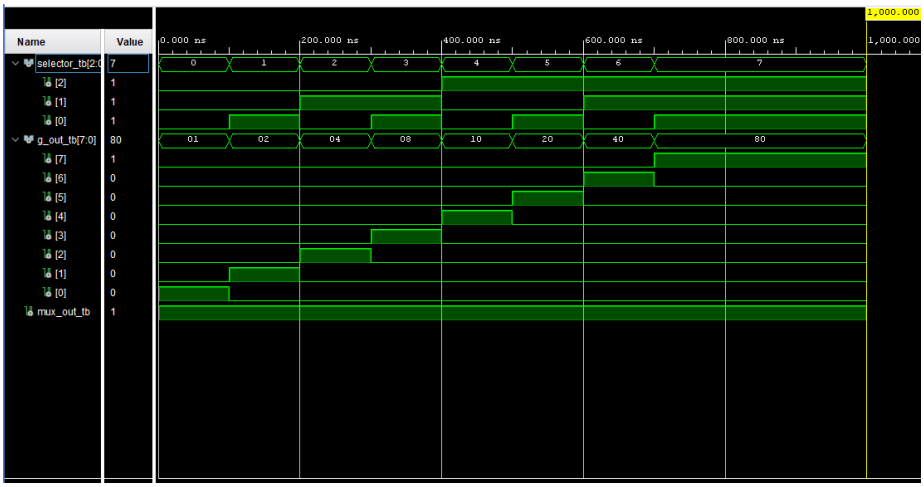

Figure 17: Waveform

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity DispDigit is
    Port ( mux_out : in STD_LOGIC;
           cathode_7sd, anode_7sd : out STD_LOGIC_VECTOR (7 downto 0));
end DispDigit;

architecture Behavioral of DispDigit is

begin
  process(Mux_out)
  begin

    if Mux_out = '1' then
      Cathode_7SD <= "10010001";
    else
      Cathode_7Sd <= "11100011";
    end if;
  end process;

  Anode_7SD <= "11111110";

end Behavioral;
```

Figure 18: source

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Display_tb is
--  Port ( );
end Display_tb;

architecture bench of Display_tb is

component DispDigit is
    Port ( mux_out : in STD_LOGIC;
           cathode_7sd, anode_7sd : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal mux_out_tb : std_logic;
signal cathode_7sd_tb, Anode_7sd_tb : std_logic_vector(7 downto 0);

begin

  uut: DispDigit port map( mux_out => mux_out_tb,
                           cathode_7sd => cathode_7sd_tb,
                           anode_7sd => anode_7sd_tb);

stimulus: process
  begin
    mux_out_tb <= '0'; wait for 100 ns;
    mux_out_tb <= '1'; wait for 100 ns;
    wait;
  end process;
end bench;
```

Figure 19: test bench

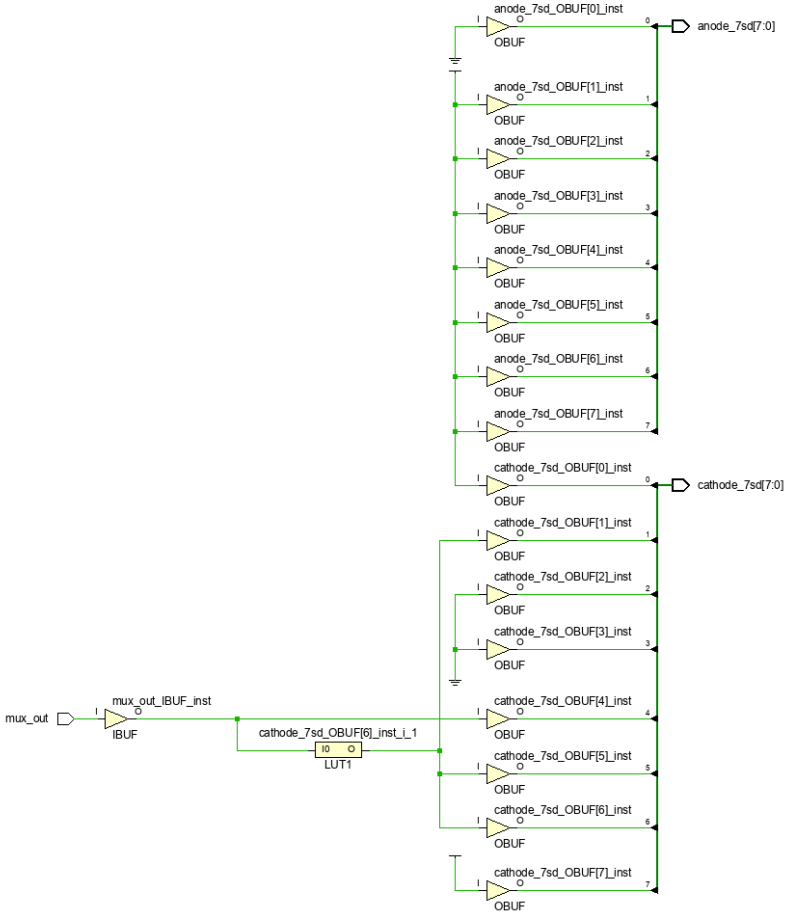

Figure 20: Schematic

cathode_7sd_OBUF[6]_inst_i_1

I0	O=!I0
0	1
1	0

Figure 21: Truth Table

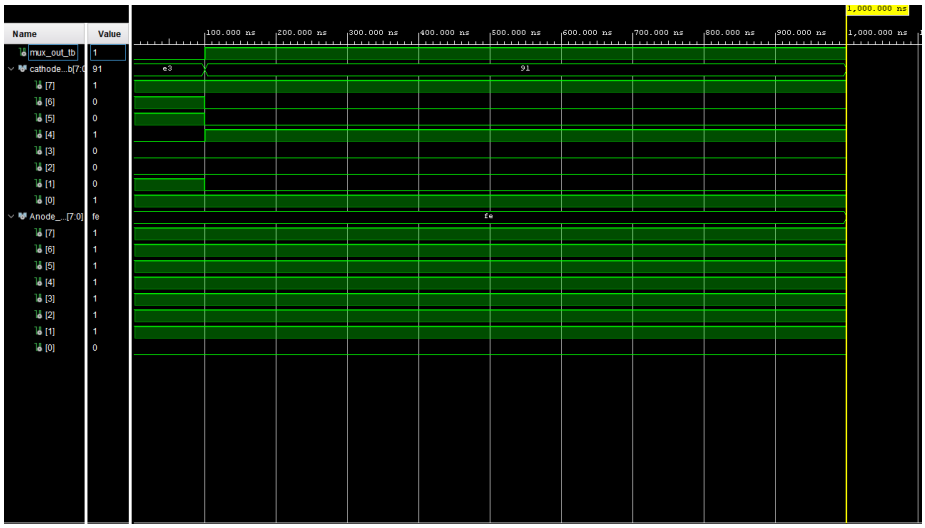

Figure 22: Wavefrom

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Lab3 is
    Port ( A, B : in STD_LOGIC;
           Selector : in STD_LOGIC_VECTOR (2 downto 0);
           Cathode_7SD, Anode_7SD : out STD_LOGIC_VECTOR (7 downto 0));
end Lab3;

architecture Behavioral of Lab3 is

component Gates is
    Port ( A, B : in STD_LOGIC;
           G_Out : out STD_LOGIC_VECTOR (7 downto 0));
end component;

component Multiplexer_8_1 is
    Port ( mux_in : in STD_LOGIC_VECTOR (7 downto 0);
           Selector : in STD_LOGIC_VECTOR (2 downto 0);
           mux_out : out STD_LOGIC);
end component;


component DispDigit is
    Port ( mux_out : in STD_LOGIC;
           cathode_7sd, anode_7sd : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal MUX8to1: std_logic;
signal G_Out : std_logic_vector(7 downto 0);

begin


  Gates_1: Gates port map( A, B, G_Out);

  Multi_8_1: Multiplexer_8_1 port map(G_Out, Selector, Mux8to1);

  Display_7_Seg: DispDigit port map(Mux8to1, Cathode_7SD, Anode_7SD );


end Behavioral;
```

Figure 23: source

```
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LAB3_TB is
   -- Port ()
end LAB3_TB;

architecture Bench of LAB3_TB is

component Lab3 is
    Port ( A, B : in STD_LOGIC;
           Selector : in STD_LOGIC_VECTOR (2 downto 0);
           Cathode_7SD, Anode_7SD : out STD_LOGIC_VECTOR (7 downto 0));
end component;



signal A_tb :  STD_LOGIC;
signal  B_tb :  STD_LOGIC;
signal Selector_tb : STD_LOGIC_VECTOR (2 downto 0);
signal Cathode_7SD_tb: STD_LOGIC_VECTOR (7 downto 0);
signal Anode_7SD_tb : STD_LOGIC_VECTOR (7 downto 0);

begin

  uut:Lab3 port map(Selector=> Selector_tb,
                    A => A_tb,
                    B => B_tb,
                    Cathode_7SD => Cathode_7SD_tb,
                    Anode_7SD  => Anode_7SD_tb);
stimulus: process

  begin
    Selector_tb <= "000"; A_tb <= '0'; B_tb <= '0'; wait for 100 ns;
    Selector_tb <= "001"; A_tb <= '0'; B_tb <= '1'; wait for 100 ns;
    Selector_tb <= "010"; A_tb <= '1'; B_tb <= '0'; wait for 100 ns;
    Selector_tb <= "011"; A_tb <= '1'; B_tb <= '1'; wait for 100 ns;
    Selector_tb <= "100"; A_tb <= '1'; B_tb <= '0'; wait for 100 ns;
    Selector_tb <= "101"; A_tb <= '0'; B_tb <= '1'; wait for 100 ns;
    Selector_tb <= "110"; A_tb <= '1'; B_tb <= '0'; wait for 100 ns;
    Selector_tb <= "111"; A_tb <= '1'; B_tb <= '1'; wait for 100 ns;
    wait;
  end process;
end Bench;
```

Figure 24: test bench

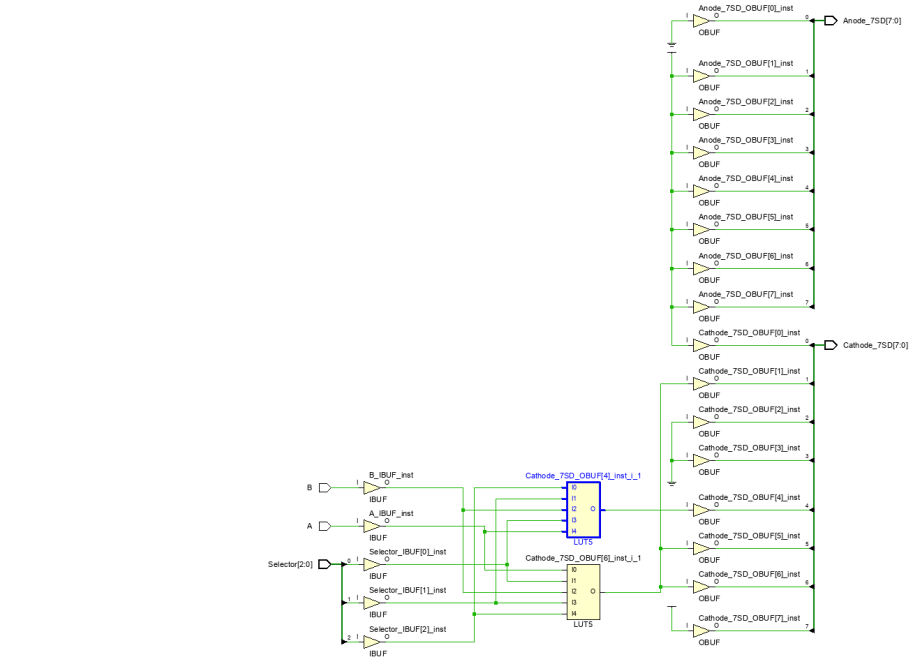

Figure 25: Schematic

Cell Properties

Cathode_7SD_OBUF[4]_inst_i_1

I4	I3	I2	I1	I0	O=I0 & I2 & !I3 & !I4 + I0 & !I2 & I3 & !I4 + !I0 & I1 & I2 & I3 + I0 & !I2 & !I3 & I4 + I1 & I2 & I3 & I4 + !I0 & I2 & !I3 & I4 + !I0 & !I2 & I3 & I4 + I0 & !I1 & !I3 & !I4 + !I1 & !I2 & I3 & !I4 + !I1 & !I2 & !I3 & I4
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	1

Figure 26: Truth Table

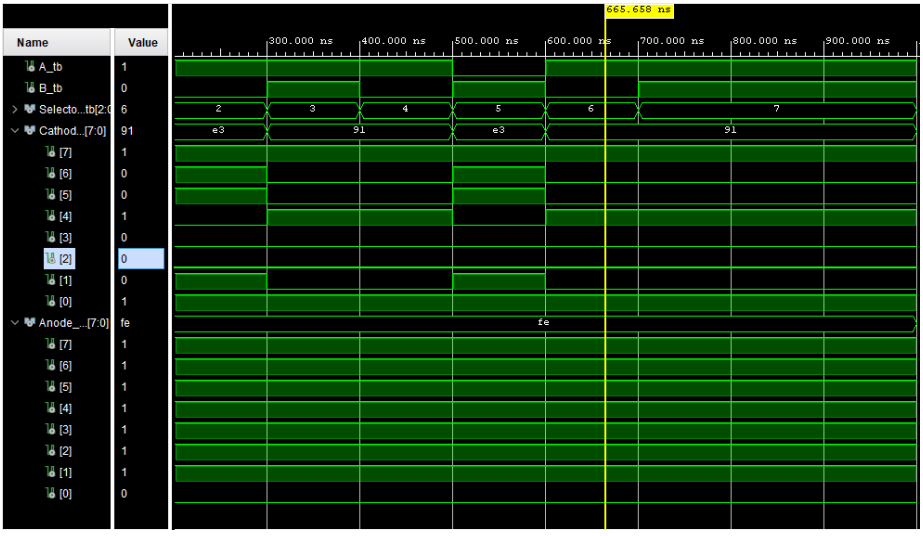

Figure 27: Decoder Wave