Lab1
Comparator and 7-Segment Display
ECE 238

Kenneth Cox

February 19, 2021

Date Performed:	Feb 11, 2021
Section:	003
Instructor:	Professor Eric Hamke

1 VHDL Design Source Files

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LAB01A is
    Port ( A,B : in STD_LOGIC;
           F_E, F_G, F_L : out STD_LOGIC);
end LAB01A;

architecture Behavioral of LAB01A is

begin
    F_E <= (not(A) and not(B)) or (A and B);
    F_G  <= not(A) and B;
    F_L <= (A and not(B));
end Behavioral;
```

Figure 1: Lab 1A source.

```
architecture bench of LAB01A_tb is

    component LAB01A
      port(A,B : in std_logic;
           F_G, F_L, F_E : out std_logic);
    end component;

    signal A_tb, B_tb   : std_logic;
    signal F_G_tb, F_L_tb, F_E_tb    : std_logic;
begin

    uut:LAB01A port map(A => A_tb,
                        B => B_tb,
                        F_G => F_G_tb,
                        F_E => F_E_tb,
                        F_L => F_L_tb);

stimulus: process
    begin
        A_tb <= '0'; B_tb <= '0'; wait for 100 ns;
        A_tb <= '0'; B_tb <= '1'; wait for 100 ns;
        A_tb <= '1'; B_tb <= '1'; wait for 100 ns;
        A_tb <= '1'; B_tb <= '0'; wait for 100 ns;
        wait;
    end process;
end bench;
```

Figure 2: Lab 1A testbench

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity LAB1B is
    Port ( A, B : in STD_LOGIC;
           cathode_7sd : out STD_LOGIC_VECTOR (7 downto 0);
           anode_7sd : out STD_LOGIC_VECTOR (7 downto 0));
end LAB1B;

architecture Comparator of LAB1B is
signal F_E, F_L, F_G: std_logic;
begin
    F_E <= (not(A) and not(B)) or (A and B);
    F_L <= (A) and not(B);
    F_G <= not(A) and B;
process(F_E, F_L, F_G)
  Begin
    if F_E = '1' then
        cathode_7sd <= "11100001";
    elsif F_L = '1' then
        cathode_7sd <= "11100011";
    elsif F_G = '1' then
        cathode_7sd <= "11000001";
    else
        cathode_7sd <= "00000010";
  end if;
end process;
Anode_7sd <= "11111110";
end Comparator;
```

Figure 3: Lab 1B source.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Lab1B_tb is
end Lab1B_tb;

architecture bench of Lab1B_tb is

component Lab1B is
    Port ( A, B : in STD_LOGIC;
           Cathode_7sd : out STD_LOGIC_VECTOR (7 downto 0);
           anode_7sd : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal A_tb, B_tb : std_logic ;
signal Cathode_7sd_tb, Anode_7sd_tb : std_logic_vector (7 downto 0);

begin

 uut:Lab1B port map(A => A_tb,
                    B => B_tb,
                    Cathode_7sd => Cathode_7sd_tb,
                    Anode_7sd => Anode_7sd_tb);

stimulus: process
begin
  A_tb <= '0'; B_tb <= '0'; wait for 100 ns;
  A_tb <= '0'; B_tb <= '1'; wait for 100 ns;
  A_tb <= '1'; B_tb <= '0'; wait for 100 ns;
  A_tb <= '1'; B_tb <= '1'; wait for 100 ns;
  wait;
  end process;
end bench;
```

Figure 4: Lab 1B testbench.

2 Design Schematics

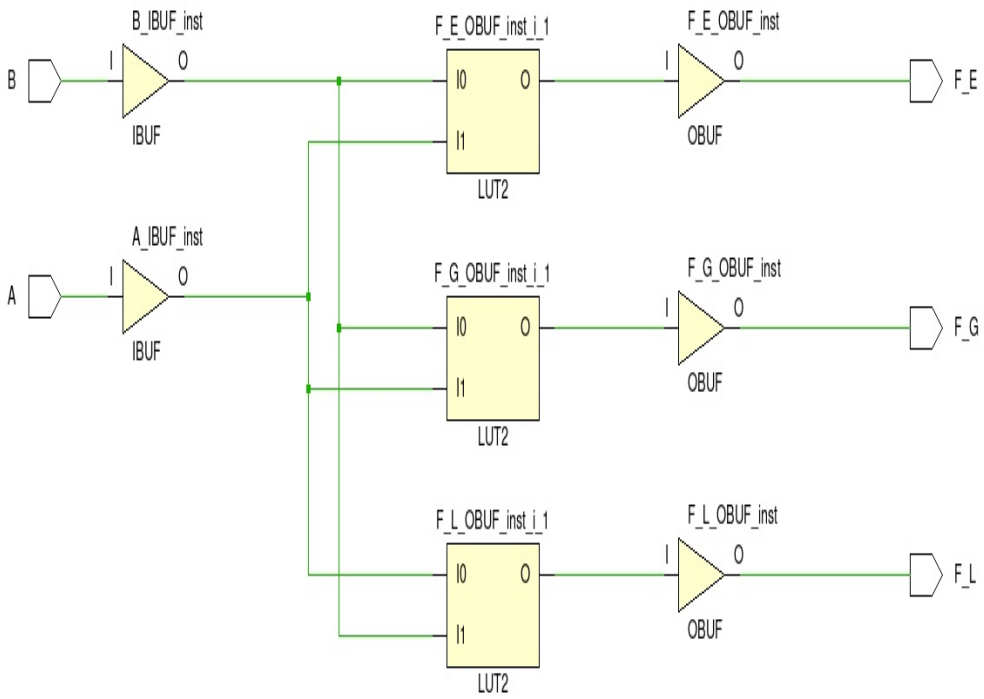

Figure 5: Lab 1A Schematics.

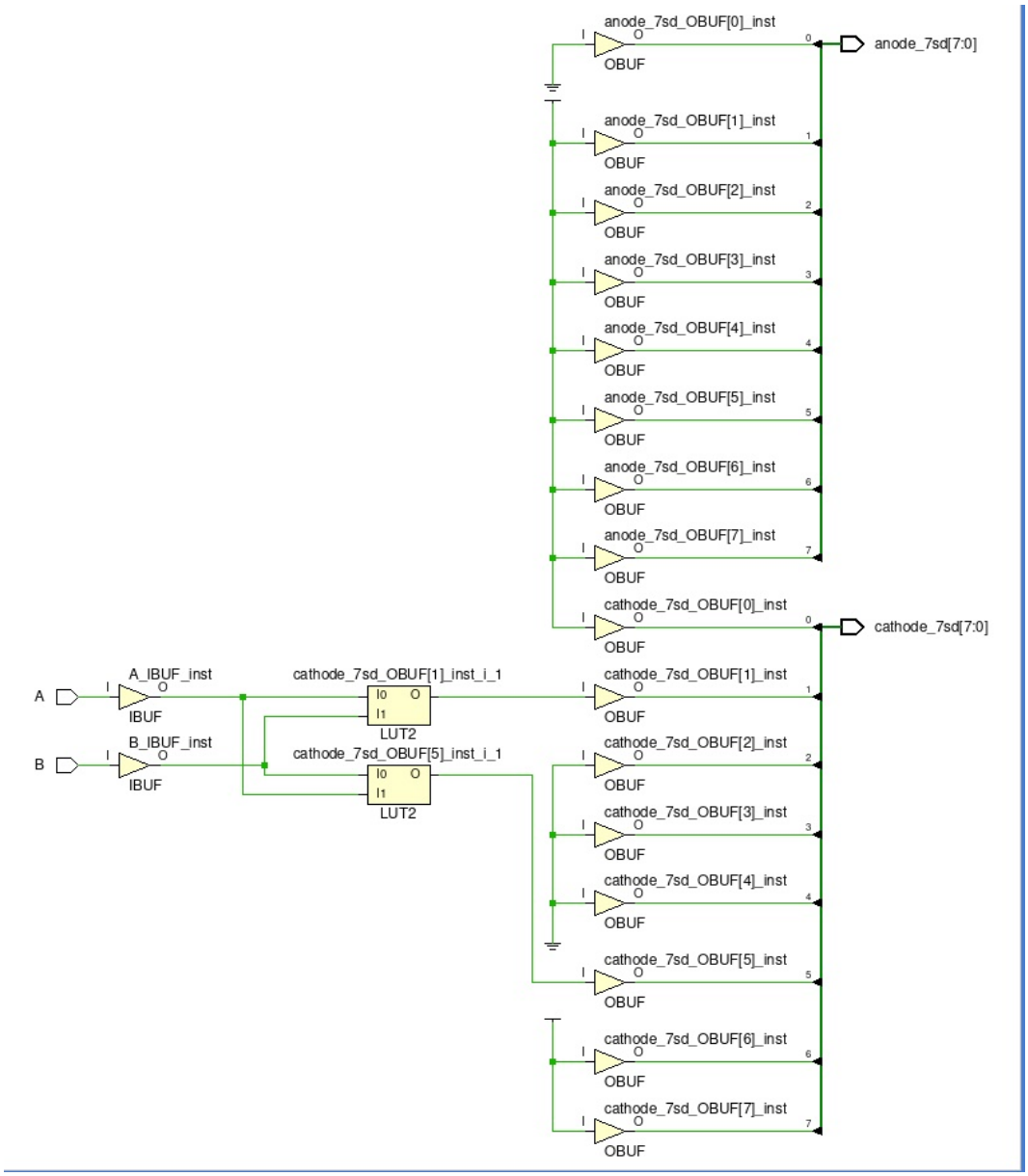

Figure 6: Lab 1B Schematics.

3 Truth Tables

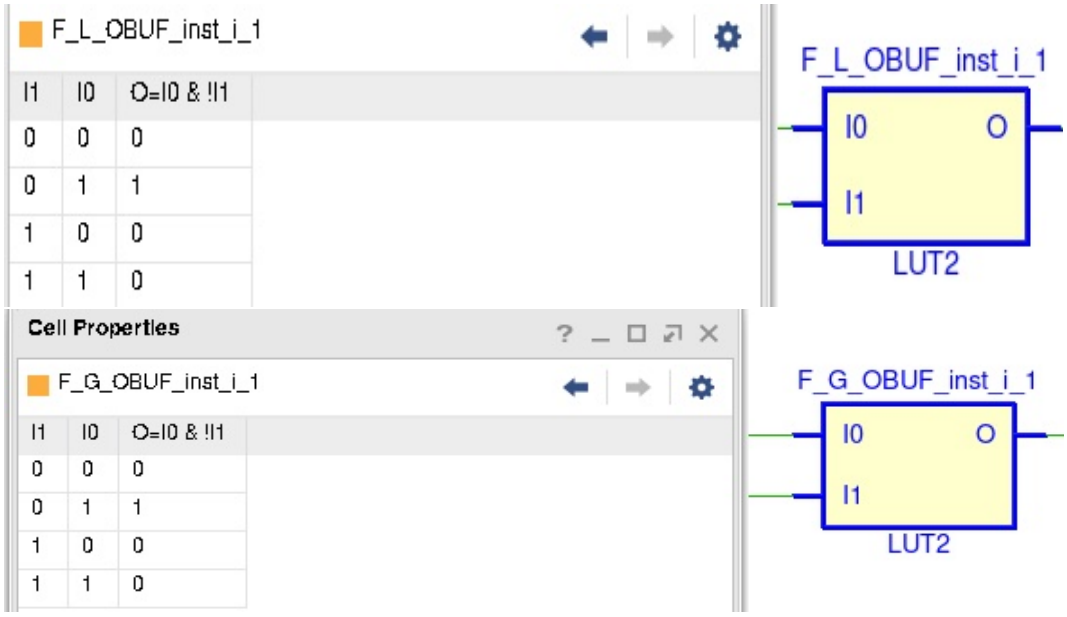

Figure 7: Lab 1A truth tables

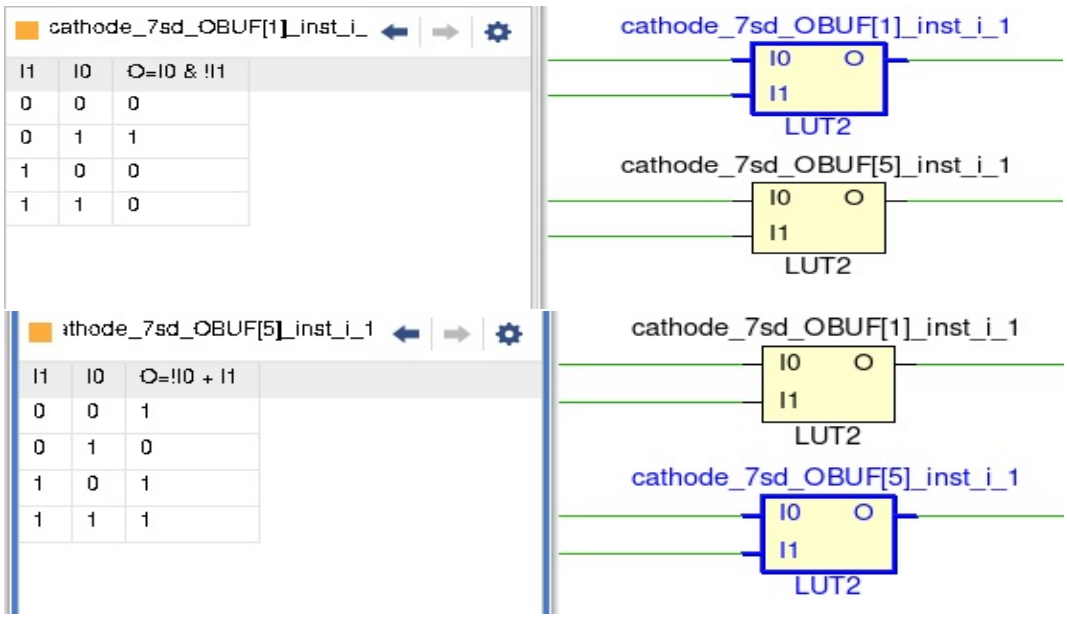

Figure 8: Lab 1B truth tables

4 Waveforms

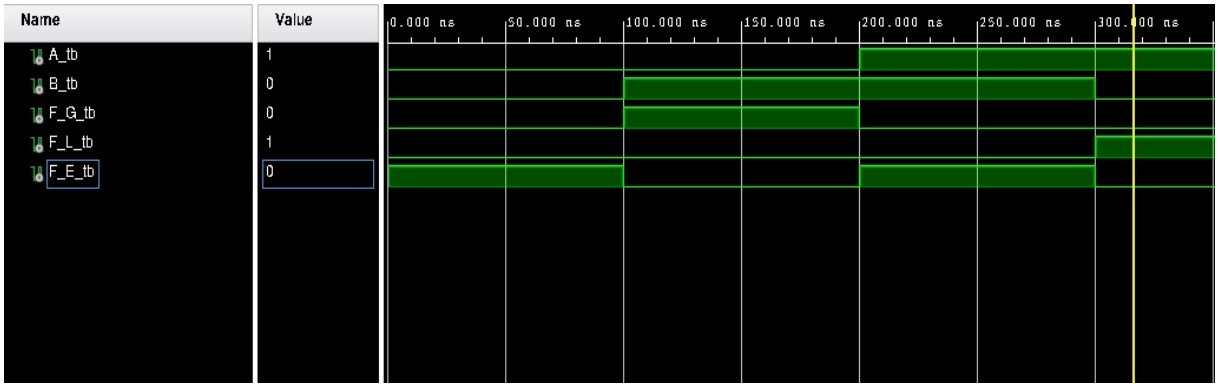

Figure 9: Lab 1A Waveform

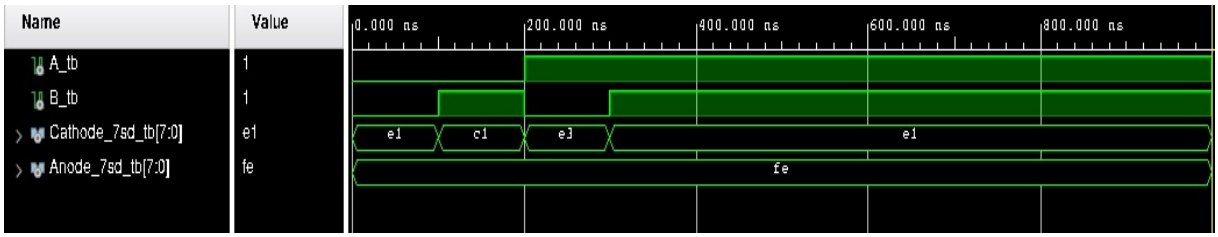

Figure 10: Lab 1B Waveform

5 Summary

This lab was a more independent venture. I frequently had to reference the first lab (Lab 0). A few problems encountered; not having familiarity with VHDL, no code reuse (from what I can tell), and a lack of syntax and data structure knowledge. I am not even sure if data structure is the correct word for what I am trying to describe. I have found resources recently so I can discern the different structures; entity, component, etc... and their applications to a circuit design.