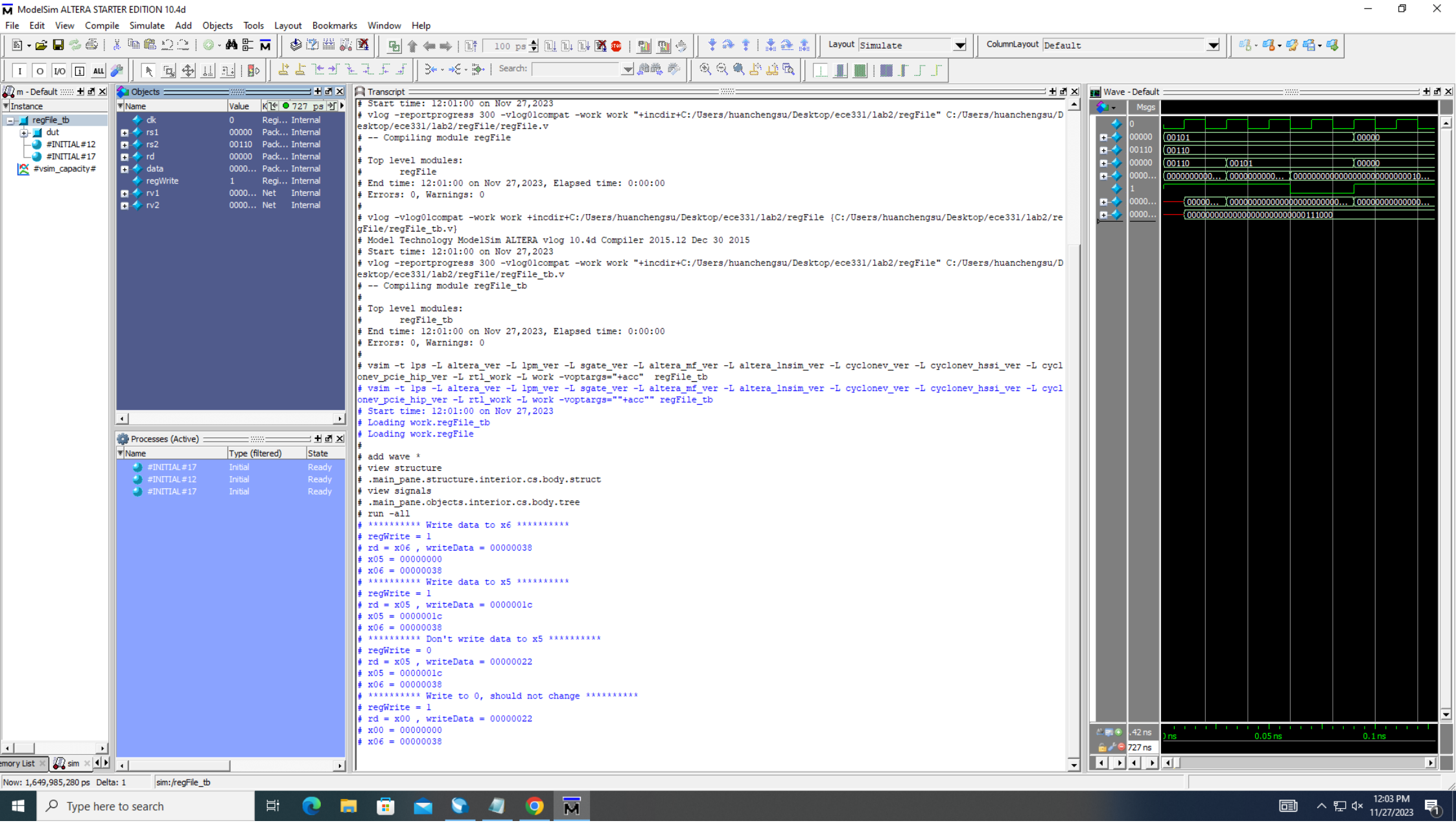
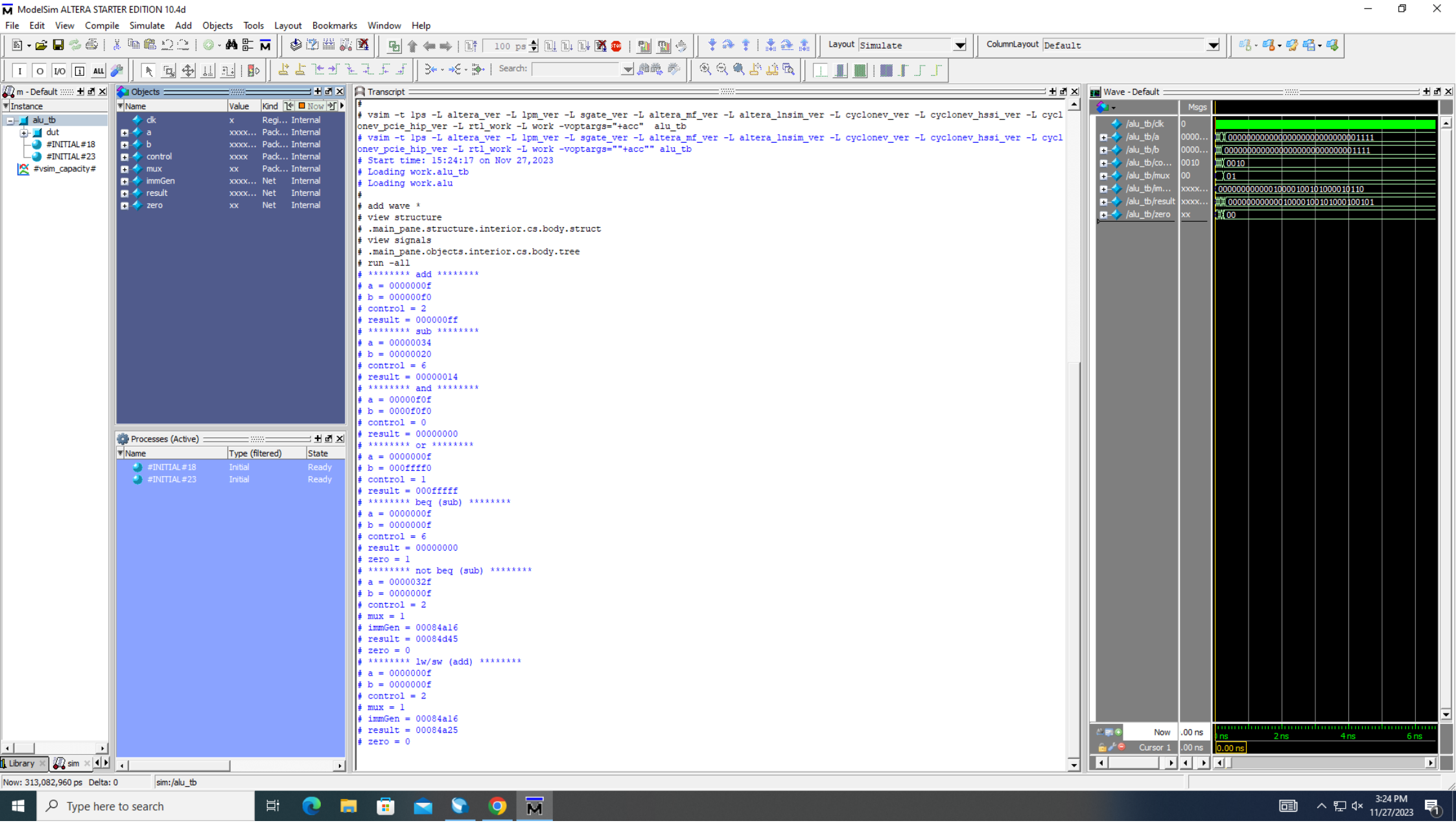
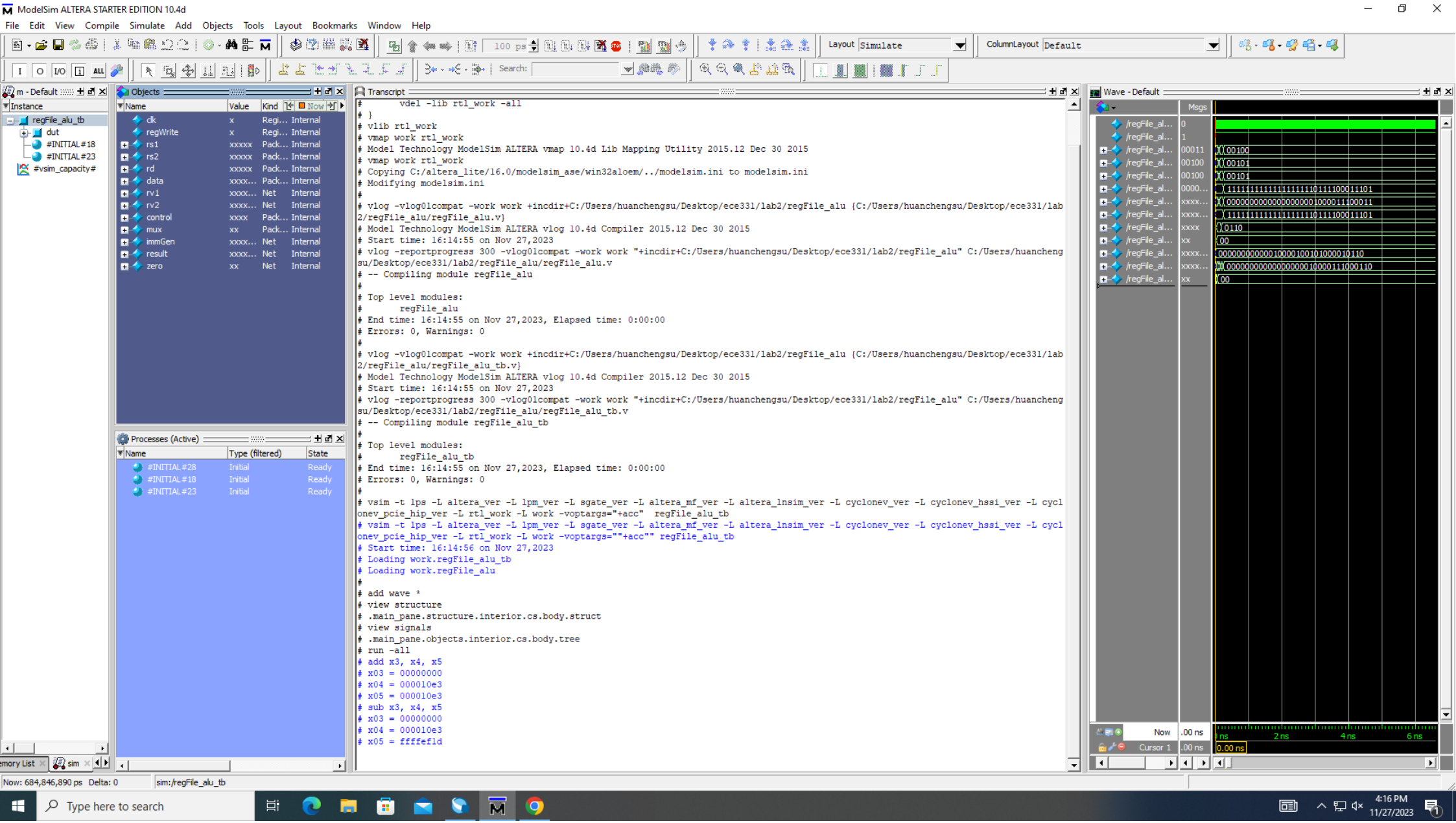

ModelSim ALTERA STARTER EDITION 10.4d
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
Objects
Name Value
clk 0
rs1 00000
rs2 00110
rd 00000
data 0000...
regWrite 1
rv1 0000...
rv2 0000...
Processes (Active)
Name Type (filtered) State
#INITIAL#17 Initial Ready
#INITIAL#12 Initial Ready
#INITIAL#17 Initial Ready
Transcript
Start time: 12:01:00 on Nov 27,2023
vlog -reportprogress 300 -vlog01compat -work work "+incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile" C:/Users/huanchengsu/Desktop/ece331/lab2/regFile/regFile.v
-- Compiling module regFile
Top level modules:
regFile
End time: 12:01:00 on Nov 27,2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vlog -vlog01compat -work work +incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile {C:/Users/huanchengsu/Desktop/ece331/lab2/regFile/regFile_tb.v}
Model Technology ModelSim ALTERA vlog 10.4d Compiler 2015.12 Dec 30 2015
Start time: 12:01:00 on Nov 27,2023
vlog -reportprogress 300 -vlog01compat -work work "+incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile" C:/Users/huanchengsu/Desktop/ece331/lab2/regFile/regFile_tb.v
-- Compiling module regFile_tb
Top level modules:
regFile_tb
End time: 12:01:00 on Nov 27,2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs="+acc" regFile_tb
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs=""+acc"" regFile_tb
Start time: 12:01:00 on Nov 27,2023
Loading work.regFile_tb
Loading work.regFile
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
********** Write data to x6 **********
regWrite = 1
rd = x06 , writeData = 00000038
x05 = 00000000
x06 = 00000038
********** Write data to x5 **********
regWrite = 1
rd = x05 , writeData = 0000001c
x05 = 0000001c
x06 = 00000038
********** Don't write data to x5 **********
regWrite = 0
rd = x05 , writeData = 00000022
x05 = 0000001c
x06 = 00000038
********** Write to 0, should not change **********
regWrite = 1
rd = x00 , writeData = 00000022
x00 = 00000000
x06 = 00000038
Wave - Default
Msgs
0
00000
00110
00000
0000...
1
0000...
0000...
00101
00000
00110
00101
00000
0000000000...
0000000000...
0000000000000000000000010...
00000...
0000000000000000000000000...
0000000000000...
0000000000000000000000000111000
.42 ns
727 ns
0.05 ns
0.1 ns
Now: 1,649,985,280 ps Delta: 1
sim:/regFile_tb
Type here to search
12:03 PM
11/27/2023


ModelSim ALTERA STARTER EDITION 10.4d
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
m - Default
Instance
alu_tb
dut
#INITIAL#18
#INITIAL#23
#vsim_capacity#
Objects
Name Value Kind Now
clk x Regi... Internal
a xxxx... Pack... Internal
b xxxx... Pack... Internal
control xxxx Pack... Internal
mux xx Pack... Internal
immGen xxxx... Net Internal
result xxxx... Net Internal
zero xx Net Internal
Processes (Active)
Name Type (filtered) State
#INITIAL#18 Initial Ready
#INITIAL#23 Initial Ready
Transcript
vsim -t lps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs="+acc" alu_tb
Start time: 15:24:17 on Nov 27,2023
Loading work.alu_tb
Loading work.alu
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
******** add ********
a = 0000000f
b = 000000f0
control = 2
result = 000000ff
******** sub ********
a = 00000034
b = 00000020
control = 6
result = 00000014
******** and ********
a = 00000f0f
b = 0000f0f0
control = 0
result = 00000000
******** or ********
a = 0000000f
b = 000ffff0
control = 1
result = 000fffff
******** beq (sub) ********
a = 0000000f
b = 0000000f
control = 6
result = 00000000
zero = 1
******** not beq (sub) ********
a = 0000032f
b = 0000000f
control = 2
mux = 1
immGen = 00084a16
result = 00084d45
zero = 0
******** lw/sw (add) ********
a = 0000000f
b = 0000000f
control = 2
mux = 1
immGen = 00084a16
result = 00084a25
zero = 0
Wave - Default
Msgs
/alu_tb/clk
/alu_tb/a
/alu_tb/b
/alu_tb/co...
/alu_tb/mux
/alu_tb/im...
/alu_tb/result
/alu_tb/zero
Now
Cursor 1
Library
sim
Now: 313,082,960 ps Delta: 0
sim:/alu_tb
Type here to search
3:24 PM
11/27/2023


ModelSim ALTERA STARTER EDITION 10.4d
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
Objects
Name Value Kind
clk x Regi... Internal
regWrite x Regi... Internal
rs1 xxxxx Pack... Internal
rs2 xxxxx Pack... Internal
rd xxxxx Pack... Internal
data xxxx... Pack... Internal
rv1 xxxx... Net Internal
rv2 xxxx... Net Internal
control xxxx Pack... Internal
mux xx Pack... Internal
immGen xxxx... Net Internal
result xxxx... Net Internal
zero xx Net Internal
Processes (Active)
Name Type (filtered) State
#INITIAL#28 Initial Ready
#INITIAL#18 Initial Ready
#INITIAL#23 Initial Ready
Transcript
vdel -lib rtl_work -all
}
vlib rtl_work
vmap work rtl_work
Model Technology ModelSim ALTERA vmap 10.4d Lib Mapping Utility 2015.12 Dec 30 2015
vmap work rtl_work
Copying C:/altera_lite/16.0/modelsim_ase/win32aloem/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
#
vlog -vlog01compat -work work +incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu {C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu/regFile_alu.v}
Model Technology ModelSim ALTERA vlog 10.4d Compiler 2015.12 Dec 30 2015
Start time: 16:14:55 on Nov 27,2023
vlog -reportprogress 300 -vlog01compat -work work "+incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu" C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu/regFile_alu.v
-- Compiling module regFile_alu
#
Top level modules:
regFile_alu
End time: 16:14:55 on Nov 27,2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
#
vlog -vlog01compat -work work +incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu {C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu/regFile_alu_tb.v}
Model Technology ModelSim ALTERA vlog 10.4d Compiler 2015.12 Dec 30 2015
Start time: 16:14:55 on Nov 27,2023
vlog -reportprogress 300 -vlog01compat -work work "+incdir+C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu" C:/Users/huanchengsu/Desktop/ece331/lab2/regFile_alu/regFile_alu_tb.v
-- Compiling module regFile_alu_tb
#
Top level modules:
regFile_alu_tb
End time: 16:14:55 on Nov 27,2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
#
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs="+acc" regFile_alu_tb
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs=""+acc"" regFile_alu_tb
Start time: 16:14:56 on Nov 27,2023
Loading work.regFile_alu_tb
Loading work.regFile_alu
#
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
add x3, x4, x5
x03 = 00000000
x04 = 000010e3
x05 = 000010e3
sub x3, x4, x5
x03 = 00000000
x04 = 000010e3
x05 = ffffef1d
Wave - Default
Msgs
Now
Cursor 1
Now: 684,846,890 ps Delta: 0
sim:/regFile_alu_tb
Type here to search
4:16 PM
11/27/2023

Lab 2 – Report

I learned a lot from this lab although it would have been much more helpful if there were instructions on how to get started or even just a statements that says to use the same environment as last lab. Getting started on the lab was the difficult part because I did not know which environment to set up but once I did things started to get easier. The other difficult part was to start the program; due to the lack of instructions it was difficult to get the initial program to begin. After Googling for a while I figured out how to figure the starting part of the program out.

After that I really enjoyed the project. Things became straight forward because I only had to look at the single-cycle processor diagram to write out the register file and the ALU. Thing lab was really helpful for learning the process and really reinforced the learning. I would like to emphasize again how much more helpful and better this lab would be for the learning if there were more instructions on the lab instruction. Overall it had been really fun and a great achievement. From this lab I actually wanted to work on more verilog. I was confused on what field I wanted to work in that applies both CompE and CompSci skills and this lab has given me a sense of direction.