ECE331

Lab 3 – Design and simulation of the CPU Controller for RISC-V Processor

Report Due: Monday 12/04/2023 – 11:59pm

a) Design and simulate the CPU Control circuit for multistage implementation of RISC-V processor with the 7 instructions discussed in class (See slide 22 of Lesson 16).

Hint 1: The controller is usually designed as an FSM (Finite State Machine) in which each state generates two set of signals: i) The control signals (outputs) required for that state (See slides 23 through 27 of Lesson 16), and ii) The state transition signals that cause the FSM move to the next expected state when the clock edge arrives.

Hint 2: This controller can be designed in one of the following two ways:

i) A 5-state (Fetch, Decode, Execute, memory, and Write-Back) Mealy machine, in which the control signals (outputs) in each stage will be a function of the state and the inputs (Instruction code + other status bits) to that stage, as required.

ii) An 11-state (Fetch, Decode, EX_beq, Ex_lw, EX_add, …, Memory, and Write-Back) Moore machine, in which the control signals (outputs) will be a function of the states only.

In both cases, the next state will be a function of both the present state and the inputs. Also, the state machine does NOT need to go through all states for all instructions and states can be skipped to run the instruction faster if not needed by the instruction.

Hint 3: You may choose either of the two approaches defined in Hint 2 to design the controller.

b) Your report should include:

1. The FSM for the controller
2. The Verilog codes (design and testbench) for the controller
3. Screen shots of the simulation of the controller for the following four instructions:

   lw x5, 12(x2)
   sw x7, 16(x22)
   sub x3, x9, x31
   beq x8, x11, L1 (L1 being the label of the fourth instruction before this beq instruction)

   showing the instruction codes and the generated control signals for each instruction

4. A short write-up of the challenges and what you learned from this lab

NOTE1: Please submit two Verilog files for the design (the module definition and the testbench) for b.2.

NOTE2: Please submit one single PDF file with all other items in b.1, b.3, and b.4.