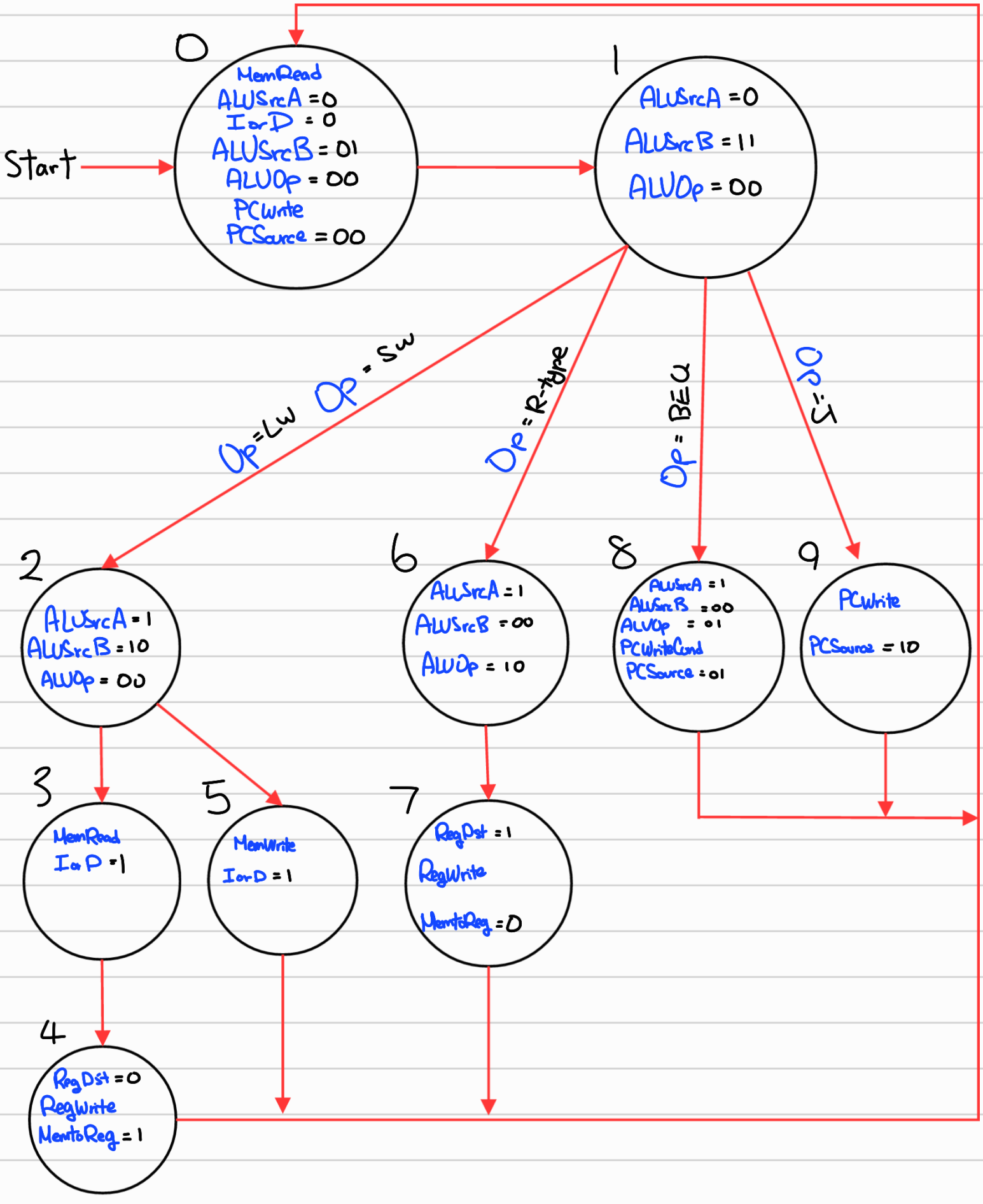
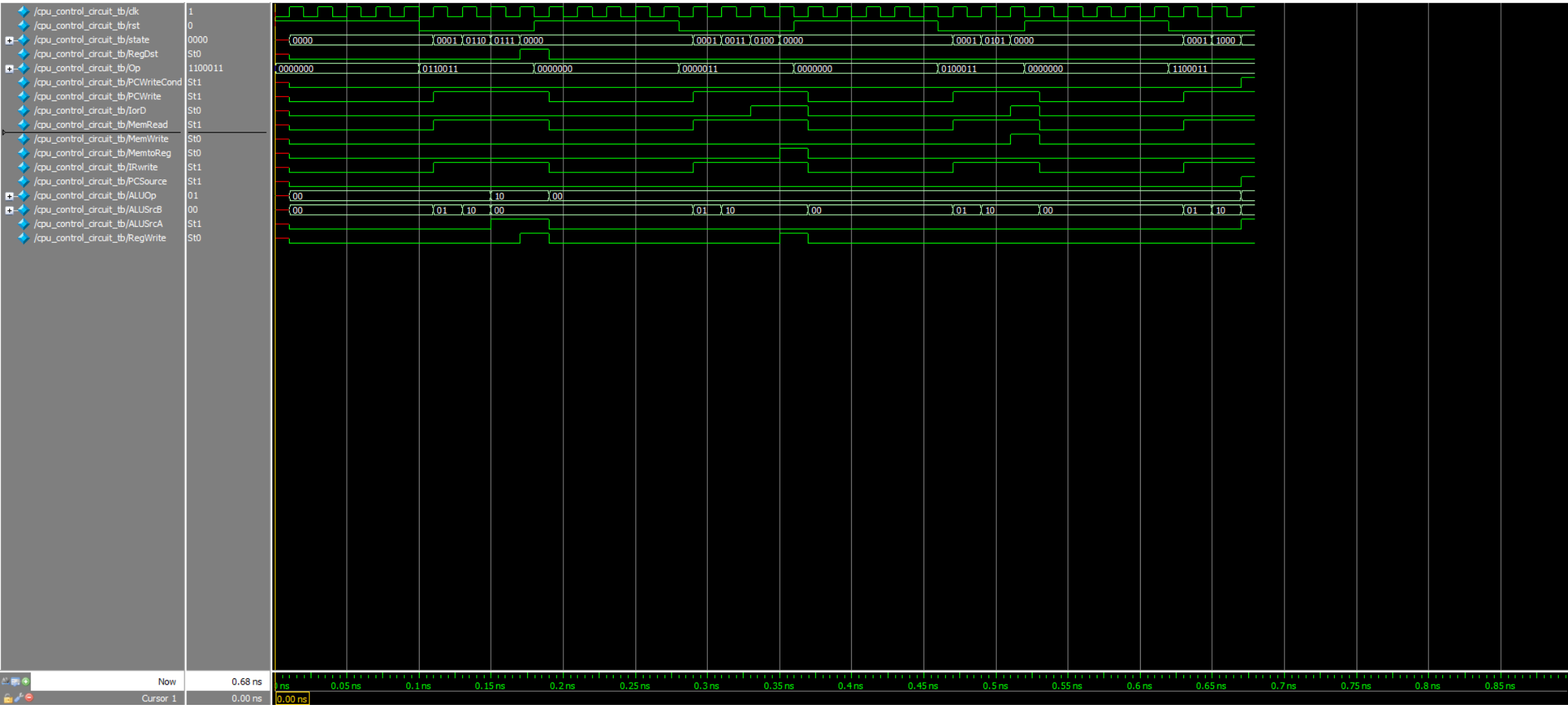

0
MemRead
ALUSrcA = 0
IorD = 0
ALUSrcB = 01
ALUOp = 00
PCWrite
PCSource = 00
Start
1
ALUSrcA = 0
ALUSrcB = 11
ALUOp = 00
OP = LW
OP = SW
OP = R-type
OP = BEQ
OP = J
2
ALUSrcA = 1
ALUSrcB = 10
ALUOp = 00
6
ALUSrcA = 1
ALUSrcB = 00
ALUOp = 10
8
ALUSrcA = 1
ALUSrcB = 00
ALUOp = 01
PCWriteCond
PCSource = 01
9
PCWrite
PCSource = 10
3
MemRead
IorD = 1
5
MemWrite
IorD = 1
7
RegDst = 1
RegWrite
MemtoReg = 0
4
RegDst = 0
RegWrite
MemtoReg = 1


/cpu_control_circuit_tb/clk
/cpu_control_circuit_tb/rst
/cpu_control_circuit_tb/state
/cpu_control_circuit_tb/RegDst
/cpu_control_circuit_tb/Op
/cpu_control_circuit_tb/PCWriteCond
/cpu_control_circuit_tb/PCWrite
/cpu_control_circuit_tb/IorD
/cpu_control_circuit_tb/MemRead
/cpu_control_circuit_tb/MemWrite
/cpu_control_circuit_tb/MemtoReg
/cpu_control_circuit_tb/IRwrite
/cpu_control_circuit_tb/PCSource
/cpu_control_circuit_tb/ALUOp
/cpu_control_circuit_tb/ALUSrcB
/cpu_control_circuit_tb/ALUSrcA
/cpu_control_circuit_tb/RegWrite
1
0
0000
St0
1100011
St1
St1
St0
St1
St0
St0
St1
St1
01
00
St1
St0
0000 0001 0110 0111 0000 0001 0011 0100 0000 0001 0101 0000 0001 1000
0000000 0110011 0000000 0000011 0000000 0100011 0000000 1100011
00 10 00
00 01 10 00 01 10 00 01 10 00 01 10
Now
0.68 ns
Cursor 1
0.00 ns
0 ns 0.05 ns 0.1 ns 0.15 ns 0.2 ns 0.25 ns 0.3 ns 0.35 ns 0.4 ns 0.45 ns 0.5 ns 0.55 ns 0.6 ns 0.65 ns 0.7 ns 0.75 ns 0.8 ns 0.85 ns
0.00 ns

Transcript

File Edit View Bookmarks Window Help

Transcript

```
# vsim -t lps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclon
ev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs=""+acc"" cpu_co
ntrol_circuit_tb
# Start time: 18:35:56 on Dec 03,2023
# Loading work.cpu_control_circuit_tb
# Loading work.cpu_control_circuit
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# sub x3, x9, x31
# Initial State:  0
# State =  1
# State =  6
# State =  7
#
# State: 0111
# State: 0111
# RegDst: 0
# PCWriteCond: 0
# PCWrite: 1
# IorD: 0
# MemRead: 1
# MemWrite: 0
# MemtoReg: 0
# IRwrite: 1
# PCSource: 0
# ALUOp: 10
# ALUSrcB: 00
# ALUSrcA: 1
# RegWrite: 0
#
# State =  0
#
# lw x5, 12(x2)
# Initial State:  0
# State =  1
# State =  3
# State =  4
#
# State: 0100
# RegDst: 0
# PCWriteCond: 0
# PCWrite: 1
# IorD: 1
# MemRead: 1
# MemWrite: 0
# MemtoReg: 0
# IRwrite: 1
# PCSource: 0
# ALUOp: 00
# ALUSrcB: 10
# ALUSrcA: 0
# RegWrite: 0
#
# State =  0
```

Transcript

File Edit View Bookmarks Window Help

Transcript

```
# PCWrite: 1
# IorD: 1
# MemRead: 1
# MemWrite: 0
# MemtoReg: 0
# IRwrite: 1
# PCSource: 0
# ALUOp: 00
# ALUSrcB: 10
# ALUSrcA: 0
# RegWrite: 0
#
# State =  0
#
# sw x7, 16(x22)
# Initial State:  0
# State =  1
# State =  5
#
# State: 0101
# RegDst: 0
# PCWriteCond: 0
# PCWrite: 1
# IorD: 0
# MemRead: 1
# MemWrite: 0
# MemtoReg: 0
# IRwrite: 1
# PCSource: 0
# ALUOp: 00
# ALUSrcB: 10
# ALUSrcA: 0
# RegWrite: 0
#
# State =  0
#
# beq x8, x11, L1
# Initial State:  0
# State =  1
# State =  8
#
# State: 1000
# RegDst: 0
# PCWriteCond: 0
# PCWrite: 1
# IorD: 0
# MemRead: 1
# MemWrite: 0
# MemtoReg: 0
# IRwrite: 1
# PCSource: 0
# ALUOp: 00
# ALUSrcB: 10
# ALUSrcA: 0
# RegWrite: 0
#
# State =  0
# ** Note: $finish    : C:/Users/huanchengsu/Desktop/ece331/lab3/cpu_control_circuit_tb.v(234)
#    Time: 680 ps  Iteration: 0  Instance: /cpu_control_circuit_tb
# 1
# Break in Module cpu_control_circuit_tb at C:/Users/huanchengsu/Desktop/ece331/lab3/cpu_control_c
ircuit_tb.v line 234
```

# Ken Su
# Lab 3 – Report

From this lab I learned that I have to open the trasncript window by myself and look carefully at the errors that it describes. For hours I was restarting project and testing different code to figure out why ModelSim was not displaying any signals. Then I found out that I have to open transcript myself. After opening transcript I noticed that it poitned towards an error on my testbench that made the dsign fail. After correcting the error the testbench worked. Then I ran in to a problem where it was only jumping between states 0 and 1. After more research I found out that since I had only set the out put as 1 bit the displays was only displaying 1 bit. After setting the state variable to 4 bits it was displaying the states properly. The last thing I had to change was my delays I noticed that I was delaying for too long so not all the states are showing, after adjusting the delays all the states were showing and the lab was working properly. Overall this was a very fun lab and I had learned alot of verilog and gained a better understanding of how the CPU control works.