# Post Lab 2

## 1. Exclusive Use of External Interrupt Pins

You can’t use both pins PA0 and PC0 for external interrupts at the same time because they are multiplexed onto EXTI0. Only one or the other can be selected at a time, which means that if one pin is used for an external interrupt, the other cannot be used for the same purpose simultaneously.

## 2. Interrupt Priority Levels

The highest software priority level is -3, which is the non-maskable interrupt (NMI). This type of interrupt has the highest precedence and cannot be masked or preempted by other interrupts. On the other hand, the lowest priority level for this specific microcontroller is indicated by level 3, which will be preempted by any other active interrupt with a higher priority.

## 3. NVIC Priority Register Bits

The NVIC has 8 bits reserved in its priority (IPR) registers for each interrupt. However, this microcontroller only implements the two most significant bits (MSB) within this register group, with all other bits (from 5:0) being non-implemented and read as zeroes. This implementation detail dictates the resolution and range of priority levels that can be assigned to the interrupts.