**Kennieth Rajesh Kakara** Majors: Electrical Engineering (ASIC design, formal Verification & Embedded systems)

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**Objective**

To attain a Summer Internship (co-op) in the field of Electrical and Electronics Engineering position as an intern, wherein I can enhance my technical skills and gain a hands on experience of the current technology and in turn grow within the company.

**Education**

* **Santa Clara University, CA** March 2017

**Master** of Science in Electrical Engineering, Expected Graduation

Related Courses: *Semi custom design, System On Chip Verification, Low Power Design, Modern Timing Analysis, Logic Design - HDL, VLSI Design 1&11, Logic Analysis synthesis, Computer Architecture, Engineering Management*

* **Mumbai University, India** June 2014

**Bachelor** of Electronics Engineering

* **Maharashtra State Board of Technical Education, India**  June 2011

**Diploma** In Industrial Electronics

**Skills and Certifications**

* Programming Languages: C, C++, MIPS Assembly Language, Matlab, Python, Tcl-tk, Verilog, System Verilog
* EDA Tools: Synopsys VCS, Formality, Conformal LEC, Cadence Virtuoso, Xilinx Vivado 15.2, Synopsys DC compiler, Spice, Eagle, Logisim, Graphical user Interface for verilog , Mentor Graphics.
* OS Worked on: Windows, Linux, Mac OS
* CPU worked with: 8086, 8085, ATMEGA16, ARM(32 and 64bits), MIPS (32bits),Pic Microcontroller
* FPGA’s worked with: Xilinx Zybo 7000, Spartan 6
* Prolific certified for PLC ladder diagram designing & SCADA software logic designing.
* Photo Shop, Corel Draw & Adobe Illustrator

**Work Experience**

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| **Santa Clara University:** Sports Marketing Intern   * Marketing the events and also ensuring the proper working of the electronic equipment involved in a sports event.   **Godrej & Boyce Fmg.Ltd, India:** Project Intern   * Performed Verification of different chip level designs * Programmed PPLCso as toimplement a system called Interlocking Of Safety & Scrap reduction, which resulted in a 20 % reduction in the number of injuries per year in the Interio department. * Developed a full fledge human machine interface (HMI) of the production line of plant-13 and also installed and programmed a completely automated messaging system for the conveyor belt stoppage time which in turn increased the production rate by 30%. | **Sai Anand Education Trust, India:** Teaching Assistant   * Adapted conceptual teaching for subjects like Logic Design, Micro controller and processor, VLSI Design and Physics. * Modeled Final year projects for undergraduate students using Verilog. * Coached an Autistic child about the basic ways of life and could considerably teach him computer basics, Adobe Illustrator, Photo Shop and Corel Draw. |

**Academic project**

* **Design of Data Route**  Language – *Verilog Environment - Synopsys VCS, Design Compiler*

Designed Data Router which can transfer multiple packets concurrently from each three input ports to single output port.

Synthesized design against lsi\_10k library making sure that it does not contain any latches, meets timing and area constraints.

Functionally simulated and verified its gate level design using testbench.

* **Design, simulation and implementation of 32-Bit MIPS Processor** *Language – Verilog Environment - Synopsys VCS, Xilinx Vivado*

Modified the architecture of a given 32- Bit MIPS Processor to support 12 instructions, which includes arithmetic, logical, branch, and jump instructions using Verilog in Synopsys VCS.

Added three pipeline stages so as to improve latency and throughput. Simulated the design and verified functional correctness of imple mented instructions. Optimized and mapped design for smaller area, meeting the timing constraints onto FPGA using Xilinx Vivado.

* **Analysis and Evaluation of Assertion & Equivalence Formal Verification** Environment*:*

*Cadence Conformal LEC & Synopsys Formality*

Researched and studied the methodologies of Assertion and Equivalence based Formal Verification.

Formally verified equivalence of RTL codes of 7-segment display, 16x16 internet switch and Bluetooth Module on two Verification tool.

* **Xilinx Zybo 7000 FPGA :** Interfacing an analog accelerometer to the Zybo through the PMOD ports. Using the data received the system could control, detect, store or monitor any changes which included acceleration in all axis.
* **Hand Gesture based Multiple Control System**: Using ATMEGA 16 Automated a Wheel Chair to move around, decoded hand gestures of profoundly deafthen displayed it on an LCD display and wirelessly operated the home switches using ZigBee .
* **Circuit Optimization**: Reduction in the time delay of the circuit by optimizing the position of the output node with the help Elermore’s time constant calculation and realizing the same in Spice Schematic software.
* **Electronic Car Dashboard**: With micro controller 8051 we automated car temperature control, head light on and off, tyer pressure control and even tried to change the rear view mirror angle by taking the back road and the retina of the driver as a reference.
* **Micro processor based Electronic Code Locking System:** An alpha numeric system lock which could be installed into an electronic system, the main feature of it was it could generate one time passwords and also have different passcodes with different accessibility levels.