CMPE110 Lecture 26
Final Exam Review

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https://canvas.ucsc.edu/courses/12652

Announcements

- Final Exam
  - Next Tuesday June 12th
  - 3 hours from 12-3pm
  - Location: Here, Baskin Auditorium

General Tips for the Exam

- Read the questions carefully
  - Especially if you have seen the question before, it is likely that its not an identical copy but that some numbers have changed
  - There might be small twist to what you are used to e.g. 5-stage vs. 6-stage pipeline
  - Get a precise understanding of what is asked, e.g. dependencies vs. hazards

General Tips for the Exam

- Manage your time well
  - Move on when you struggle with a question
- Consider 3 pass system
  - First hour for the easy half of the exam
  - 1.5 hours for the difficult questions
  - Last half hour, double check your answers

Can you answer the following questions?

- What is the task of each of the 5 pipe stages?
- Can you reason about dependencies for arbitrary long pipelines?
- Number of NOPs in presence of dependencies?
- Forwarding paths?
- What are tag, index, byte offset in a cache?
- Can you compute the three for arbitrary architectures? e.g. fully associative, 32K entries, 4 byte cache lines?

Can you answer the following questions?

- Why do we use hierarchical PTs?
- Can you compute the size of a PT given pages, present, mapped bits?
- How do you traverse a multi-level PT?
- Can you translate the following C into RISC-V?

  -
    ```
    switch(a) {
      case 0: b++;
      case 1: b--;
      }
    ```
- Why no WAW/WAR for in-order pipelines?

Piazza Questions

- Branch prediction with 1 vs. 2 bit BHT

branch stall CPI

- 8.) Assume a processor where all instructions have a CPI of 1 except branches which introduce a 1 cycle bubble (control point is the instruction decode stage). Assume a branch strategy of Predict Not Taken, a branch frequency of 20% (% of instructions) and that 50% of all branches are taken. What is the branch stall CPI?
  - 0.1
  - 0.2
  - 0.25
  - 0.5

WAR/WAW

- 'in-order, scalar, pipelined processor where all instructions require the same number of pipelined stages' are subject to RAW hazards.
- What would be subject to WAW and WAR hazards in these respects?

OOO vs. in-order

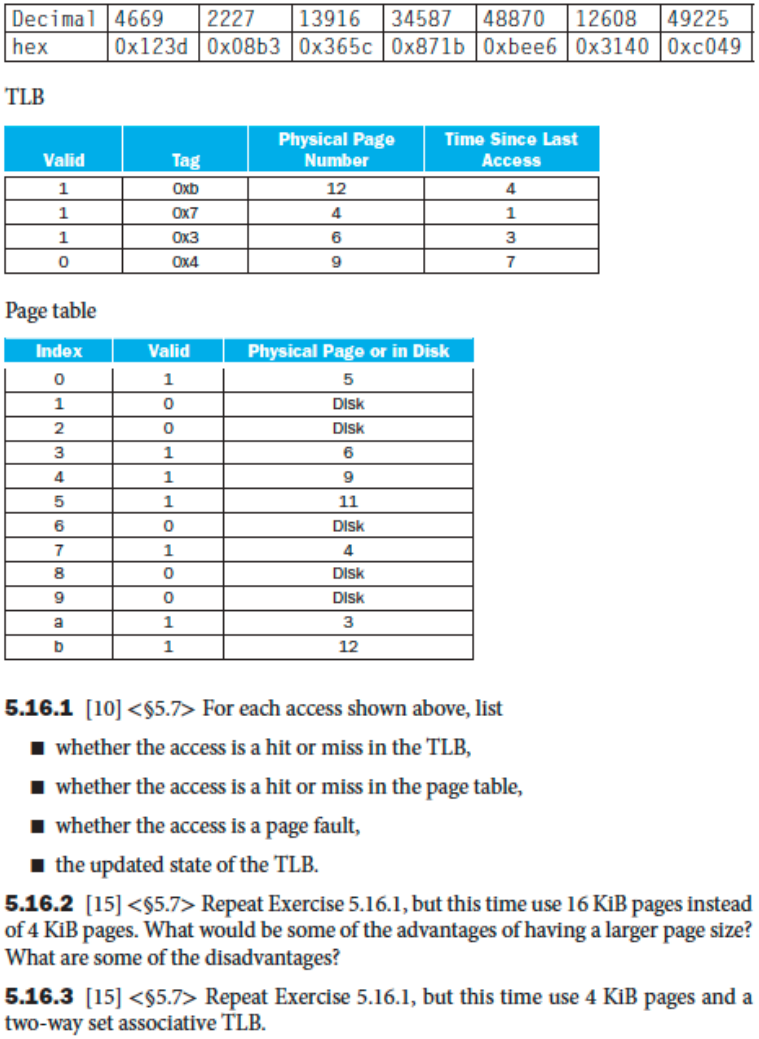
- 10.) Assume the following instruction sequence executed on an out-of-order processor that supports register renaming (32 additional physical registers). What is the maximum number of instructions that can be executed in parallel during a single clock cycle?
  - Add x1, x1, x2
  - Sub x1, x3, x4
  - Mul x3, x1, x5
  - Div x5, x5, x4

What is the effect of RR?

What can we reorder?

Which dependencies always serialize even in OOO?

VM



Decimal	4669	2227	13916	34587	48870	12608	49225
hex	0x123d	0x08b3	0x365c	0x871b	0xbee6	0x3140	0xc049

TLB

Valid	Tag	Physical Page Number	Time Since Last Access
1	0xb	12	4
1	0x7	4	1
1	0x3	6	3
0	0x4	9	7

Page table

Index	Valid	Physical Page or in Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
a	1	3
b	1	12

5.16.1 [10] <§5.7> For each access shown above, list

- whether the access is a hit or miss in the TLB,
- whether the access is a hit or miss in the page table,
- whether the access is a page fault,
- the updated state of the TLB.

5.16.2 [15] <§5.7> Repeat Exercise 5.16.1, but this time use 16 KiB pages instead of 4 KiB pages. What would be some of the advantages of having a larger page size? What are some of the disadvantages?

5.16.3 [15] <§5.7> Repeat Exercise 5.16.1, but this time use 4 KiB pages and a two-way set associative TLB.