

Basic RISC CPU Verification

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ECE 4435: Computer Architecture and Design

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Add Test

1. Program loads 0x00000040 into R1 using la instruction
2. Program loads 0x00000020 into R2 using la instruction
3. Program adds the contents of R1 and R2 and stores the result in R3
4. Program stores the R3 contents into memory and loads it back into R4
5. At the end of the program, PC = 0x00000018 and IR = 0xF8000000

Add Test: Simulator

Register Contents

- PC = 0x00000018
- IR = 0xF8000000
- R1 = 0x00000040
- R2 = 0x00000020
- R3 = 0x00000060
- R4 = 0x00000060
- R5-R31 = 0x00000000

PC = 00000018

r0 = 00000000	r1 = 00000040	r2 = 00000020	r3 = 00000060
r4 = 00000060	r5 = 00000000	r6 = 00000000	r7 = 00000000
r8 = 00000000	r9 = 00000000	r10 = 00000000	r11 = 00000000
r12 = 00000000	r13 = 00000000	r14 = 00000000	r15 = 00000000
r16 = 00000000	r17 = 00000000	r18 = 00000000	r19 = 00000000
r20 = 00000000	r21 = 00000000	r22 = 00000000	r23 = 00000000
r24 = 00000000	r25 = 00000000	r26 = 00000000	r27 = 00000000
r28 = 00000000	r29 = 00000000	r30 = 00000000	r31 = 00000000

Exit Print Load Reload Edit Step Run Stop

Clear RegFile Clear BreakPts Clear Memory Clear Console

Time Model Editor Timing Statistics

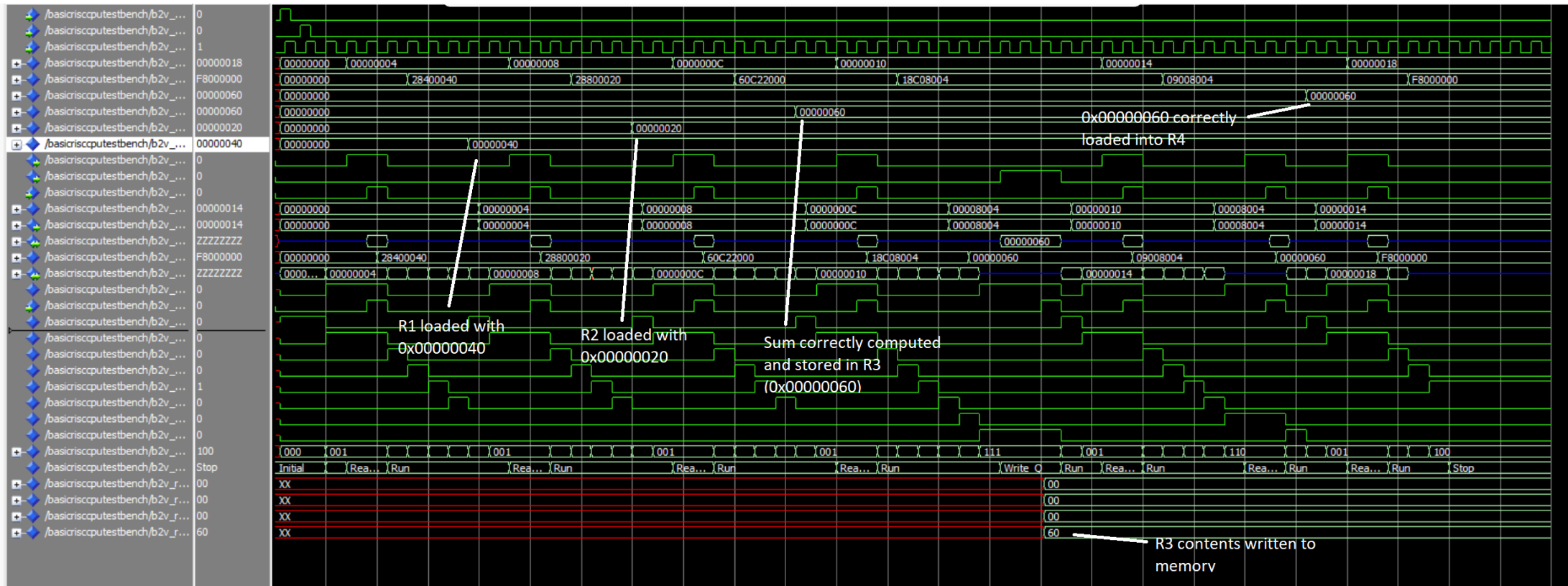
Hex Dec ☒ Update Screen ☐ Allow Exceptions

Loc	BreakPt	MachWord	Source Code	
[00000010]	<input type="checkbox"/>	09008004	ld r4, 32772(r0)	Prev. 8
[00000014]	<input type="checkbox"/>	f8000000	stop	Prev. 4
[00000018]	<input type="checkbox"/>	00000000	nop	Prev. 1
[0000001c]	<input type="checkbox"/>	00000000	nop	Next 1
[00000020]	<input type="checkbox"/>	00000000	nop	Next 4
[00000024]	<input type="checkbox"/>	00000000	nop	Next 8
[00000028]	<input type="checkbox"/>	00000000	nop	
[0000002c]	<input type="checkbox"/>	00000000	nop	

Loc	Offset 00	Offset 04	Offset 08	Offset 0c	
[00000000]	28400040	28800020	60c22000	18c08004	Prev. 16
[00000010]	09008004	f8000000	00000000	00000000	Prev. 8
[00000020]	00000000	00000000	00000000	00000000	Prev. 4
[00000030]	00000000	00000000	00000000	00000000	Next 4
					Next 8
					Next 16

(SRCTools Version 3.1.1)

Add Test: Modelsim



Register Contents

PC = 0x00000018 R1 = 0x00000040 R2 = 0x00000020 R3 = 0x00000060 R4 = 0x00000060
IR = 0xF8000000 R5-R31 = 0x0000000-0

ALU Tests

1. Program uses a variety of arithmetic ALU operations (add, addi, or, ori, sub, neg, and) to populate R1-R11, R15, and R27 (using their register number)
2. Registers R16 through R23 were populated with strings to test the shift and bit manipulation operations (not, shr, shra, shl, shc)
3. Registers R24 through R31 were filled with their register number
4. At the end of the program, PC = 0x000010A8 and IR = 0xF8000000

ALU Tests: Simulator

Register contents

- PC = 0x000010A8
- IR = 0xF8000000
- R0-R15 = 0x00000000-0x0000000F (0 through 15)
- R16 = 0xFFFFFFFF
- R17 = 0x7FFFFFFF
- R18 = 0x7FFFFFFE
- R19 = 0xFFFE7FFF
- R20 = 0xF0000000
- R21 = 0x000000F0
- R22 = 0xFFFFFFFF
- R23 = 0xFFFFFFFF
- R24-R31 = 0x00000018-0x0000001F (24 through 31)

PC = 000010a8

r0 = 00000000	r1 = 00000001	r2 = 00000002	r3 = 00000003
r4 = 00000004	r5 = 00000005	r6 = 00000006	r7 = 00000007
r8 = 00000008	r9 = 00000009	r10 = 0000000a	r11 = 0000000b
r12 = 0000000c	r13 = 0000000d	r14 = 0000000e	r15 = 0000000f
r16 = ffffffff	r17 = 7fffffff	r18 = 7ffffffe	r19 = fffe7fff
r20 = f0000000	r21 = 000000f0	r22 = ffffffff	r23 = ffffffff
r24 = 00000018	r25 = 00000019	r26 = 0000001a	r27 = 0000001b
r28 = 0000001c	r29 = 0000001d	r30 = 0000001e	r31 = 0000001f

Exit Print Load Reload Edit Step Run Stop

Clear RegFile Clear BreakPts Clear Memory Clear Console

Time Model Editor Timing Statistics

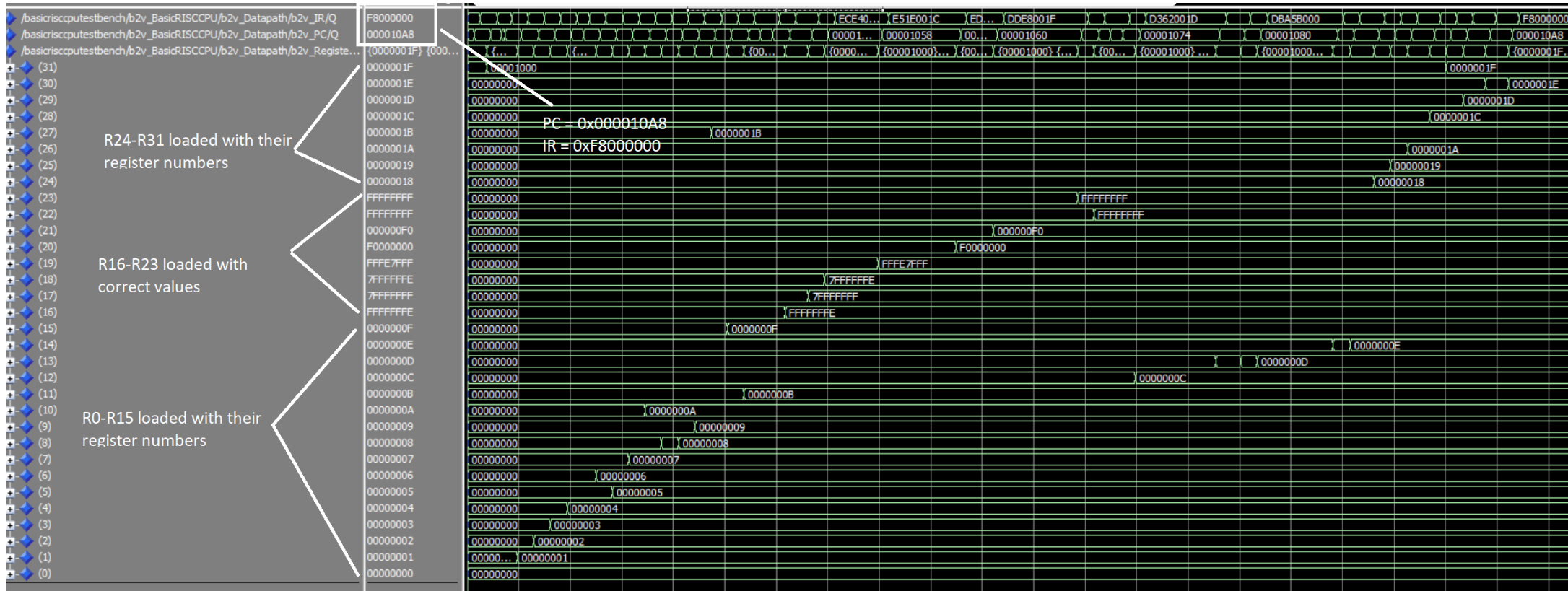
☒ Hex ☐ Dec ☒ Update Screen ☐ Allow Exceptions

Loc	BreakPt	MachWord	Source Code	
[000010a0]	<input type="checkbox"/>	e7bc0001	shl r30, r30, 1	Prev. 8
[000010a4]	<input type="checkbox"/>	f8000000	stop	Prev. 4
[000010a8]	<input type="checkbox"/>	00000000	nop	Prev. 1
[000010ac]	<input type="checkbox"/>	00000000	nop	Next 1
[000010b0]	<input type="checkbox"/>	00000000	nop	Next 4
[000010b4]	<input type="checkbox"/>	00000000	nop	Next 8
[000010b8]	<input type="checkbox"/>	00000000	nop	
[000010bc]	<input type="checkbox"/>	00000000	nop	

Loc	Offset 00	Offset 04	Offset 08	Offset 0c	
[00000000]	2fc01000	403e0001	00000000	00000000	Prev. 16
[00000010]	00000000	00000000	00000000	00000000	Prev. 8
[00000020]	00000000	00000000	00000000	00000000	Prev. 4
[00000030]	00000000	00000000	00000000	00000000	Next 4
					Next 8
					Next 16

(SRCTools Version 3.1.1)

ALU Tests: Modelsim



Register Contents

PC = 0x000010A8 IR = 0xF8000000 R0-R15 = 0x00000000-0x0000000F R16 = 0xFFFFFFFF
 R17 = 0x7FFFFFFF R18 = 0x7FFFFFFE R19 = 0xFFFE7FFF R20 = 0xF0000000 R21 = 0x000000F0
 R22 = 0xFFFFFFFF R23 = 0xFFFFFFFF R24-R31 = 0x00000018-0x0000001F

Branch Tests

1. First, 4096 is loaded into R31 and 11 various addresses are loaded into R1-R11 using la to act as jump locations
2. R20 is loaded with the address of “Stop”
3. Various loops are used to test the different branch instructions (br, brzr, brnv, brmi, brpl, brlzs, brl, brlnv, brlnz, brlmi)
 1. R31 loop counts from 5-0 then breaks
 2. R30 loop counts from 7 to -1
 3. R29 loop counts from -6 to 0
 4. R24 loop counts from 5-0 then up to 1
 5. R28 loop counts from 1 to 0 to -1 then breaks

Branch Tests: Simulator

Register Contents

- PC = 4332
- IR = 0xF8000000
- R0 = 0, R1 = 4160, R2 = 4176, R3 = 4188
- R4 = 4200, R5 = 4212, R6 = 4224, R7 = 4244
- R8 = 4280, R9 = 4292, R10 = 4304, R11 = 4316
- R12 = 4252, R13 = 4256, R14 = 4264, R15 = 4268
- R16 = 4272, R17-R19 = 0, R20 = 4328, R21-R23 = 0
- R24 = 1, R25-R27 = 0, R28 = -1, R29-R31 = 0

PC = 4332

r0 = 0	r1 = 4160	r2 = 4176	r3 = 4188
r4 = 4200	r5 = 4212	r6 = 4224	r7 = 4244
r8 = 4280	r9 = 4292	r10 = 4304	r11 = 4316
r12 = 4252	r13 = 4256	r14 = 4264	r15 = 4268
r16 = 4272	r17 = 0	r18 = 0	r19 = 0
r20 = 4328	r21 = 0	r22 = 0	r23 = 0
r24 = 1	r25 = 0	r26 = 0	r27 = 0
r28 = -1	r29 = 0	r30 = 0	r31 = 0

Exit Print Load Reload Edit Step Run Stop

Clear RegFile Clear BreakPts Clear Memory Clear Console

Time Model Editor Timing Statistics

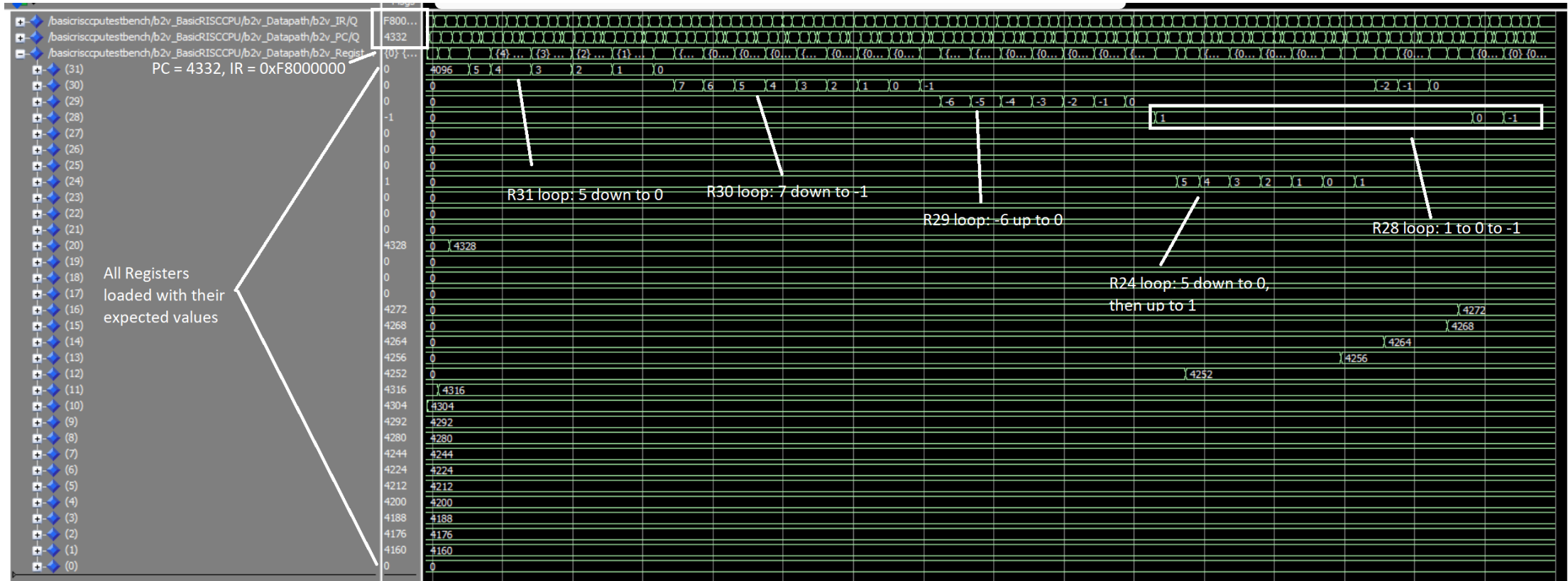
☐ Hex ☒ Dec ☒ Update Screen ☐ Allow Exceptions

Loc	BreakPt	MachWord	Source Code	
[4324]	<input type="checkbox"/>	40160001	br r11	Prev. 8
[4328]	<input type="checkbox"/>	f8000000	stop	Prev. 4
[4332]	<input type="checkbox"/>	00000000	nop	Prev. 1
[4336]	<input type="checkbox"/>	00000000	nop	Next 1
[4340]	<input type="checkbox"/>	00000000	nop	Next 4
[4344]	<input type="checkbox"/>	00000000	nop	Next 8
[4348]	<input type="checkbox"/>	00000000	nop	
[4352]	<input type="checkbox"/>	00000000	nop	

Loc	Offset 00	Offset 04	Offset 08	Offset 0c	
[0]	801116160	1077805057	0	0	Prev. 16
[16]	0	0	0	0	Prev. 8
[32]	0	0	0	0	Prev. 4
[48]	0	0	0	0	Next 4
					Next 8
					Next 16

(SRCTools Version 3.1.1)

Branch Tests: Modelsim



Register Contents

- PC = 4332, IR = 0xF8000000
- R0 = 0, R1 = 4160, R2 = 4176, R3 = 4188, R4 = 4200, R5 = 4212, R6 = 4224, R7 = 4244
- R8 = 4280, R9 = 4292, R10 = 4304, R11 = 4316, R12 = 4252, R13 = 4256, R14 = 4264, R15 = 4268
- R16 = 4272, R17-R19 = 0, R20 = 4328, R21-R23 = 0, R24 = 1, R25-R27 = 0, R28 = -1, R29-R31 = 0

Load-Store Tests

- First, R0 is loaded with the constant 0x8000 (32768)
- Using the lar, str, ldr, st, ld, and la operations, each of the registers R1 through R31 are loaded with values representing their row numbers
- Ex: Registers R1-R3 are in row 1, R4-R7 are in row 2, R8-R11 are in row 3, etc
- At the end of the program, PC = 4252 and IR = 0xF8000000

Load-Store Tests: Simulator

Register Contents

- PC = 4252
- IR = 0xF8000000
- R0 = 32768
- R1-R3 = 1
- R4-R7 = 2
- R8-R11 = 3
- R12-R15 = 4
- R16-R19 = 5
- R20-R23 = 6
- R24-R27 = 7
- R28-R31 = 8

PC = 4252			
r0 = 32768	r1 = 1	r2 = 1	r3 = 1
r4 = 2	r5 = 2	r6 = 2	r7 = 2
r8 = 3	r9 = 3	r10 = 3	r11 = 3
r12 = 4	r13 = 4	r14 = 4	r15 = 4
r16 = 5	r17 = 5	r18 = 5	r19 = 5
r20 = 6	r21 = 6	r22 = 6	r23 = 6
r24 = 7	r25 = 7	r26 = 7	r27 = 7
r28 = 8	r29 = 8	r30 = 8	r31 = 8

Exit	Print	Load	Reload	Edit	Step	Run	Stop
Clear RegFile		Clear BreakPts		Clear Memory		Clear Console	
Time Model Editor				Timing Statistics			

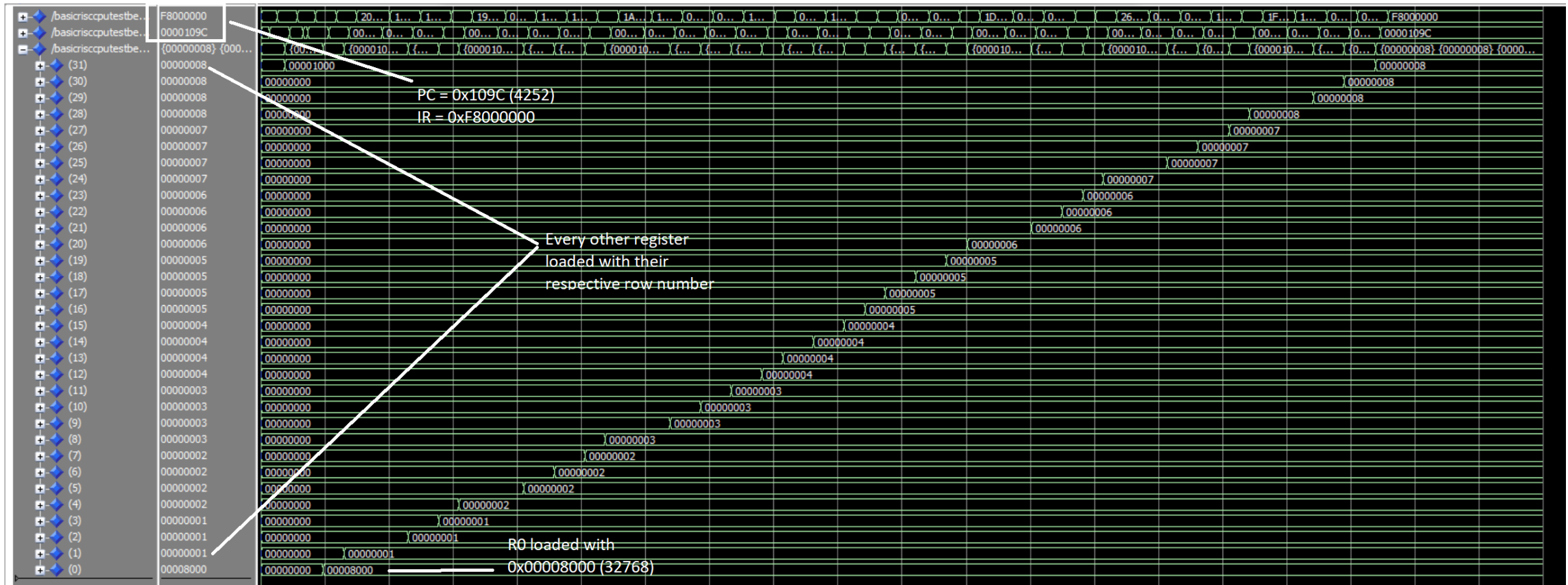
☐ Hex ☒ Dec ☒ Update Screen ☐ Allow Exceptions

Loc	BreakPt	MachWord	Source Code	
[4244]	<input type="checkbox"/>	0ffc8034	ld r31, 32820(r30)	Prev. 8
[4248]	<input type="checkbox"/>	f8000000	stop	Prev. 4
[4252]	<input type="checkbox"/>	00000000	nop	Prev. 1
[4256]	<input type="checkbox"/>	00000000	nop	Next 1
[4260]	<input type="checkbox"/>	00000000	nop	Next 4
[4264]	<input type="checkbox"/>	00000000	nop	Next 8
[4268]	<input type="checkbox"/>	00000000	nop	
[4272]	<input type="checkbox"/>	00000000	nop	

Loc	Offset 00	Offset 04	Offset 08	Offset 0c	
[0]	801116160	1077805057	0	0	Prev. 16
[16]	0	0	0	0	Prev. 8
[32]	0	0	0	0	Prev. 4
[48]	0	0	0	0	Next 4
					Next 8
					Next 16

(SRCTools Version 3.1.1)

Load-Store Tests: Modelsim



Register Contents

- PC = 4252 (0x0000109C), IR = 0xF8000000, R0 = 32768 (0x00008000), R1-R3 = 1
- R4-R7 = 2, R8-R11 = 3, R12-R15 = 4, R16-R19 = 5, R20-R23 = 6, R24-R27 = 7, R28-R31 = 8

Conclusion

- Collectively, all 4 of the assembly programs test all of the CPU instructions
- Every Modelsim simulation matches the results produced by the assembly simulator
- Thus, we can confidently say that the Basic RISC CPU that we have designed works as intended