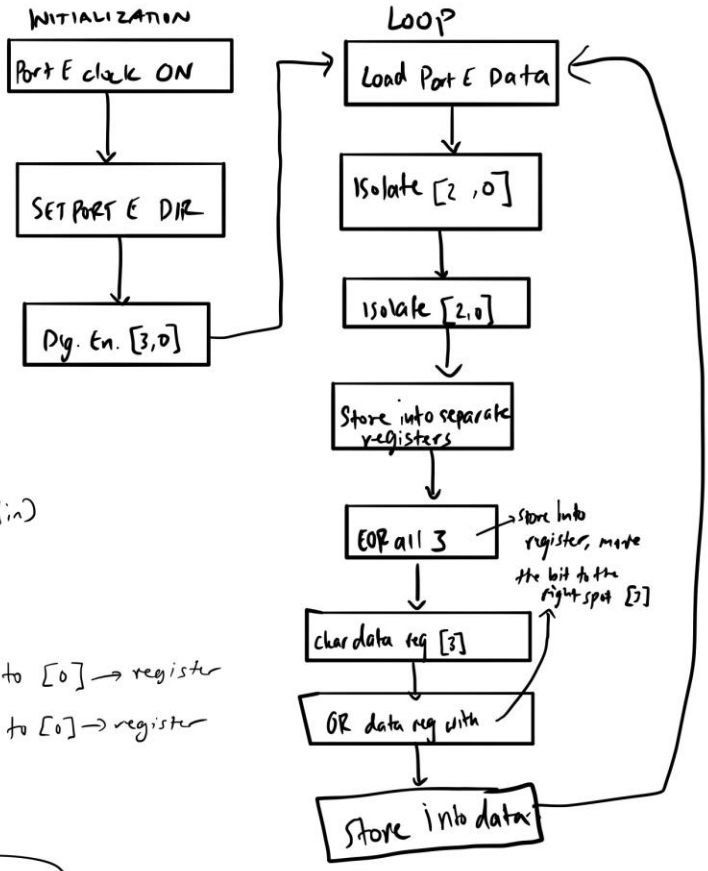
Lab 1

Flow chart:



Pseudocode

Turn on Port E clock

Modify DIR Reg (PE[3] out PE[2,0] in)

Digital enable Port E [3,0]

loop Load Port E data

Isolate PE [2] and move to [0] → register

Isolate PE [1] and move to [0] → register

Isolate PE [0] → register

EOR ALL 3
store into register

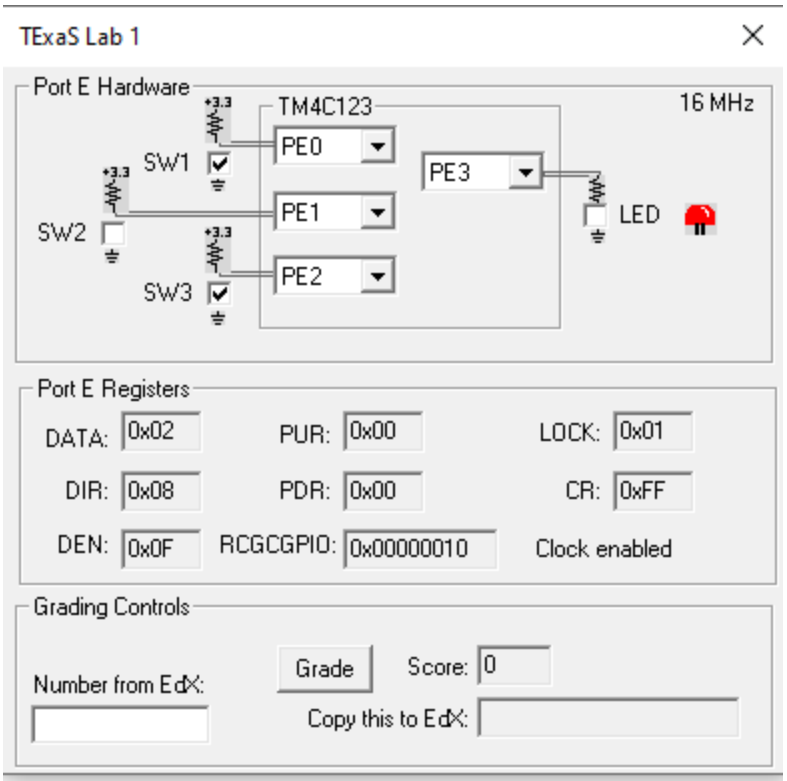
Clear data register [3]

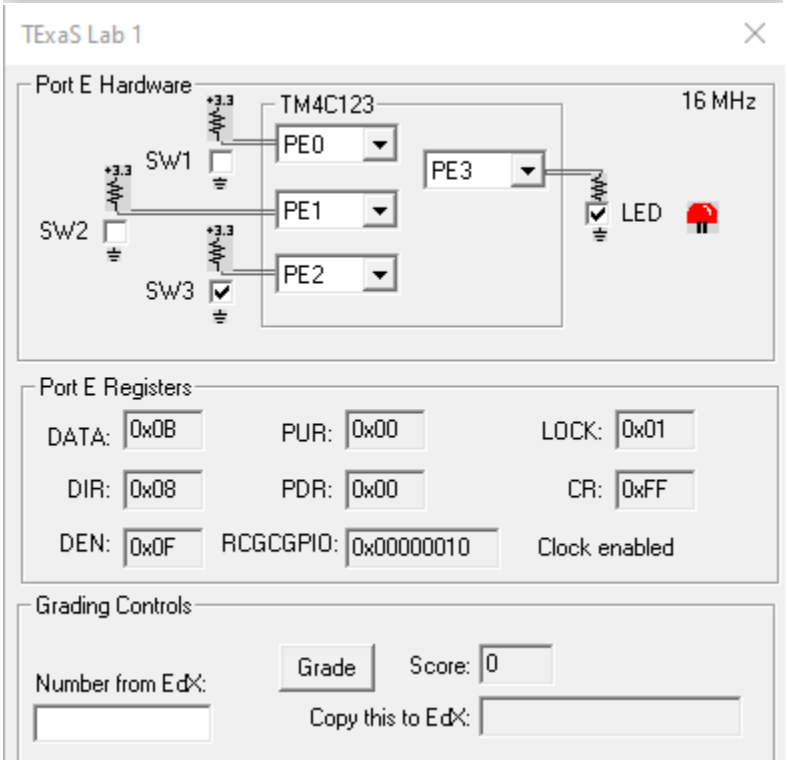
OR data register w/

B loop

LAB 1 MAIN.S SOURCE PROGRAM

```
;****************** main.s ***************
GPIO_PORTE_DATA_R  EQU 0x400243FC
GPIO_PORTE_DIR_R   EQU 0x40024400
GPIO_PORTE_DEN_R   EQU 0x4002451C
SYSCTL_RCGCGPIO_R  EQU 0x400FE608

      THUMB
      AREA    DATA, ALIGN=2
;global variables go here
     ALIGN
     AREA    |.text|, CODE, READONLY, ALIGN=2
     EXPORT  Start
Start
   ;code to run once that initializes PE3,PE2,PE1,PE0

                ;turn on clock of port E
                LDR          R0,          = SYSCTL_RCGCGPIO_R
                LDRB         R1, [R0]
                ORR          R1, #0x10
                STRB         R1, [R0]
                NOP
                NOP
                ;set direction of the needed ports
                LDR          R0, = GPIO_PORTE_DIR_R
                LDRB R1, [R0]
                AND R1, #0xF8
                ORR          R1, #0x08
                STRB R1, [R0]

                ;digital enable all pins
                LDR          R0, = GPIO_PORTE_DEN_R
                LDRB R1, [R0]
                ORR          R1, #0x0F
                STRB R1, [R0]

loop
   ;code that runs over and over
                ;read the data register B [2,0] and put each of its bits into a separate register
                ; R2=portE [0]
                ; R3=portE [1]
                ; R4=port# [2]
                LDR R0, = GPIO_PORTE_DATA_R
                LDR R1, [R0]
                AND R2, R1, #0x01
                AND R3, R1, #0x02
                LSR R3, R3, #1
                AND R4, R1, #0x04
                LSR R4, R4, #2

                ;EOR operation of each bit
                EOR R5, R2, R3
                EOR R5, R4, R5
                EOR R5, #1
                LSL R5, #3

                ;clear PortE data [3] and store modified register
                AND R1, #0xF7
                ORR R1, R1, R5
                STR R1, [R0]

   B    loop
     ALIGN       ; make sure the end of this section is aligned
     END         ; end of file
```


TExaS Lab 1
Port E Hardware
TM4C123
16 MHz
SW1
SW2
SW3
PE0
PE1
PE2
PE3
LED
Port E Registers
DATA: 0x02
PUR: 0x00
LOCK: 0x01
DIR: 0x08
PDR: 0x00
CR: 0xFF
DEN: 0x0F
RCGCGPIO: 0x00000010
Clock enabled
Grading Controls
Number from EdX:
Grade
Score: 0
Copy this to EdX:


TExaS Lab 1
Port E Hardware
TM4C123
16 MHz
SW1
SW2
SW3
PE0
PE1
PE2
PE3
LED
Port E Registers
DATA: 0x0B
PUR: 0x00
LOCK: 0x01
DIR: 0x08
PDR: 0x00
CR: 0xFF
DEN: 0x0F
RCGCGPIO: 0x00000010
Clock enabled
Grading Controls
Number from EdX:
Grade
Score: 0
Copy this to EdX: