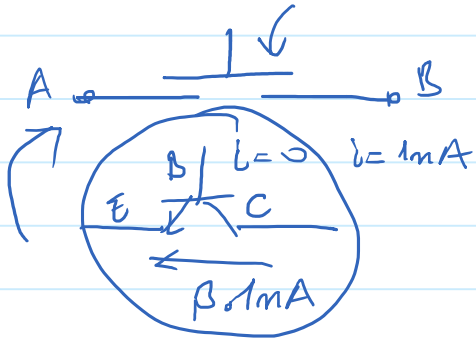
Reading

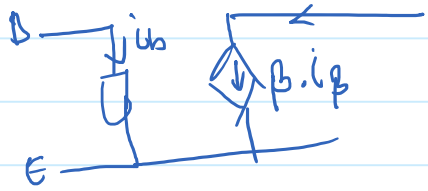
MOSFET

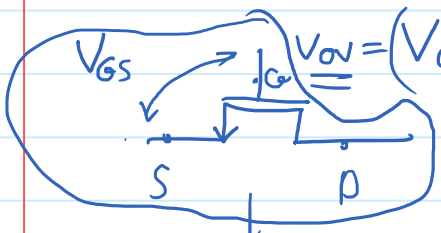
Adel S. Sedra and Kenneth C. Smith, **Microelectronic Circuits** 7th Edition, *Oxford University Press*, 2014.

- Chapter 5.1,5.3

Recap



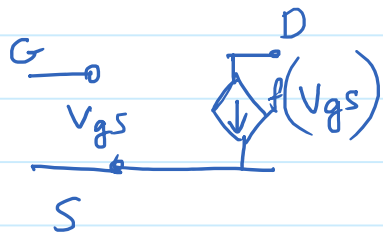


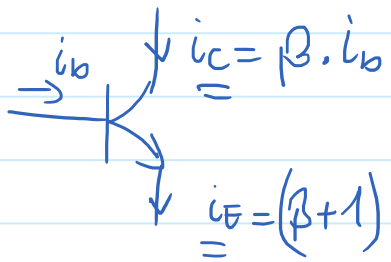


$V_{OV} = (V_{GS} - V_T) \Rightarrow V_{GS} \geq V_T$

$V_{OV} = 2.5$

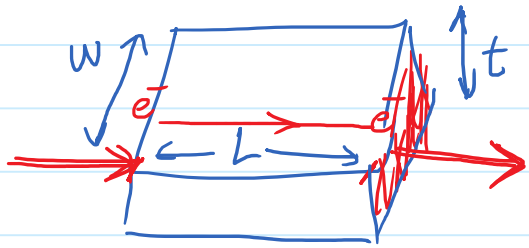
$V_{OV} = -2.5$





$i_C = \left(\frac{\beta}{\beta+1}\right) i_E$ (α)

Resistor



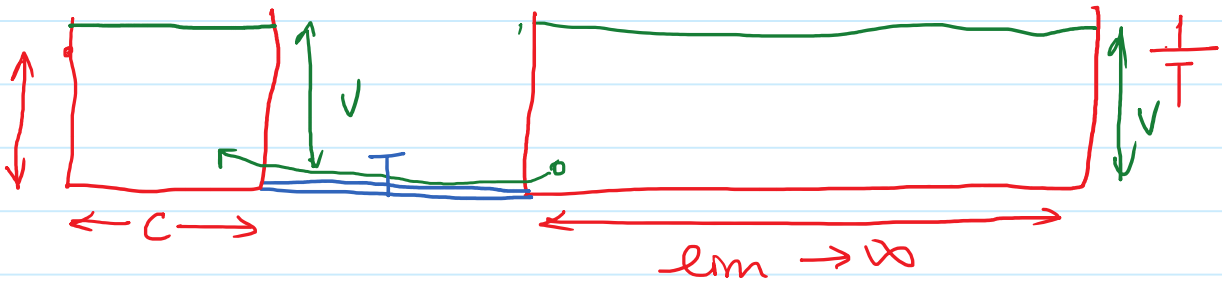
$$R = \frac{\rho \cdot L}{A}$$

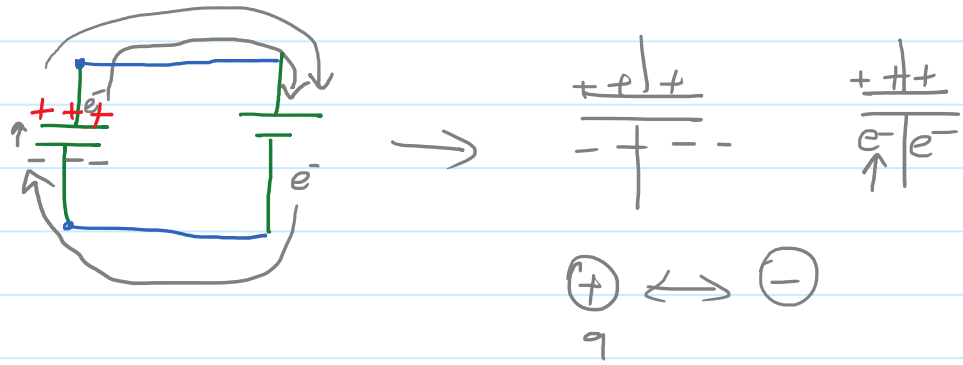
$$R = \frac{\rho \cdot L}{W \cdot t} = \left(\frac{\rho}{t}\right) \cdot \frac{L}{W}$$

ρ

$$\text{(I)}\ R = V \Rightarrow I_{DS} = \frac{V}{R} = \frac{V_{DS}}{\rho \frac{L}{W}}$$

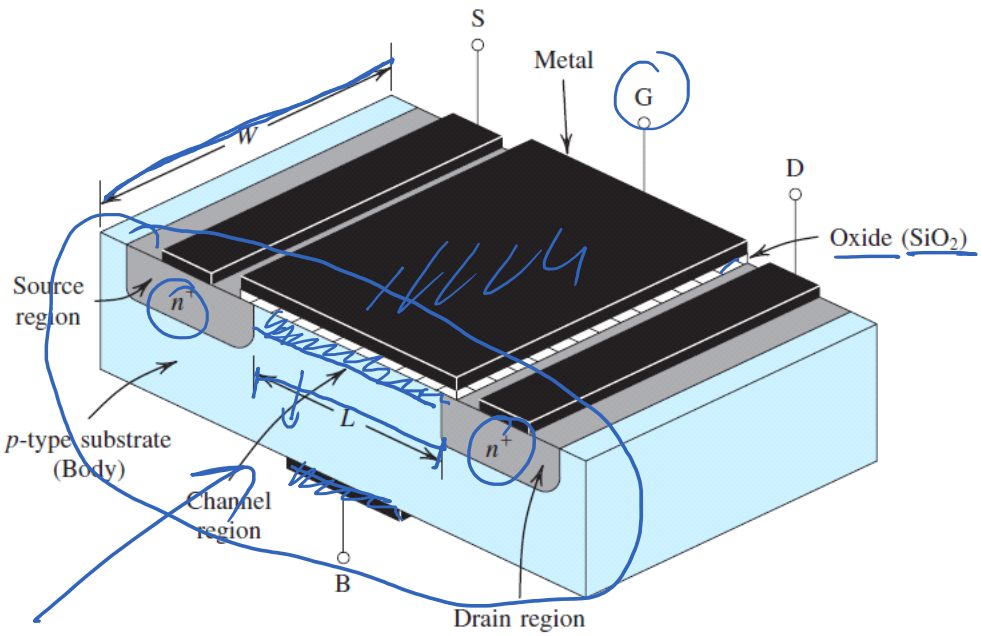
Capacitor

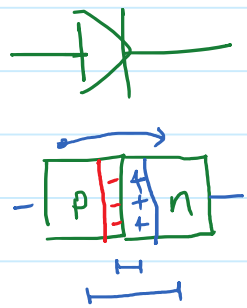


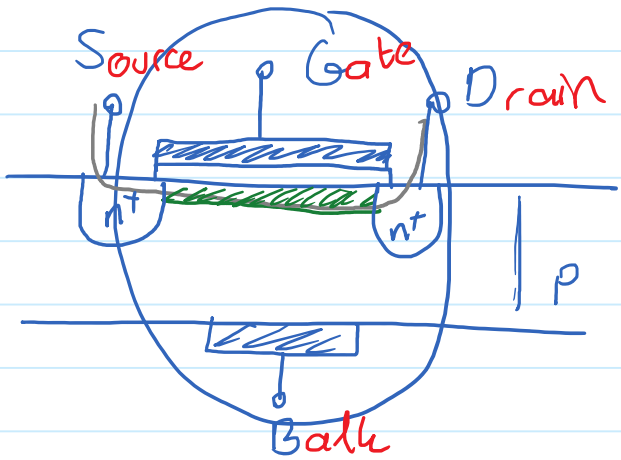


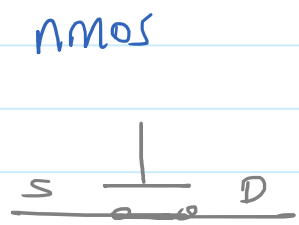
n-Channel MOSFET Structure

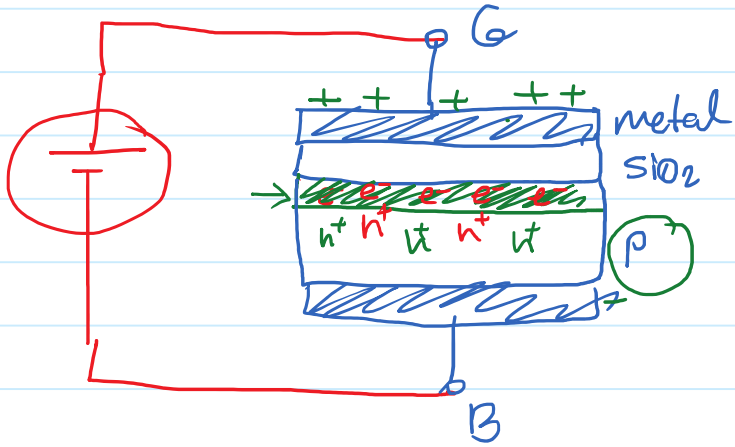
nmos
pmos

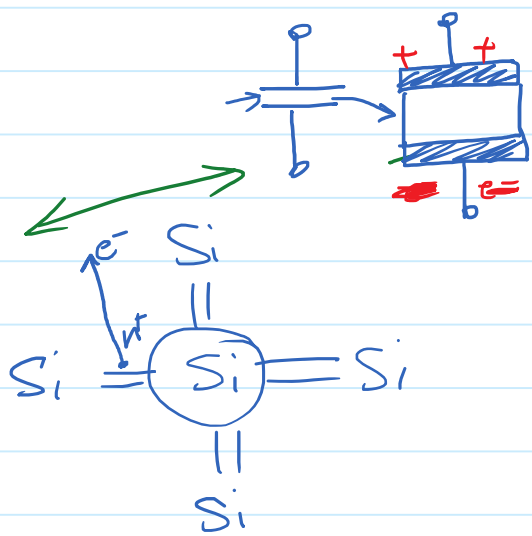




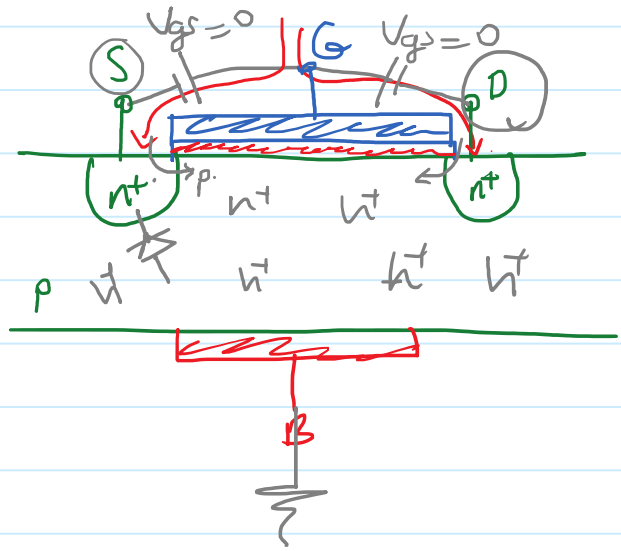








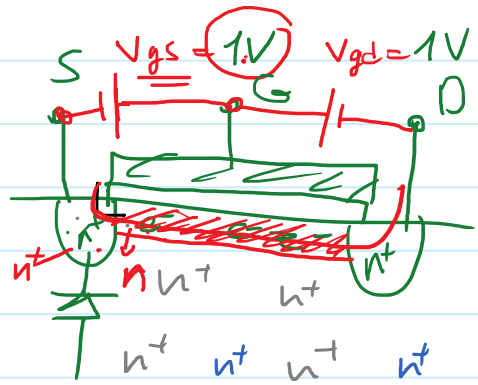
Zero Gate Voltage



$I_{DS} = 0$

$I_G = 0$

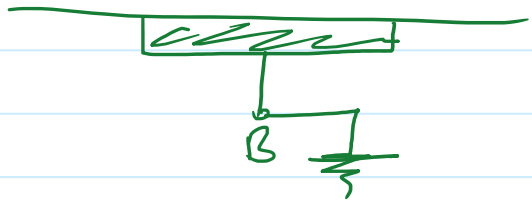
Channel Formation

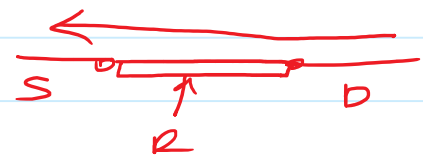


$n^+ > e^-$ p

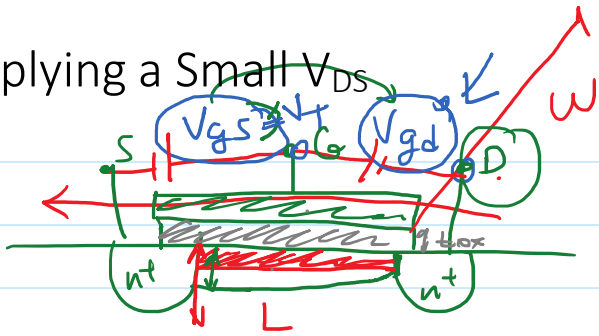
V_T

$V_{gs} = V_T$





Applying a Small V_{DS}

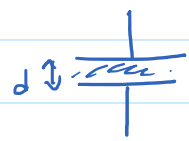


$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)\right] v_{DS}$$

$$i_D = I_{DS} = \left[\left(\mu_n C_{ox}\right)\frac{W}{L}\right]\left[(V_{GS} - V_T)\right] V_{DS}$$

$$I_{DS} = \frac{1}{R} \cdot V_{DS}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{d}$$



$$\mu_n C_{ox} = k'$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\mu_n C_{ox} \frac{W}{L} = k$$

$$i_D = k' \frac{W}{L}(v_{GS} - V_T) V_{DS} = i_D = k(v_{GS} - V_T) V_{DS}$$

V_{DS} Increased

$+ \quad V_{gd} - V_T = (V_{gs} - V_T) - V_{ds} \quad \Leftrightarrow \quad V_{gs} - V_T > V_{ds}$

$V_{gd} = V_{gs} - V_{ds}$

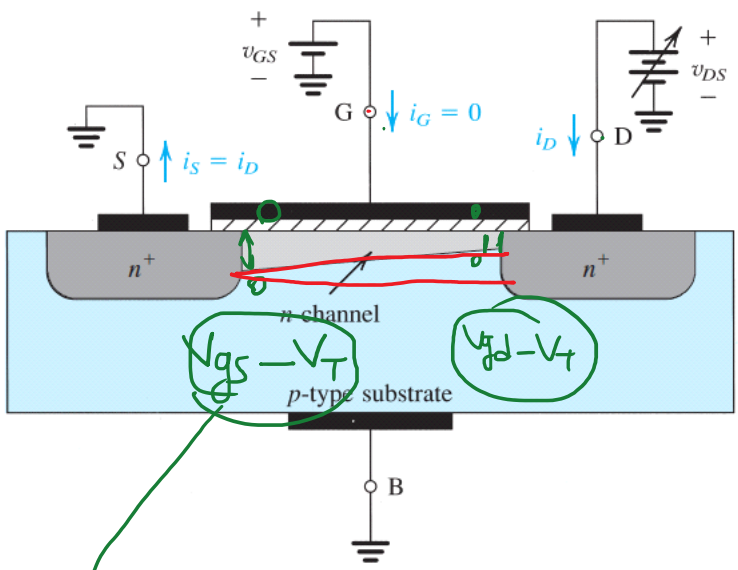
$V_{gd} - V_T = V_{gs} - V_{ds} - V_T$

$V_{gd} = V_{gs} - V_{ds}$

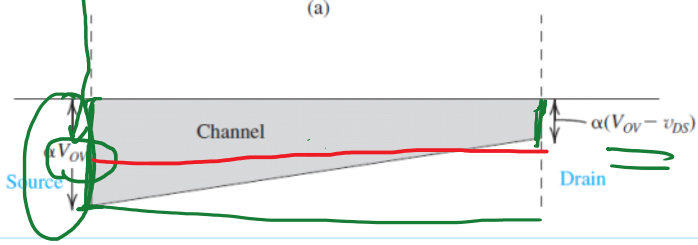
$= V_g - V_s - (V_d - V_s)$

$= V_g - V_s + V_s - V_d$

$= V_{gd}$



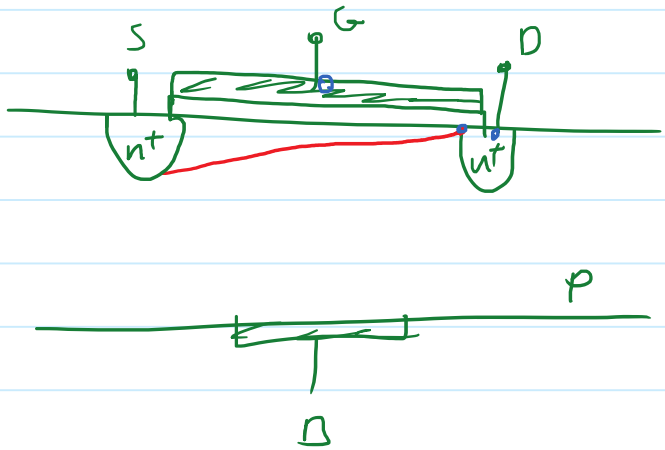
(a)



$V_{ov} = V_{gs} - V_T$

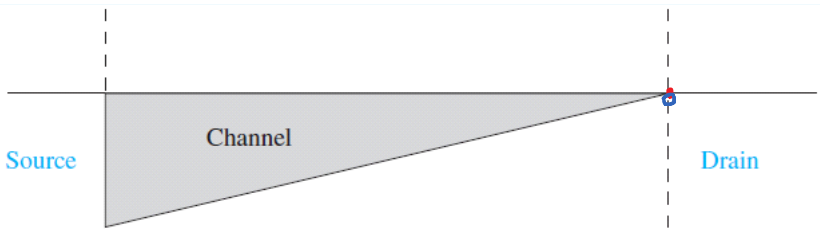
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T) V_{ds}$$

Channel Pinch-Off



$V_{ds} \uparrow \quad V_{gd} \downarrow$

$V_{gd} - V_T < 0$



$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 = I_{DS}$$

$$V_{GS} - V_T < V_{DS} \Rightarrow$$

Example

$V_{OV} > 0$

Consider a process technology for which $L_{min} = 0.4\ \mu m$, $t_{ox} = 8\ nm$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.7\ V$.

(a) Find C_{ox} and k_n'.

(b) For a MOSFET with $W/L = 8\ \mu m/0.8\ \mu m$, calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\ \mu A$.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} \cong 4.3\ fF/\mu m^2$$

10^{-15} 10^{-6}

$$k_n' = \mu_n C_{ox} = 450\ cm^2/(V \cdot s) \cdot 4.3\ fF/\mu m^2$$

$$= 194\ \mu A/V^2$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$

V_{OV}

$$100 = \frac{1}{2} 194 \cdot 10 \cdot V_{OV}^2$$

$$V_{OV} = \pm 0.32\ V.$$

$$V_{GS} - V_T = 0.32 = V_{GS} - 0.7 \Rightarrow V_{GS} = 1.02\ V$$

$V_{GS} - V_T \angle V_{DS}$

V_{OV}

$C_{ox} = 4.32\ fF/\mu m^2$

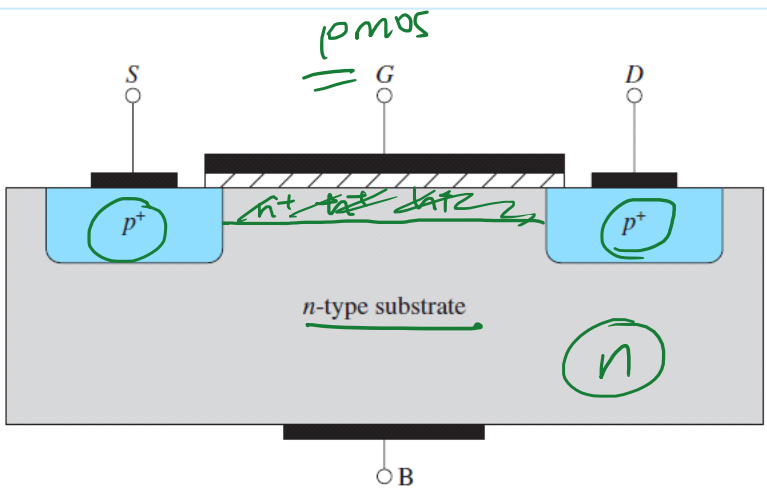
$k_n' = 194\ \mu A/V^2$

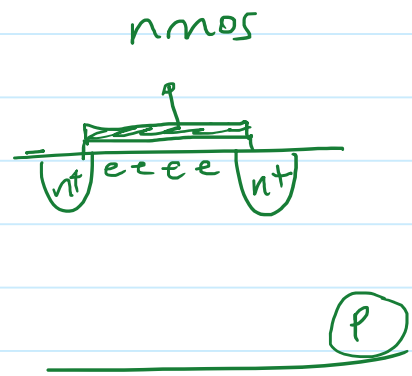
$V_{OV} = 0.32\ V$

$V_{GS} = V_t + V_{OV} = 1.02\ V$

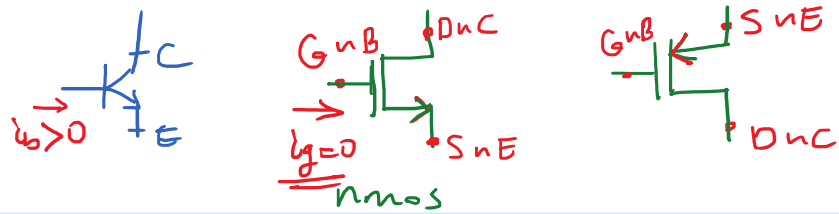
$V_{DSmin} = V_{OV} = 0.32\ V$

p-Channel MOSFET





Example



Design the circuit of Fig. 5.21: that is, determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu$A/V^2, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

$V_t = 0.7$ $k_n' = 100\mu A/V^2$ $\frac{W}{L} = 32$

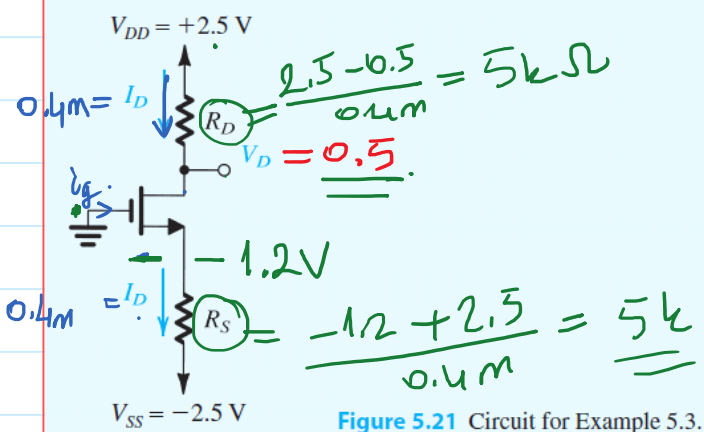


Figure 5.21 Circuit for Example 5.3.

$V_{GD} - V_T = V_G - V_D - V_T = 0 - 0.5 - 0.7 < 0$

$0.4m = I_D = \frac{1}{2} \cdot 100 \cdot 32 \cdot V_{OV}^2 \Rightarrow V_{OV} = 0.5V = V_{GS} - V_T$

$V_{GS} = 1.2V$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)\right] v_{DS}$$

linear mode

$V_{GS} - V_T > V_{DS}$

$V_{GD} - V_T > 0$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

saturation

$V_{GS} - V_T < V_{DS}$

$V_{GD} - V_T < 0$

cut-off

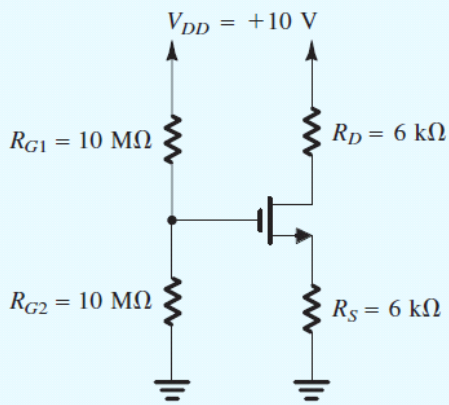
$V_{GS} - V_T < 0$

$V_{OV} < 0$

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

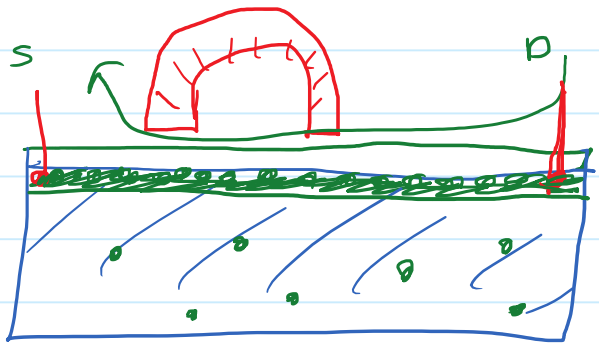
Example

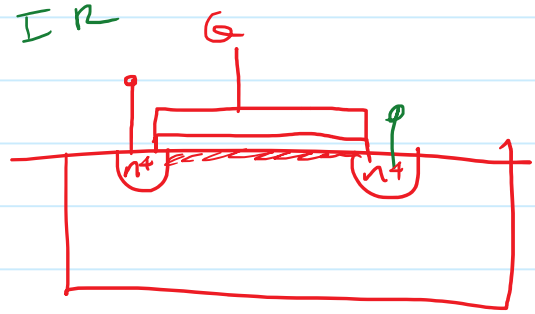
Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k'_n(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



$$I_D = 0.5 \text{ mA}$$
$$V_S = 0.5 \times 6 = +3 \text{ V}$$
$$V_{GS} = 5 - 3 = 2 \text{ V}$$
$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

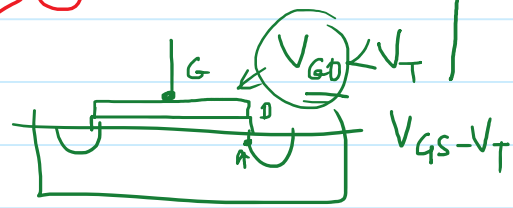
Template

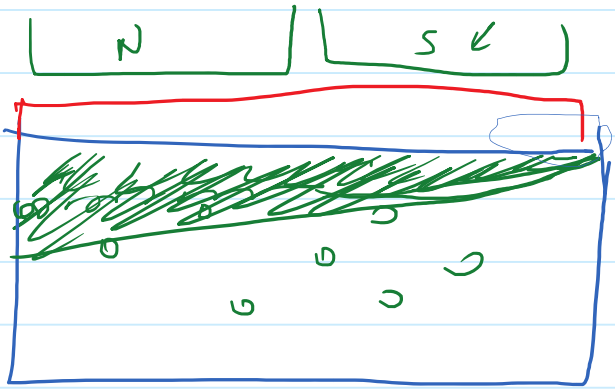




$$I_{DS} = \frac{1}{R} \cdot V_{DS} = \left(k' \frac{W}{L} (V_{GS} - V_T) \right) \cdot V_{DS}$$

$$V_{GS} \geq V_T \Rightarrow V_{GS} - V_T > 0$$





→ saturation

$$I_{DS} = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2$$