Yunus Emre Ertunç [flag]
150117069

Q3)

clear
64 cnt   5 bit
1   up counter
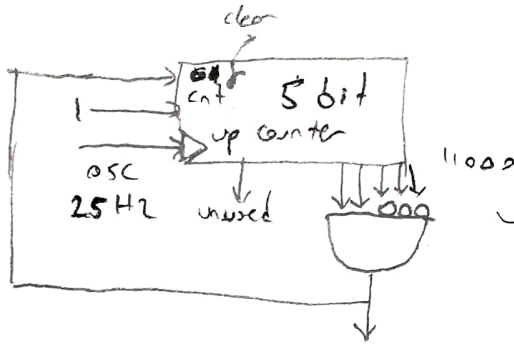OSC
25 HZ   unused   11000
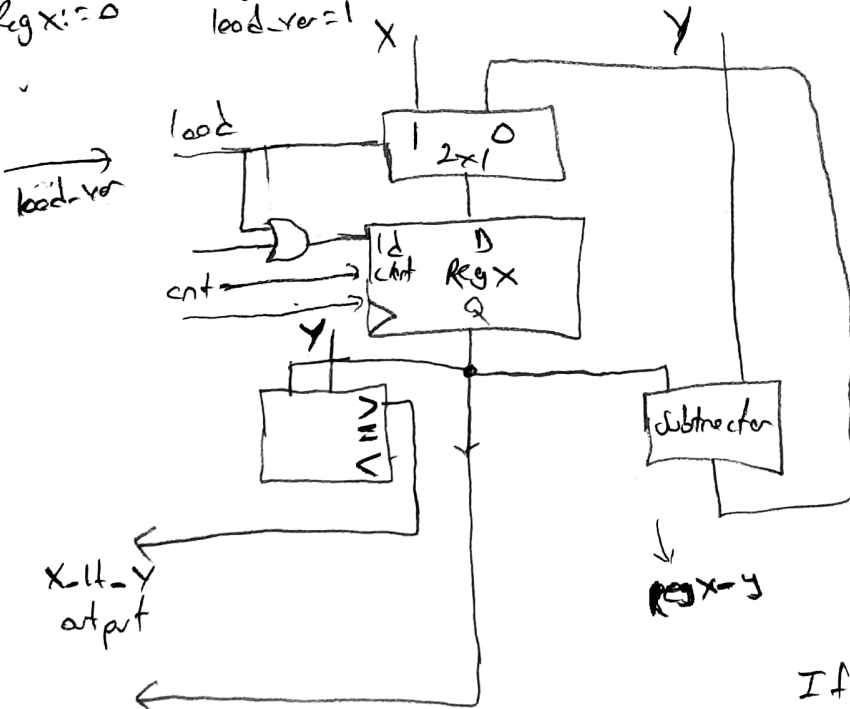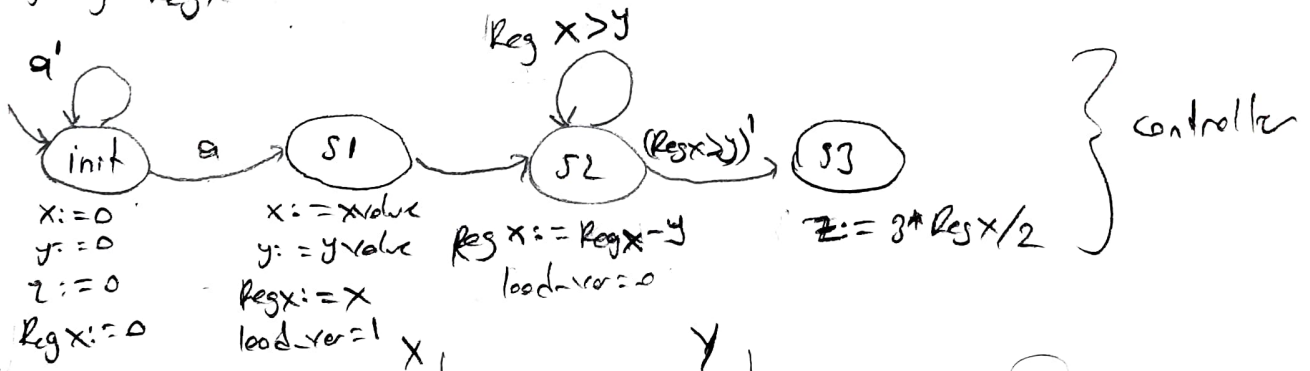
when result is 24
it pulses as signal and
clear

$(mod\ 5)$
   5   0

Q4)

inputs: $x, y, a, load\_var$
output: z
storages: $Reg\ x$

$(mod\ 3)$
   7, 4, ①

Reg $x > y$

a'
→ init —a→ S1 —→ S2 —$(Reg\ x > y)'$→ S3   } controller
                        Reg $x > y$

init: S1:   S2:   S3:
$x := 0$ $x := x\ value$ Reg $x := Reg\ x - y$ $z := 3 * Reg\ x / 2$
$y := 0$ $y := y\ value$ $load\_var := 0$
$z := 0$ Reg $x := x$
Reg $x := 0$ $load\_var := 1$

X   Y

load
load_var | 2×1 | 0
                          datapath
ld
cnt → cnt Reg X
            D
            Q
Y

$< | | >$ Subtracter

X_lt_Y
output

Reg x−y

↓
FSM
Part

If using multiplier / divider is
allowed, I would use them for result
part. when $x < y$ then $\underline{3 * reg\ x / 2}$

✓ Session 2