

Q1 (15 PTS)

You are going to enhance a machine, and there are two possible improvements: either make multiply instructions run four times faster than before or make memory access instructions run five times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 40% for memory access instructions, and 40% for other tasks. What will be the speedup if both improvements are made?

$$\text{CPU time}_{\text{old}} = 100$$

$$\text{CPU time}_{\text{new}} = \frac{20}{4} + \frac{40}{5} + 40 = 53$$

Multiplication
Memory access
other tasks

$$\text{Speedup} = \frac{100}{53}$$

Q2 (35 PTS) (parts a and b are related)

(a) Suppose we have two implementations (M1 and M2) of the same instruction set architecture. Machine 1 has a clock rate of 2.5 GHz and takes an average of 2.0 clock cycles per instruction (CPI) for a program. Machine 2 has a clock rate of 2 GHz and a CPI of 1.2 for the program. Which machine is faster for this program, and by how much?

$$\text{CPU time} = \frac{\text{IC} \times \text{CPI}}{\text{Clock rate}} \quad \text{CPU time}_{M1} = \frac{\text{IC} \times 2.0}{2.5} \quad \text{CPU time}_{M2} = \frac{\text{IC} \times 1.2}{2.0}$$

$$\frac{\text{Performance}_2}{\text{Performance}_1} = \frac{\text{CPU time}_1}{\text{CPU time}_2} = \frac{\frac{\text{IC} \times 2.0}{2.5}}{\frac{\text{IC} \times 1.2}{2.0}} = \frac{4}{3}$$

M2 is 1.33 times faster than M1

(b) Suppose that the 25 million instructions implemented on M1 fall into two performance classes, the first (Class A) takes one clock cycle to execute, while the second (Class B) takes 5 clock cycles to execute. How many Class B instructions are executed when our program is run?

$$25 \times 10^6 = A + B$$

of As
of Bs

$$\text{CPI} = \frac{(25 \times 10^6 - B) \times 1 + B \times 5}{25 \times 10^6} = 2.0$$

$$25 \times 10^6 - B + 5B = 2 \times 25 \times 10^6$$

$$4B = 25 \times 10^6$$

$$B = \frac{25}{4} \times 10^6$$

Q3 (25 PTS)

For this question, provide efficient translations (**with minimum number of instructions**) for the following standard MIPS pseudoinstructions.

- (18) ble \$s1, \$s2, label **(Your code should have 2 instructions)**
/* Conditionally branch to instruction at label, if register \$s1 is less than or equal to \$s2. */

slt \$s3, \$s2, \$s1
beq \$s3, \$zero, label

- (7) move \$s1, \$s2 **(Your code should have 1 instruction)**
/* move the value of \$s2 to \$s1 */

add \$s1, \$zero, \$s2

Q4 (25 PTS)

Assume that registers \$s1 has 0x2600AB03 value (in hexadecimal) and \$s2 has 0x0230D344 value (in hexadecimal) before the execution of the following code.

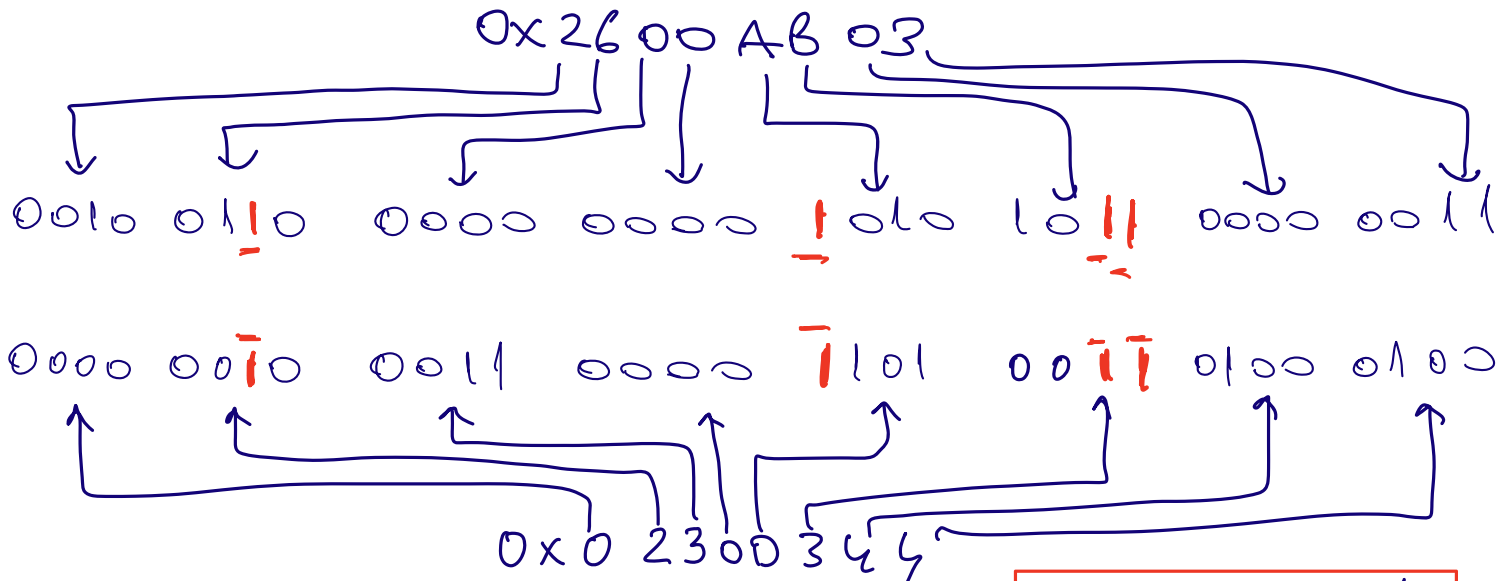
What will be the value of \$s5 (**in decimal**) after the execution of the following code is completed.

```

add    $s5, $zero, $zero
and    $s3, $s1, $s2
loop:  andi  $s4, $s3, 1
      srl  $s3, $s3, 1
      beq  $s4, $zero, check
      addi $s5, $s5, 1
check: bneq $s3, $zero, loop

```

This code counts # of bit positions
in \$s1 and \$s2 where both
are 1.
The result is in \$s5



\$s5 is equal to 4