

Q4)

	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₈	C ₉	C ₁₀	C ₁₁	C ₁₂
lw S1, 4(S2)	IF	ID	Ex	Mem	WB							
add S2, S4, S1		IF	ID	Ex	Mem	WB						
lw S4, 12(S3)			IF	ID	Ex	Mem	WB					
add S6, S4, S5				IF	ID	Ex	Mem	WB				
sub S8, t2, t3					IF	ID	Ex	Mem	WB			
and S8, S4, t1						IF	ID	Ex	Mem	WB		

12 cycles are required

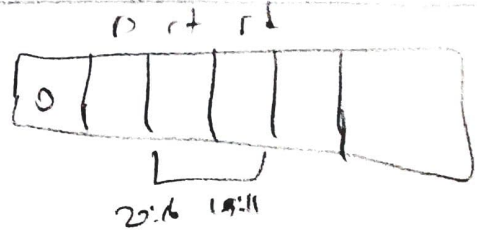
b) lw S1, 4(S2)
add S2, S4, S1
lw S4, 12(S3)
sub S8, t2, t3
and S8, S4, t1
add S6, S4, S5

IF	ID	Ex	Mem	WB	Mem	WB	Mem	WB	Mem	WB	Mem	WB
IF	ID	ID	Ex	Ex	Ex	Mem	WB	Mem	WB	Mem	WB	WB
	IF	IF	ID	ID	ID	Ex	Mem	WB	Mem	WB	Mem	WB
			IF	IF	IF	ID	Ex	Mem	WB	Mem	WB	WB

14 cycles are required

Q5) nrs, rd, rs, rt

rd=1 if rs ≠ rt



- nrs signal is added ①
- invert of ALU result and new signal ② is connected to AND matrix
- ① input and ALU Result is connected to 2x1 mux. ③
- select bit is result of ② option
- ③ option is connected to register file as write data. ④

Q6) lw2 S2, S4, S1

No need to change in datapath.
operation can be done by using correct signals.

Q7) a) $\text{Mem}[24(51)]$ will be loaded to $s2$

b) No error in beg. Because $s8 = t12$ and $t12 = s8$
will yield some result for beg.