CSE 3015

Study Questions II

Q1) Create an FSM that has an input x and output y. Whenever x changes from 0 to 1, y should become 1 for 3 clock cycles and then return to 0 – even if x is still 1. Design the controller.

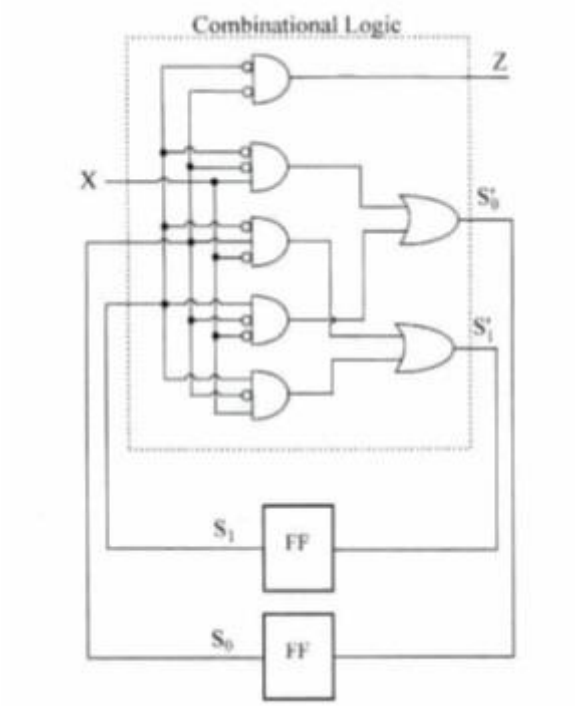
Q2) Design an 8-bit register with 2 control inputs s1 and s0, 8 data inputs I7…I0 and 8 data output Q7..Q0. The details of control bits are given below:

- s1s0=00: Register maintains its present value
- s1s0=01: Register loads from data inputs.
- s1s0=10: Register reverses its bits. 1110 becomes 0111, 1010 becomes 0101
- s1s0=11: Register complements itself. 1110 becomes 0001, 0000 becomes 1111.

Q3) Design a full adder using:

a. Half adders
b. A 3-to-8 decoder

Q4) The logic diagram shown below is an FSM. Constrcut the truth table and draw the state machine for the given logic diagram.



Q5)

Design a 4-bit register with 2 control inputs s_1 and s_0, 4 data inputs $I_3..I_0$, and 4 data outputs $Q_3..Q_0$. The function table below shows the configurations for the register.
In this question you have to design the circuit inside the "Black Box".

S1	S0	Action
0	0	Clear the contents of the register
0	1	Load I
1	0	Rotate right by one bit
1	1	Rotate left by one bit

Q6) Using **only a 4-bit up** binary counter, you are going to design a circuit that detects odd numbers in a sequence of numbers, its output (denoted by **ODD**) is 1 when the sequence value is an odd number, 0 otherwise. The sequence is defined below in Q3a. You can use any of the following components (**Specify the bit widths, and name all inputs/outputs**):

1) Adders
2) Shifters
3) Comparators
4) Multiplexers
5) Subtractors

Make sure you answer both parts 6a, and 6b.

6a. Using the 4-bit up binary counter, create a circuit that generates the following sequence:

48 -> 45 -> 42 -> 39 -> 36 -> 33 ->30 -> 27 -> 24 -> 21 ->18 -> 15 -> 12 -> 9 -> 6 -> 3 -> 48 -> 45 -> 42

6b. Using the circuit designed in part 6a, modify it so that whenever an odd number is encountered in the sequence generated, your circuit outputs a 1 (ODD signal is 1), otherwise, it outputs a 0.