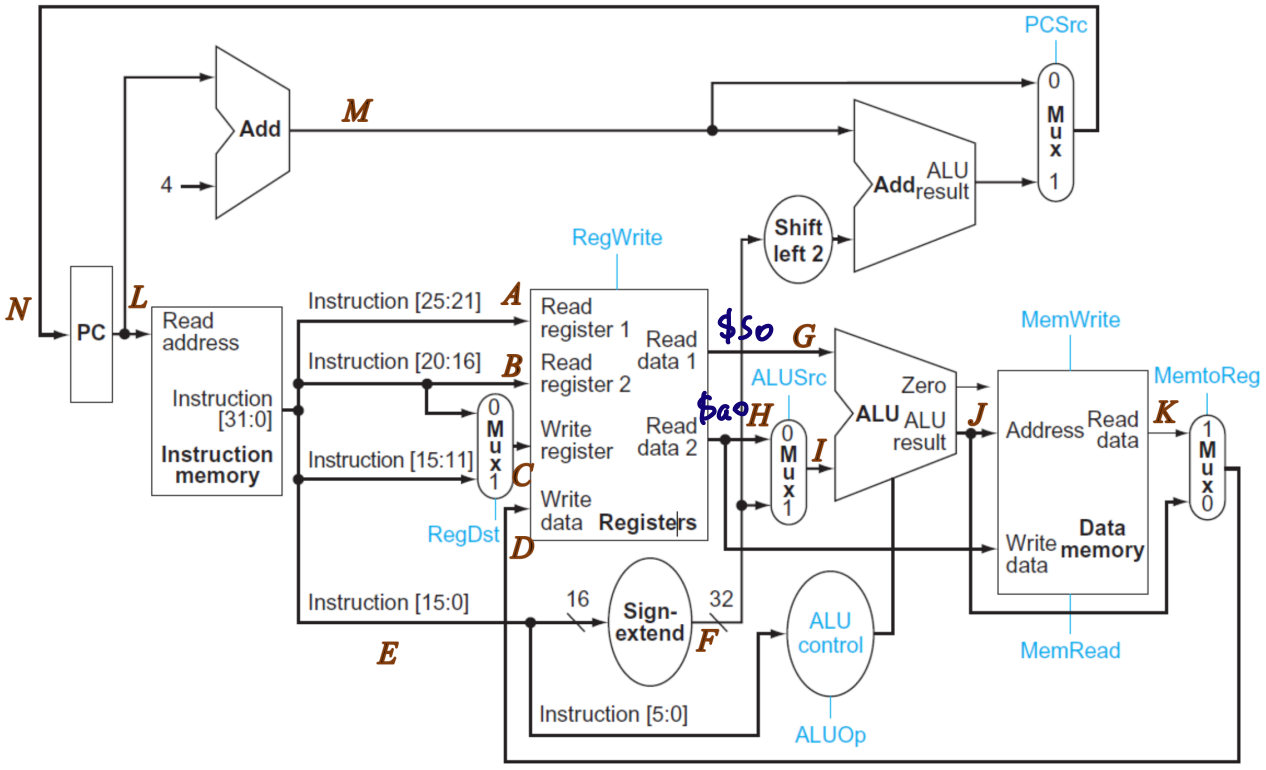
CSE 3038 – Computer Organization - QUIZ 3 – Spring 2022

Name: **Signature:**

Question 1 (40 PTS)- Consider the following single cycle datapath model, answer the following questions:



Given that: registers **$a0 = -128** and **$s0 = 130**; and the instruction at the input (the instruction read from instruction memory) is **add $t0, $s0, $a0**; and the instruction is in memory address **0x00404400**,

What are the values for wires/buses given in the following table? (one answer was already given)
Give all your answers in an ***appropriately-sized hexadecimal.***

A	B	C	D	E	G
0x10	0x04	0x08	0x0000 0002	0x4020	0x0000 0082

H	J	L	N

0xFFFFFF80

0x0000 0002

0x00404400

0x00404404

Answer: add $t0, $s0, $a0

C A B

$a0 reg → #4 $t0 reg → #8

B → 0x04 C → 0x08

130 → 1000 0010

8 2

G → 0x00000082

```
00000...00  1000 0000
11111...11  0111 ...1
                   +1
-----------------------
11111...11  1000 0000   ⇒ -128
```

H → FFFF FF80

-128 + 130 = 2 D → 0x00000002

J and D are same.

Consider I[15:0] ↓

01000 00000 100000

rd shmt funct code

0100|0 000|00|10|0 000

→ 0x4020 → E

Question 2 (25 PTS)

Assume that we extend our single-cycle MIPS implementation so that it handles the "`jr` (jump to register)" instruction, where "`jr`" has R-type instruction format.

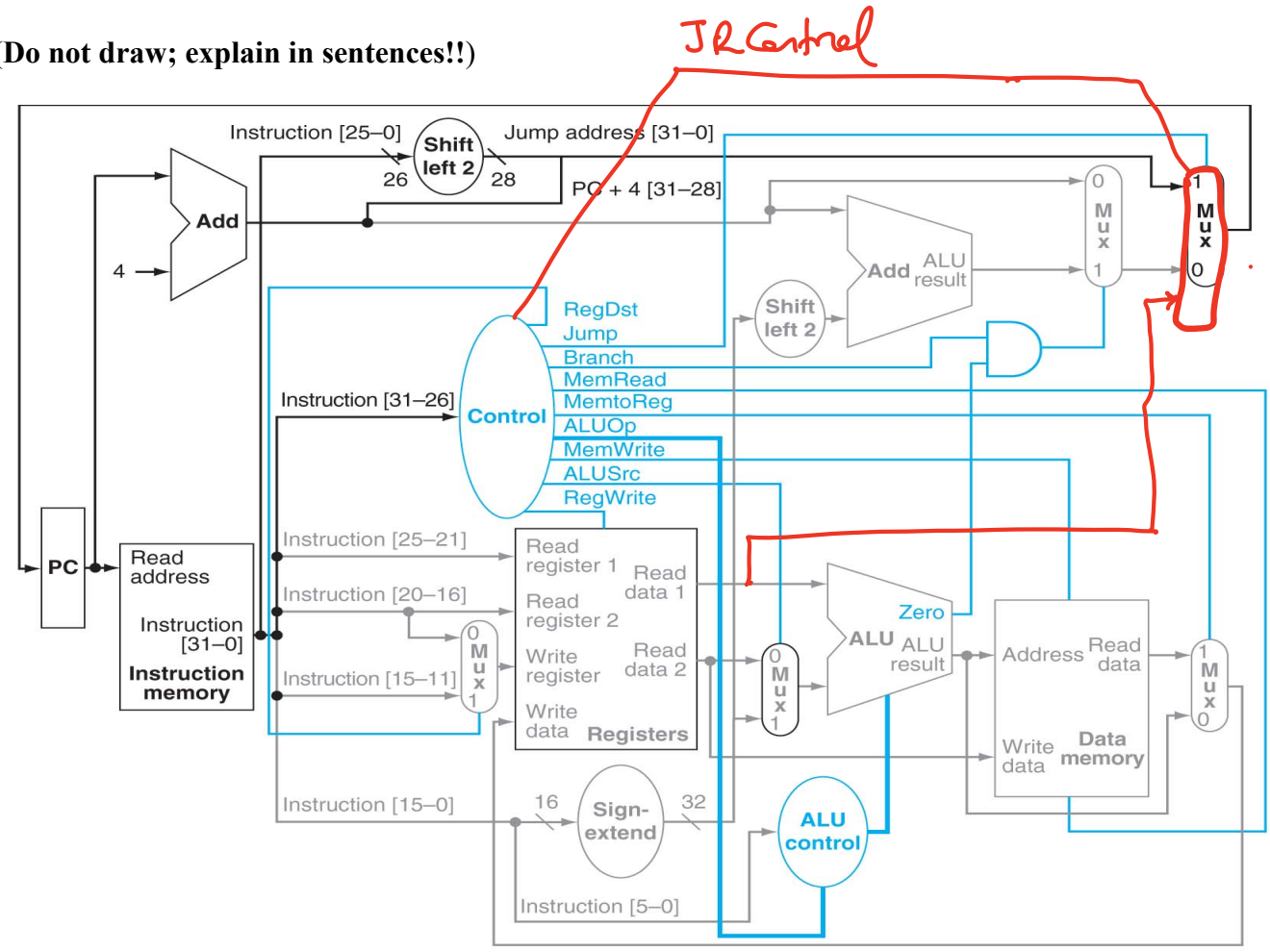
```
Example:        jr    $s2
```

The values of fields of the instruction format for the above instruction is the following:

Opcode(6)	rs(5)	rt(5)	rd(5)	shamt(5)	function code(6)
0	18($s2)	0	0	0	8

Explain the required changes in the complete single-cycle datapath clearly and *write down* any changes (additional wires, muxes and control and selector signals etc.) *if necesssary*.
In case of no change in the datapath, then express it accordingly.

(Do not draw; explain in sentences!!)



Answer

(1) Draw a line from "ReadData1" output of Register File to Jump Mux

(2) Mux controlled by Jump will be a 3 input mux Therefore a new control signal "JRCntrl" is required.

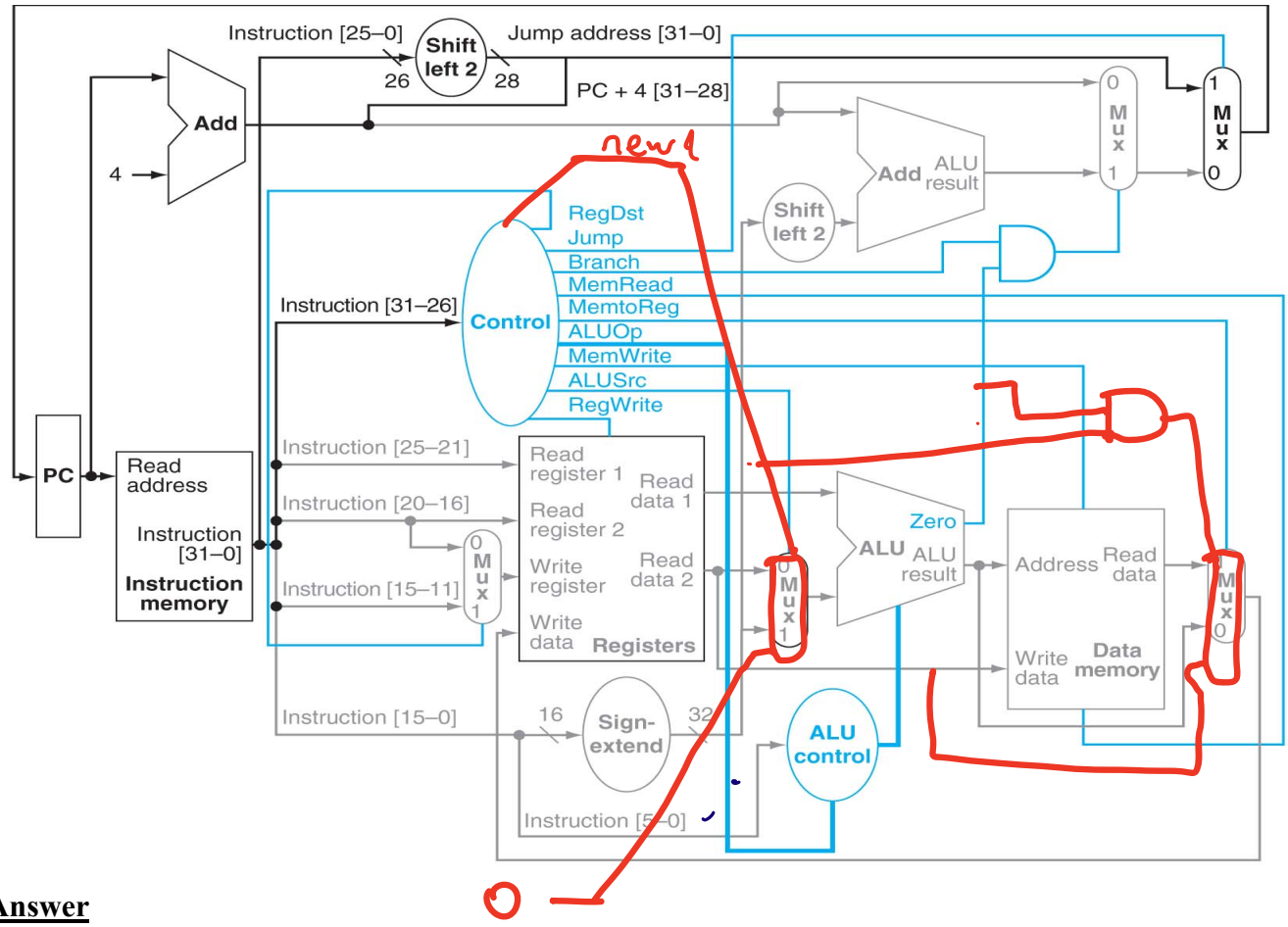
Question 3 (35 PTS)
Assume that a new R-type MIPS instruction "new1" is considered as follows:

```
new1 rd, rs, rt // if (R[rs] == 0) R[rd]←R[rt]

new1 $s1, $s2, $s3 // If ($s2 == 0) then $s1 ← $s3
                   // If ($s2 == 0) then copy the value from  $s3 to $s1)
```

Explain the required changes in the complete single-cycle datapath clearly and *write down* any changes (additional wires, muxes and control and selector signals etc.) *if necesssary*.
In case of no change in the datapath, then express it accordingly.

(Do not draw; explain in sentences!!)



Answer

(1) Expand ALUSrc mux (it will be 3-input mux)
(2) ADD Zero as the new input to ALUSrc mux
(3) new1 control signal connected to ALUSrc mux
(5) A new adder (connect Zero & new1 signal)
(5) Connect output of new adder to MemtoReg mux as the new control signal (MemtoReg will be 3-input mux)
(6) Connect "read data2" from register file to MemtoReg mux (3 input)