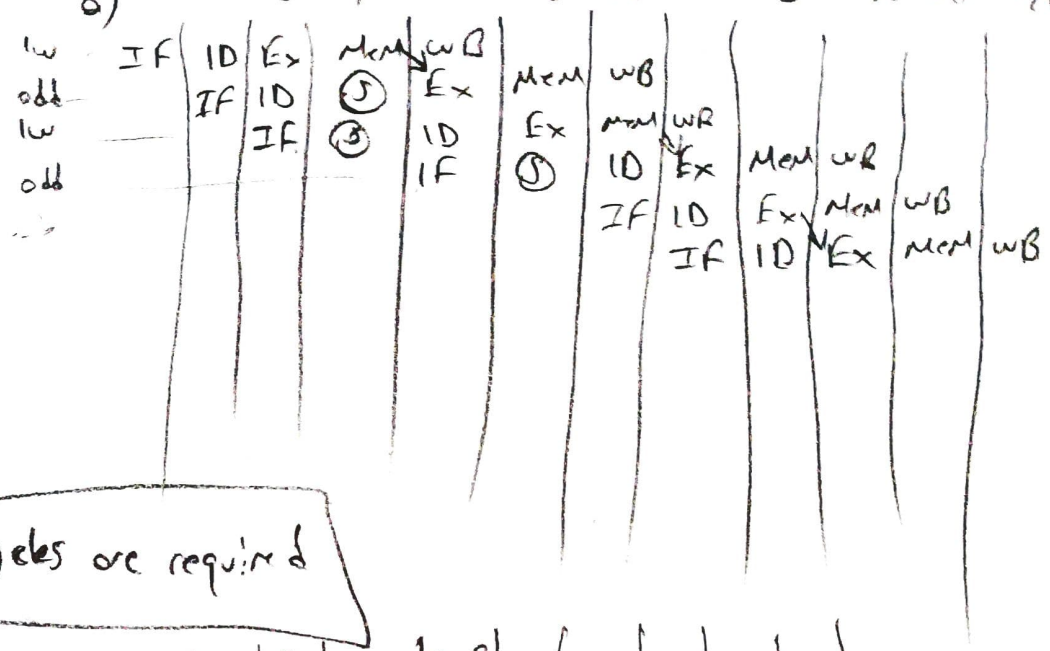
Q4)

a)

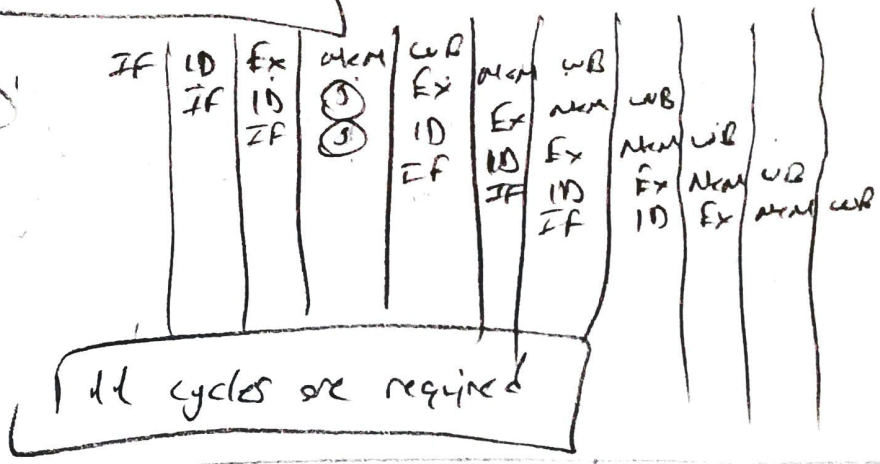
```
lw $1, 4($2)
add $2, $4, $1
lw $4, 12($3)
add $6, $4, $5
sub $8, $2, $3
and $8, $8, $1
```



12 cycles are required

b)

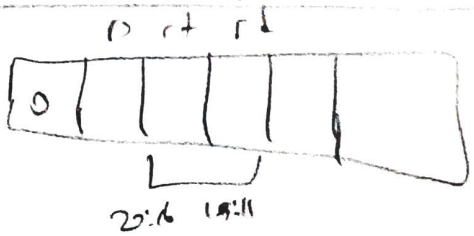
```
lw $1, 4($2)
add $2, $4, $1
lw $4, 12($3)
sub $5, $2, $3
and $8, $6, $1
add $6, $4, $7
```



11 cycles are required

Q5) nop, rd, rs, rt

rd=1 if rs ≠ rt



- nop signal is added (1)
- invert of ALU result and new signal (2) is connected to AND gate
- (1) input and ALU Result is connected to 2×1 mux. (3)
- (1) input and ALU Result is connected to 2×1 mux. (3) select bit is result of (2) option
- (3) option is connected to register file as write data. (4)

Q6) lw2 $2, $4, $1

No need to change in datapath.

operation can be done by using correct signals.

Q7) a) MEM[24(s1)] will be loaded to s2

b) No error in beq. Because s8 - t12 and t12 - s8 will yield same result for beq.