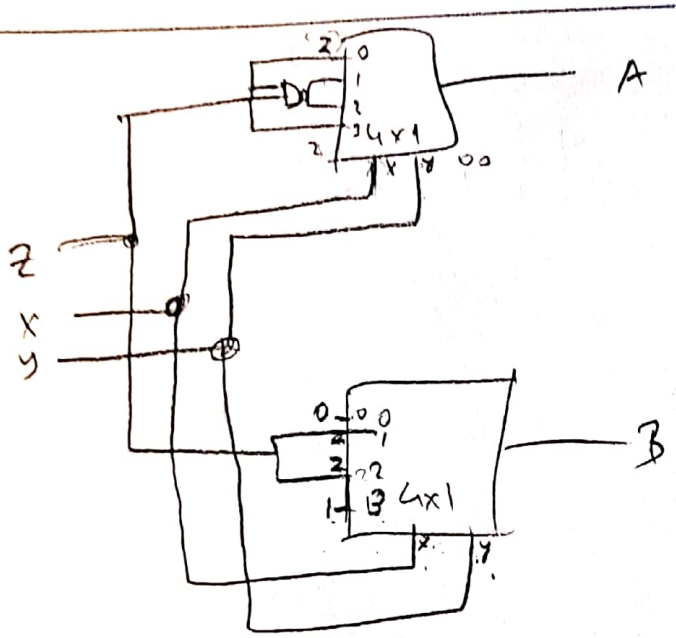
1.



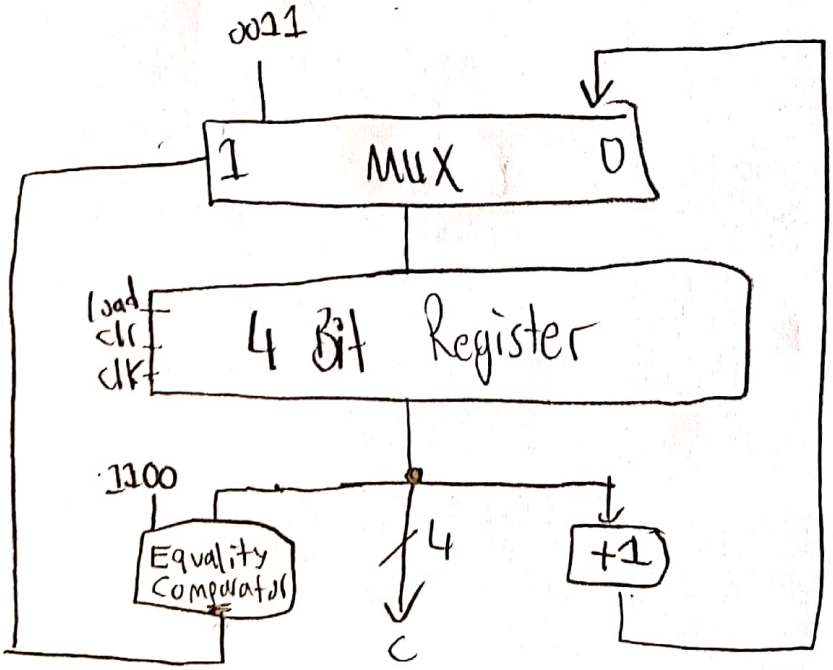
x	y	z	A	B
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

b) Show functionality.

2 NAND 2

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

2) Design counter that counts in sequence: 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 3



Bilgi: Gelen sayı 12'ye eşit ise tekrar 3'e dönmesi için MUX 1. bitine bağla. Değilse mesela 4 geldiyse +1 artır 0.'ya bağla. Ortadaki C ise o anlığı bitsin.

(3) Implement 4 bit register → 0 current, 1 loaded, 4 condition → 0 → load, 1 → current, 2 → left, 3 → right. Slayttı uygası var.

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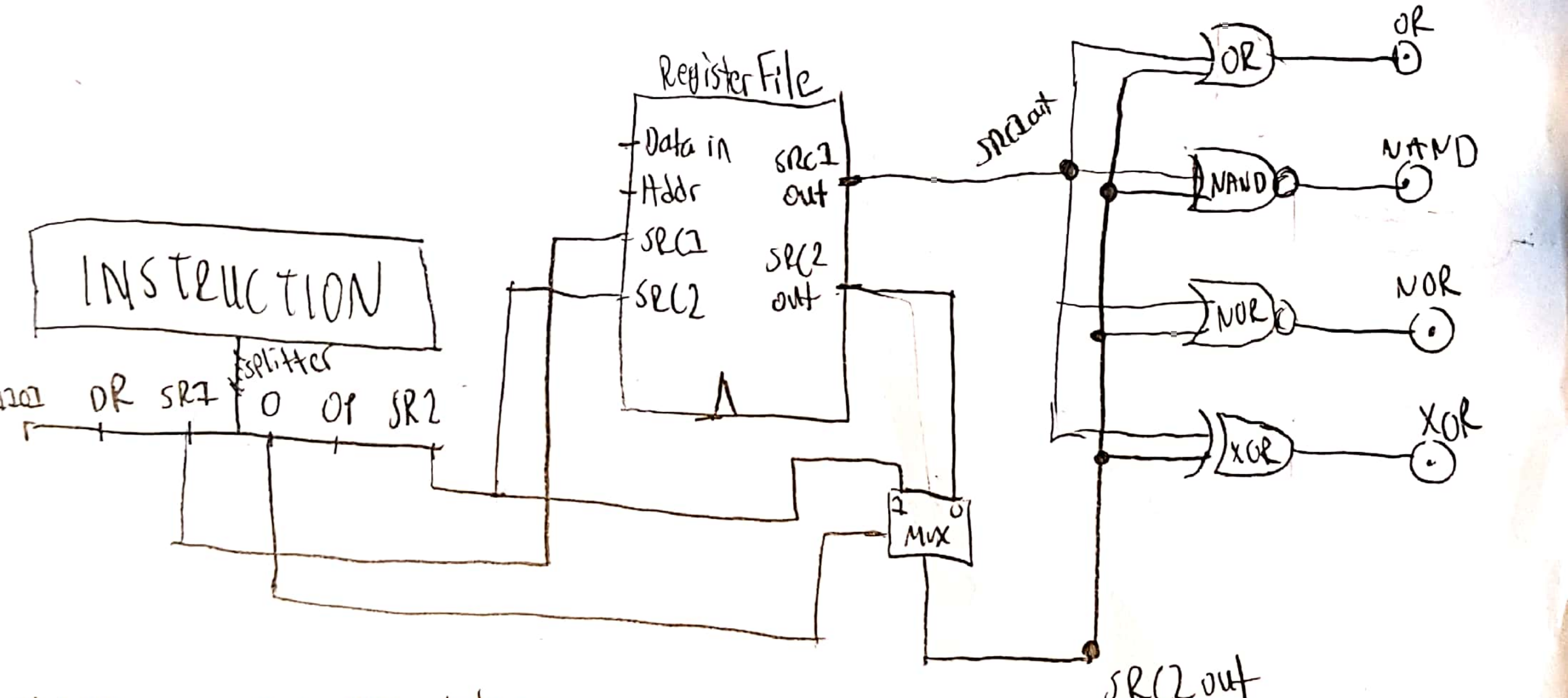
(4) Use opcode 1101 imp. four bitwise OR, NAND, NOR, XOR. 16 bit ins.

1101	DR	SR1	0	OP	SR2

. IR[5] → whether use imm val of register for the source value IR[4:3] → four logical op. to be performed. Design the circuit.



Bilgi: Eğer imm=0 ise SRC2 outtaki değeri yani SR2 adresinin içindeki değeri; imm1 ise direkt S2 adresini instruction dan al. → Bunun için mux kullandık.

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(5) RTL to find mean of the number. find mean X.
IF X → even: output: X/2. IF X → Odd → round to ⌈X/2⌉

ex: X=10, output = 5,
X=11, output: 6

Design RTL, circuit, fsm