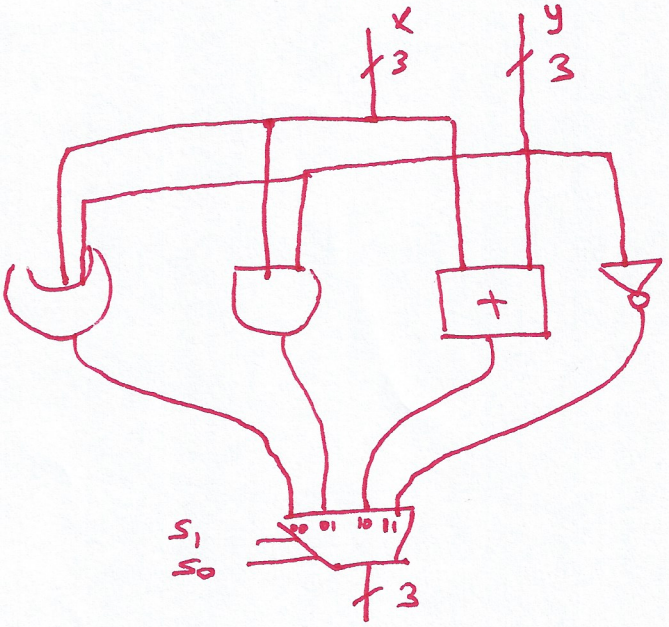
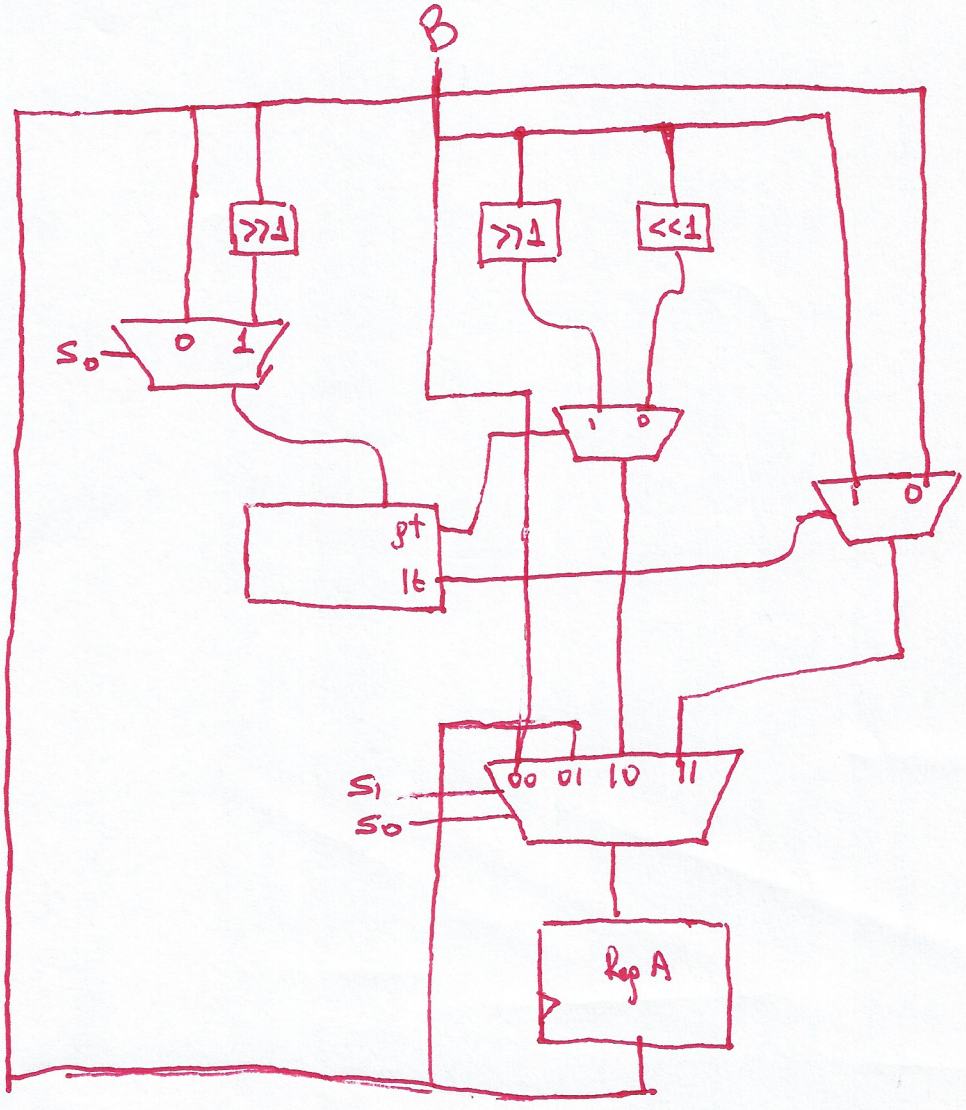
Study Questions -2

(1)



(2) Refer to chapter 4 slide 76.

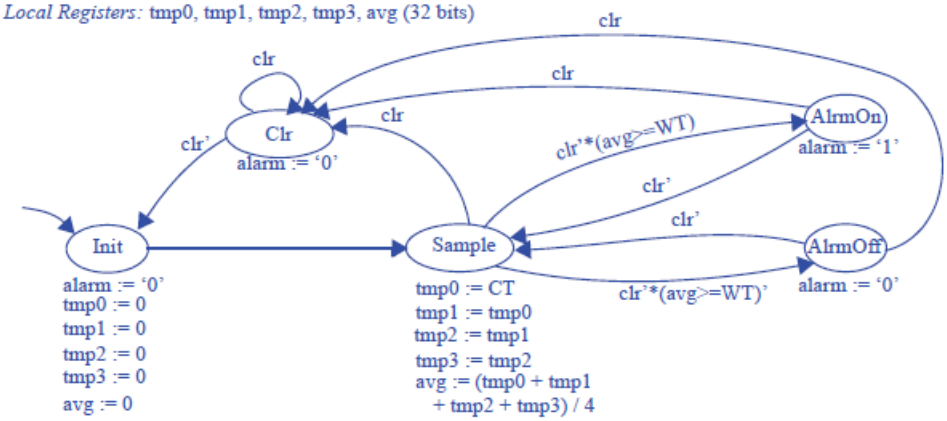
(4)



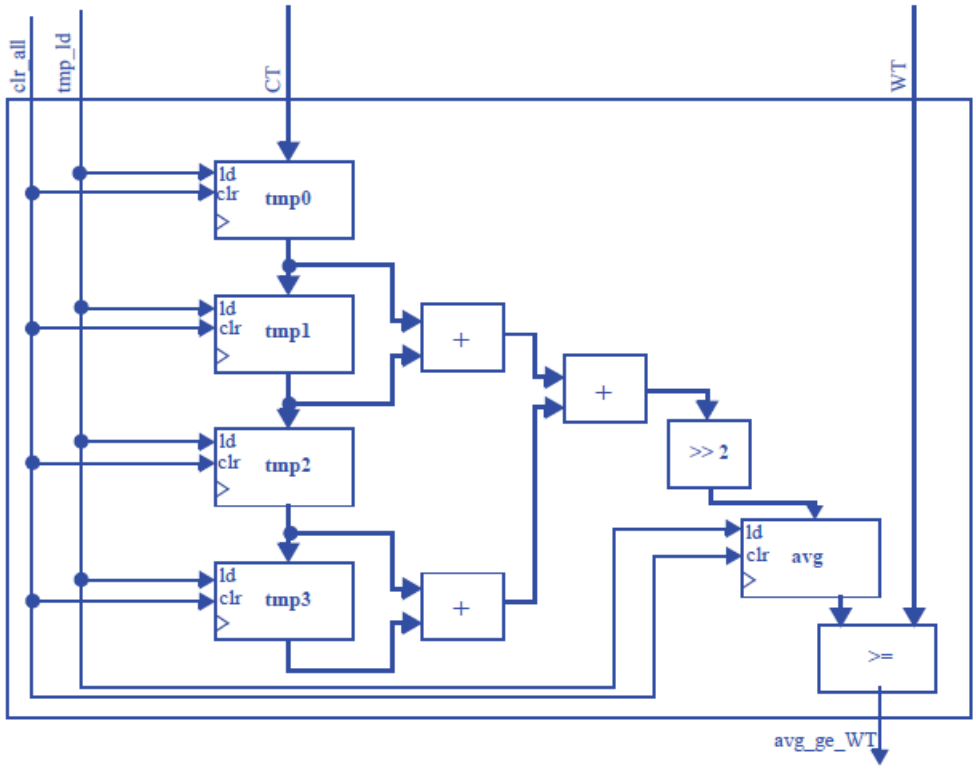
3)

Step 1 - Capture a high-level state machine

Inputs: CT, WT (32 bits); clr (bit)
Outputs: alarm (bit)
Local Registers: tmp0, tmp1, tmp2, tmp3, avg (32 bits)

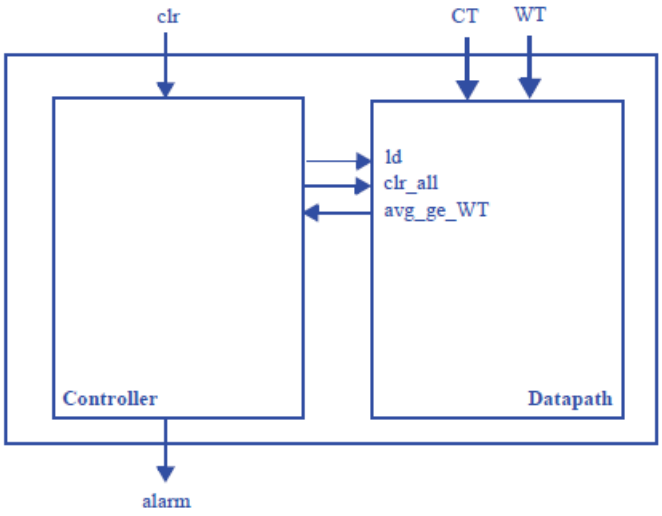


Step 2A - Create a datapath



Note: A solution more consistent with the chapter's methdology would use a separate clear and ld signal for each register. In this particular example, a single clr and a single load line happens to work.

Step 2B- Connect the datapath to a controller



Step 2C - Derive the controller's FSM

Inputs: clr, avg_lt_WT
Outputs: alarm, clr_all, ld