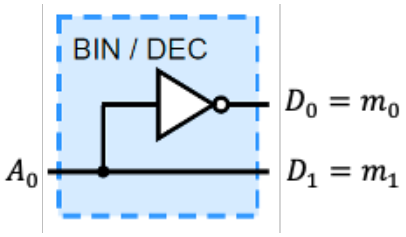
EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 8

1. (a)

Input	Outputs	
A	**D1**	**D0**
0	0	1
1	1	0

Functional block: 1-to-2 line decoder



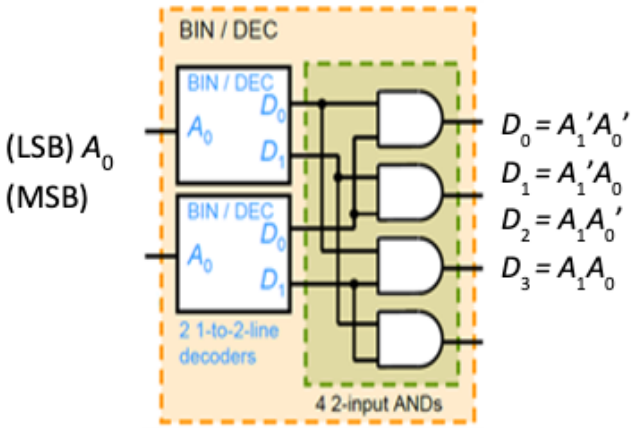
(b)

Inputs		Outputs			
A1	**A0**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Note:

Input	Outputs	
A1/A0	**SigA1(1)/SigA0(1)**	**SigA1(0)/SigA0(0)**
0	0	1
1	1	0

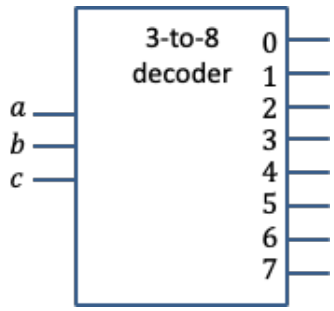
Functional block: 2-to-4 line decoder



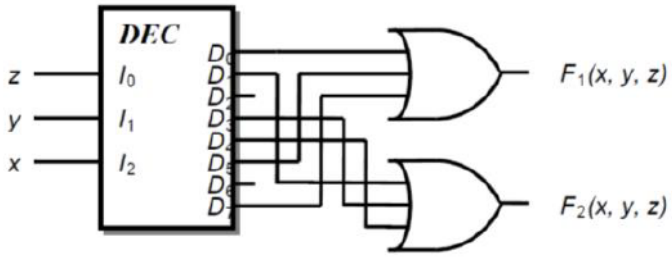
2. (a)

Input	Output
S	Q
000	00000001
001	00000010
010	00000100
011	00001000
100	00010000
101	00100000
110	01000000
111	10000000

Functional block: 3-to-8 line decoder



(b)



3.

Inputs										Outputs			
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	A_3	A_2	A_1	A_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1	0
0	0	0	0	0	1	0	0	0	0	0	1	1	1
0	0	0	0	0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1	1	0	0
0	0	0	0	0	0	0	0	0	1	1	1	0	1

```
library ieee;
use ieee.std_logic_1164.all;

entity DTG_encoder is
    port (
        D_in : in std_logic_vector(9 downto 0);
        G_out : out std_logic_vector(3 downto 0)
    );
End DTG_encoder;

architecture Behavior of DTG_encoder is
begin
        process (D_in)
        begin
                G_out(3) <= D_in(8) OR D_in(9);
                G_out(2) <= D_in(4) OR D_in(5) OR D_in(6) OR D_in(7) OR D_in(8)
        OR D_in(9);
                G_out(1) <= D_in(2) OR D_in(3) OR D_in(4) OR D_in(5);
                G_out(0) <= D_in(1) OR D_in(2) OR D_in(5) OR D_in(6) OR D_in(9);
        end process;
end Behavior
```

4.

Inputs				Internal signal	Output	State
a	**clk**	**x**	**y**	**tmp**	**z**	
1	X	X	X	0	$0 \rightarrow 0$ $1 \rightarrow 0$	Reset
0	0, 1, ↑	X	X	X	$0 \rightarrow 0$ $1 \rightarrow 1$	Hold
0	↓	0	0	X	$0 \rightarrow 0$ $1 \rightarrow 1$	Hold
0	↓	0	1	0	$0 \rightarrow 0$ $1 \rightarrow 0$	Reset
0	↓	1	0	1	$0 \rightarrow 1$ $1 \rightarrow 1$	Set
0	↓	1	1	$0 \rightarrow 1$ $1 \rightarrow 0$	$0 \rightarrow 1$ $1 \rightarrow 0$	Toggle

Functional block: Negative-edge triggered JK Flip-Flop with asynchronous Active High CLR.