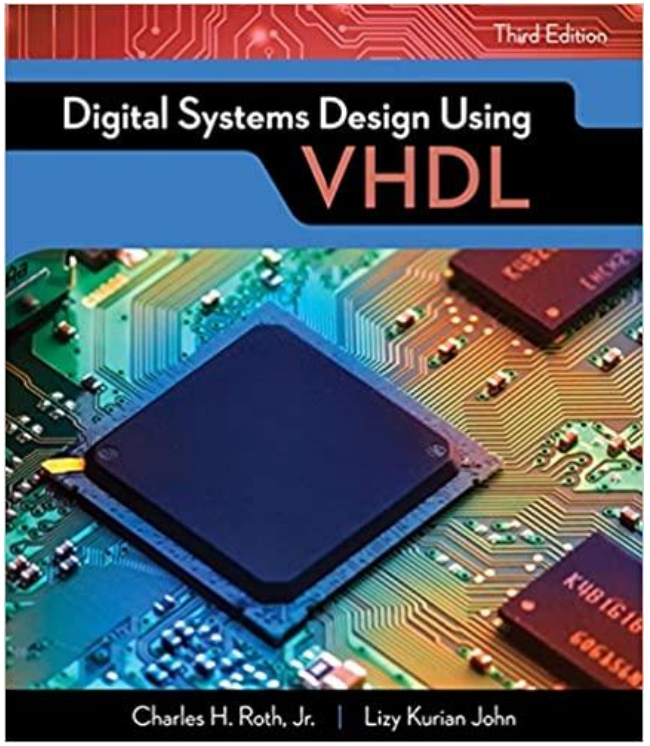
EE2000 Logic Circuit Design

Lecture 4- VHDL



Question

Which of the following identifier is illegal to be used as an entity name in VHDL?

- TwO_gaTE Legal
- 2_gate Illegal – cannot start with a number
- T2-gate Illegal – cannot have other symbol
- _2gate Illegal – cannot start with underscore
- AND Illegal – Reserved word

Exercise

```
signal C: bit_vector (0 to 3);
signal D: bit_vector (3 downto 0);
signal A: bit_vector (7 downto 0);
```

```
C <= "1101";
D <= C;
A(6 downto 3) <= D;
```

Determine the stored value in the following bit object

```
C(0) = 1  C(1) = 1  C(2) = 0  C(3) = 1
D(3) = 1  D(2) = 1  D(1) = 0  D(0) = 1
A(6) = 1  A(5) = 1  A(4) = 0  A(3) = 1
```

Exercise

Transform the following logic expression to VHDL code

1) f = ab’ + a’b

```
f <= a AND NOT b OR NOT a AND b;
f <= (a AND NOT b) OR (NOT a AND b);
```

2) f = a(b’ + a’)b

```
f <= a AND (NOT b OR NOT a) AND b;
```

Exercise

Transform the following logic expression to VHDL code

Boolean	VHDL Boolean

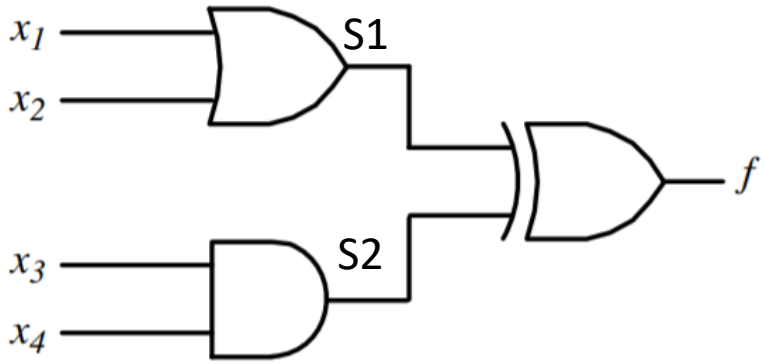
$Y = \overline{AB}$	`Y <= NOT(A AND B);`
	`or`
	`Y <= A NAND B;`

$Y = \overline{A + B}$	`Y <= NOT(A OR B);`
	`or`
	`Y <= A NOR B;`

$Y = A + BC$	`Y <= A OR (B AND C);`
$Y = C\overline{X + D}$	`Y <= C AND NOT (X OR D);`

$Y = A\bar{B}C + \bar{A}\,\bar{B}C + \overline{AB}C$	`Y <= (A AND NOT B AND C) OR`
	`(NOT A AND NOT B AND C) OR`
	`(NOT (A AND B) AND C);`

Exercise



Write your own VHDL statement to describe the logic circuit

```
S1 <= x1 OR x2;
S2 <= x3 AND x4;
F <= S1 XOR S2;
```

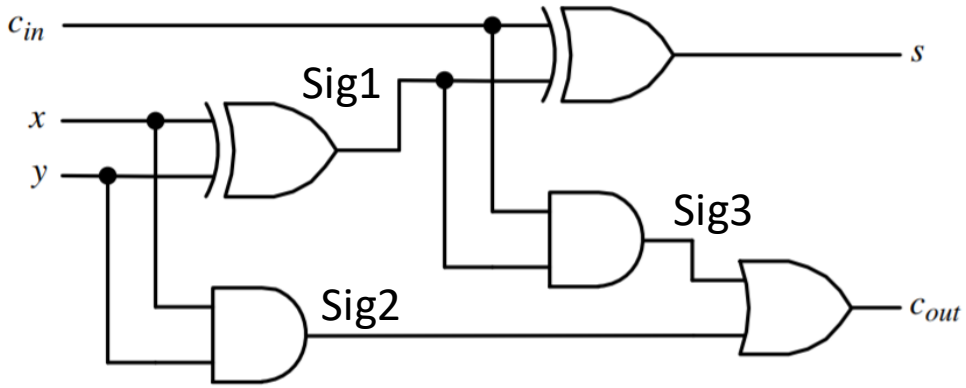
OR

```
F <= (x1 OR x2) XOR (x3 AND x4);
```

- The Left-hand style is more readable and traceable but needs to declare two more signals
- In contrast, the Right-hand style uses fewer lines of code but is a bit difficult for debugging
- They both have the same result after being synthesized

Exercise

Write your own VHDL statement to describe the logic circuit



Sig1 <= x XOR y;
Sig2 <= x AND y;
Sig3 <= Sig1 AND C_{in};
s <= C_{in} XOR Sig1;
C_{out} <= Sig3 OR Sig2;