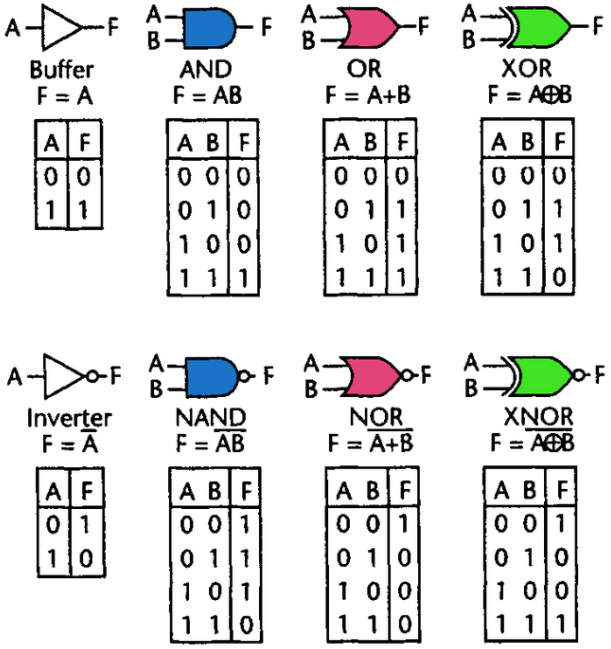
EE2000 Logic Circuit Design

Lecture 11 – Revision



Instructables.com

Exercise

$$\{(b'+c')'(c+bc')(ab'c'+b'+c')+[(a+c')(b+c)]'\}'$$

$$=\{(b'+c')'(c+bc')(b'+c')+[(a+c')(b+c)]'\}'$$

Absorption

$$=[(a+c')(b+c)]''$$ Complement

$$=(a+c')(b+c)$$ Involution

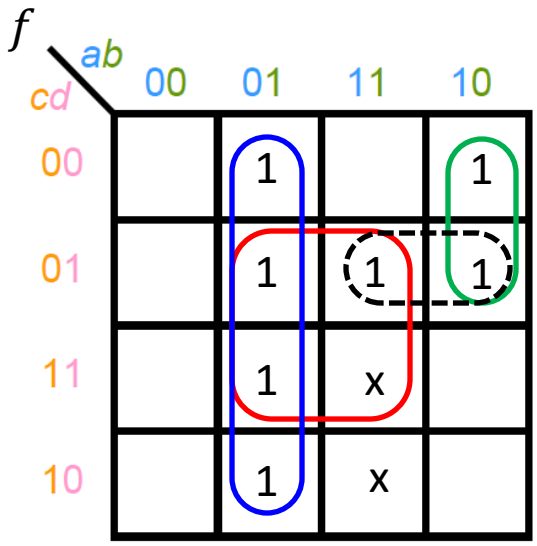
$$=ab+ac+bc'$$

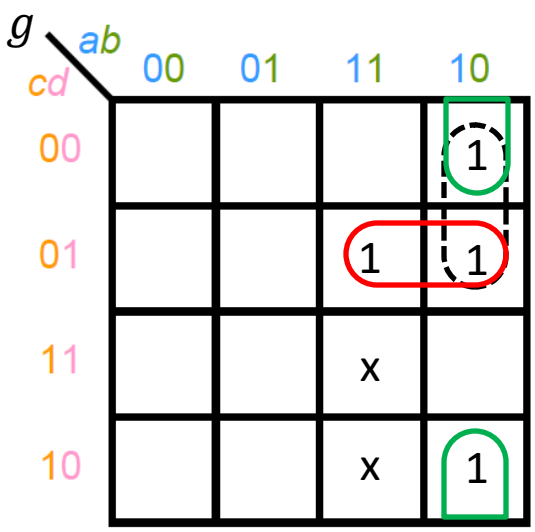
$$=ac+bc'$$ Consensus

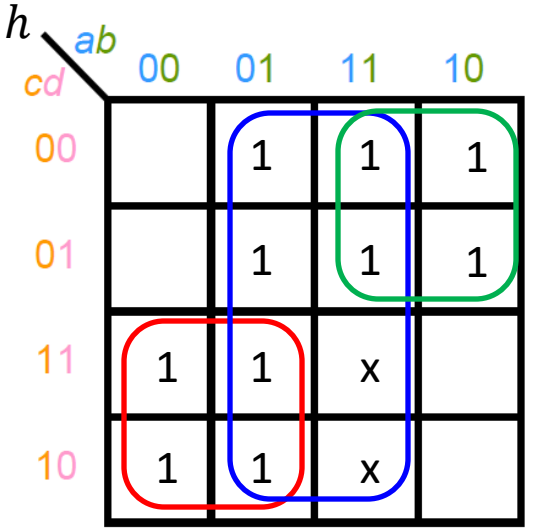
Common mistake: Copy wrongly and DeMorgan Theorem

Exercise

Which function(s) might have a timing hazard problem?
How to eliminate the hazard?



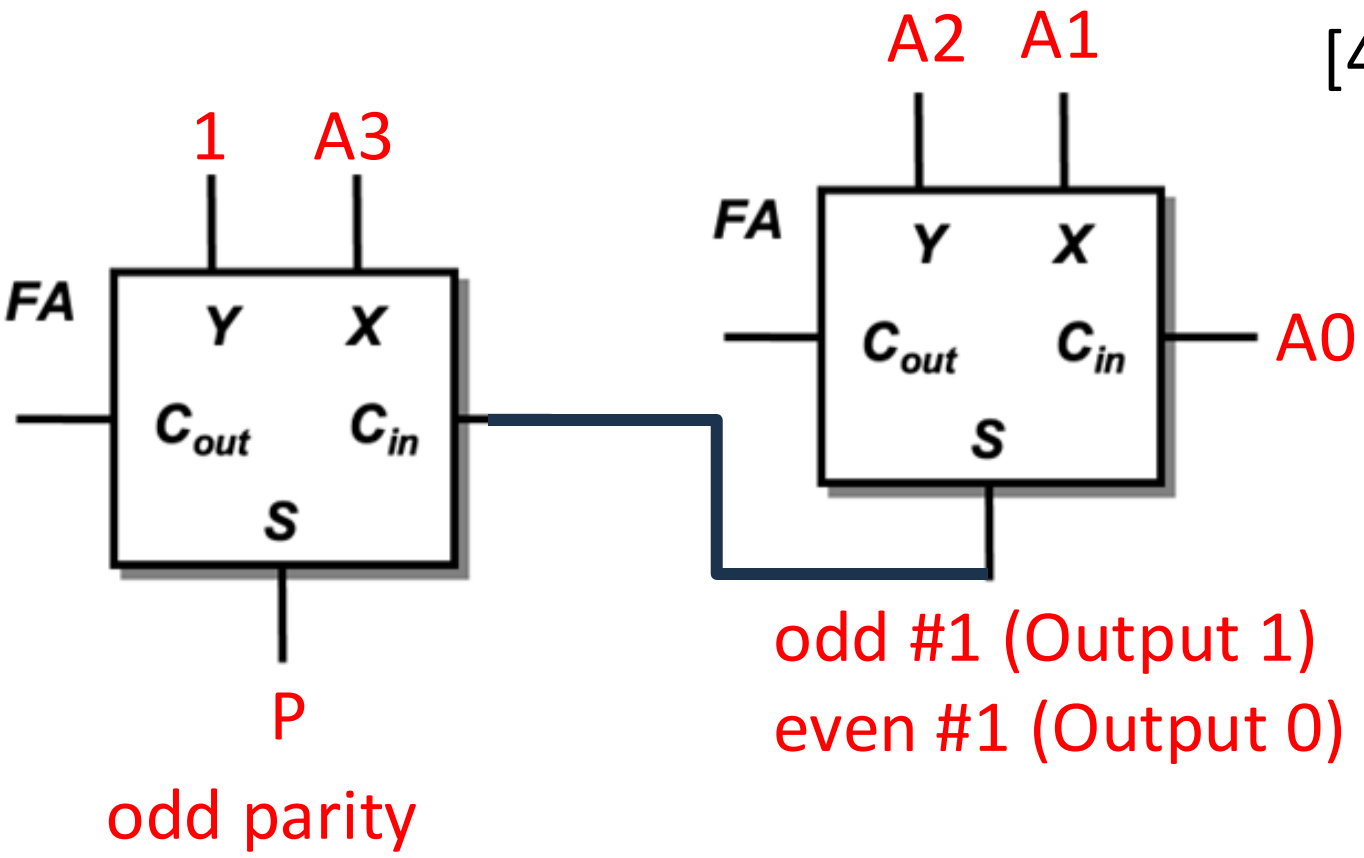




Test 2 - Question 4

(a) Design a functional block (FCB) to generate an odd parity (P) bit from 4-bit data (A3, A2, A1, A0) using only two 1-bit full adders (FAs).

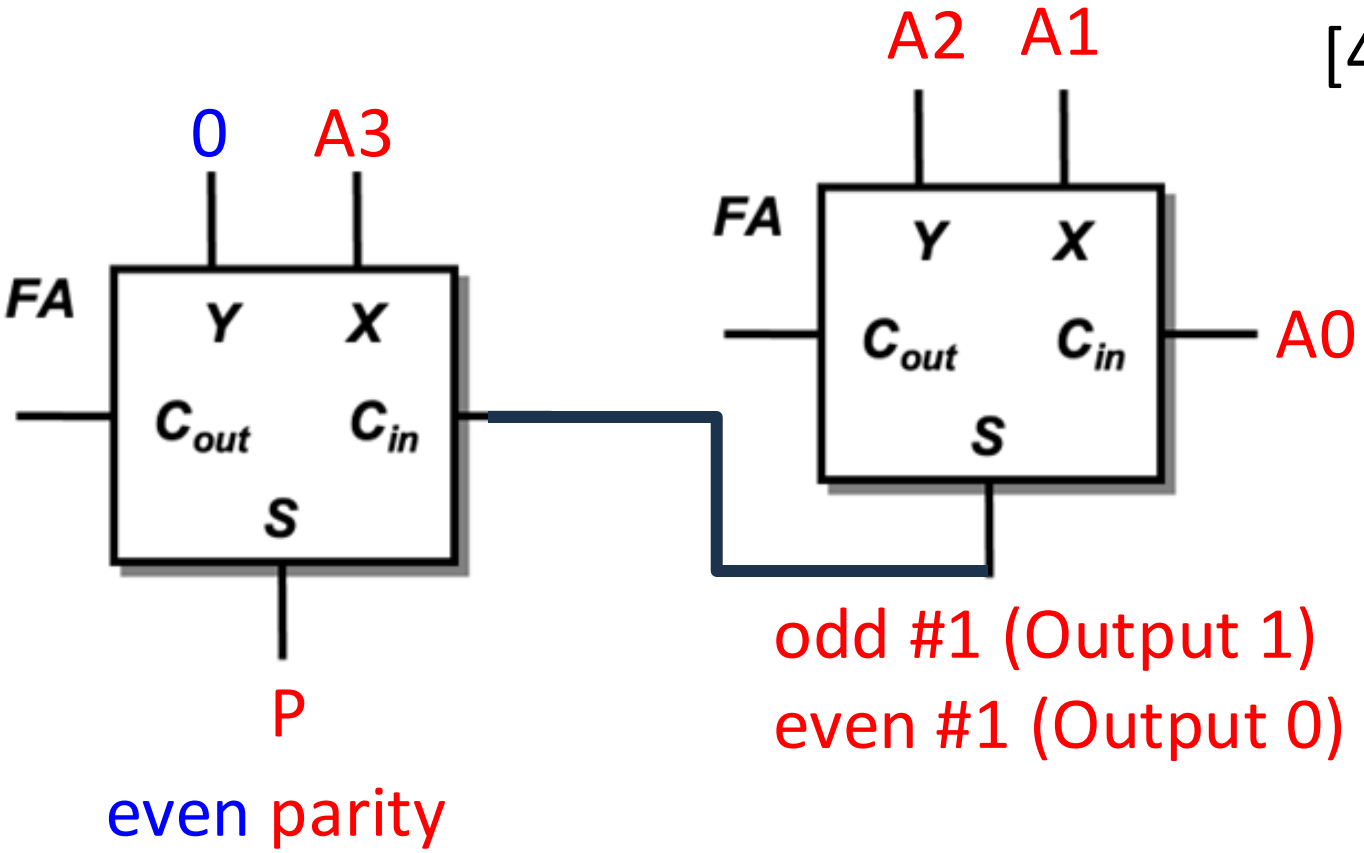
[4 marks]



Test 2 - Question 4

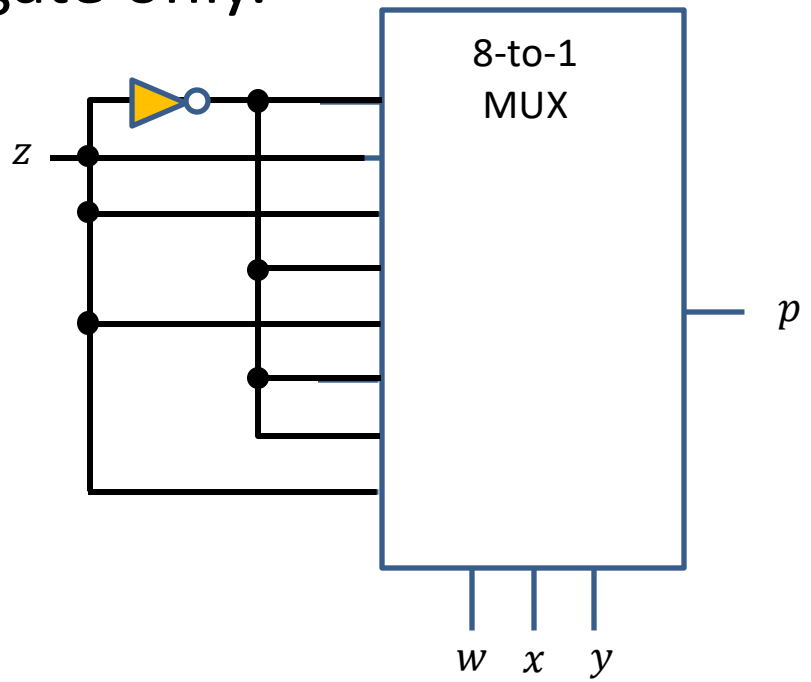
(a) Design a functional block (FCB) to generate an even parity (P) bit from 4-bit data (A3, A2, A1, A0) using only two 1-bit full adders (FAs).

[4 marks]



Exercise

Design a circuit to generate an odd parity (*p*) for a 4-bit data (*w*, *x*, *y*, *z*) using one 8-to-1-line MUX and one NOT gate only.



w	x	y	z	p
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

x

cd \ ab	00	01	11	10
00	0	1	x	0
01	0	x	1	0
11	1	x	0	x
10	x	1	x	x

y

cd \ ab	00	01	11	10
00	1	x	0	x
01	1	1	0	0
11	1	x	1	x
10	0	0	0	1

z

cd \ ab	00	01	11	10
00	1	0	0	x
01	1	0	1	1
11	0	0	0	0
10	0	1	1	x

x'

cd \ ab	00	01	11	10
00	0	1	x	0
01	0	x	1	0
11	1	x	0	x
10	x	1	x	x

y'

cd \ ab	00	01	11	10
00	1	x	0	x
01	1	1	0	0
11	1	x	1	x
10	0	0	0	1

z'

cd \ ab	00	01	11	10
00	1	0	0	x
01	1	0	1	1
11	0	0	0	0
10	0	1	1	x

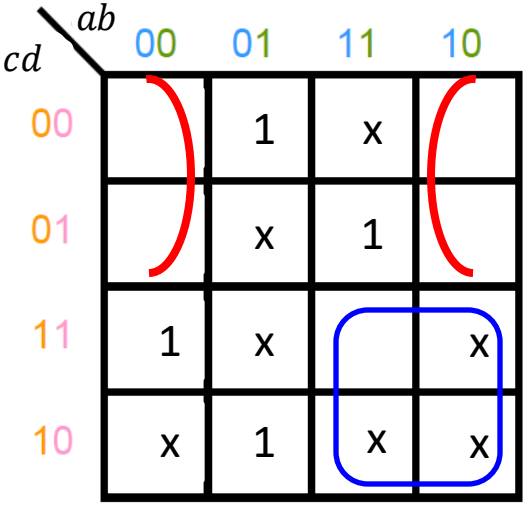
Test 2 – Question 3

$x(a,b,c,d) = \Sigma m(3,4,6,13) + \Sigma d(2,5,7,10,11,12,14)$

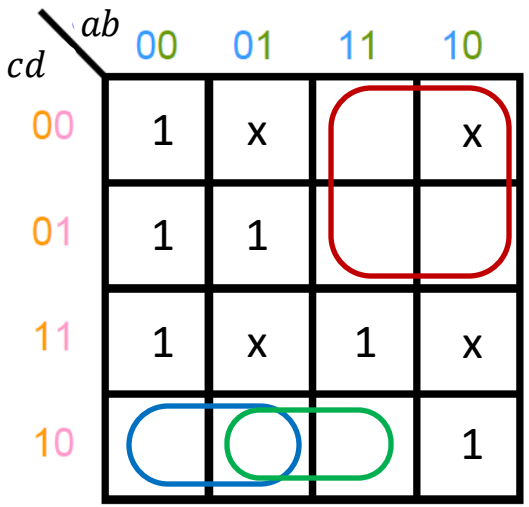
$y(a,b,c,d) = \Sigma m(0,1,3,5,10,15) + \Sigma d(4\ 7, 18\ 11)$

$z(a,b,c,d) = \Pi M(2,3,4,5,7,11,12,15)\Pi d(8,10)$

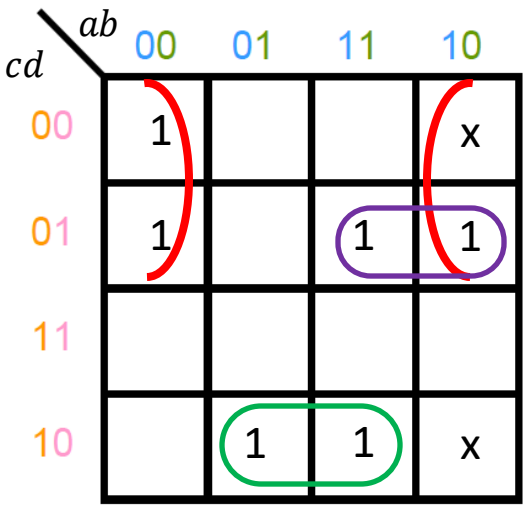
x'



y'



z



$x' = b'c' + ac$

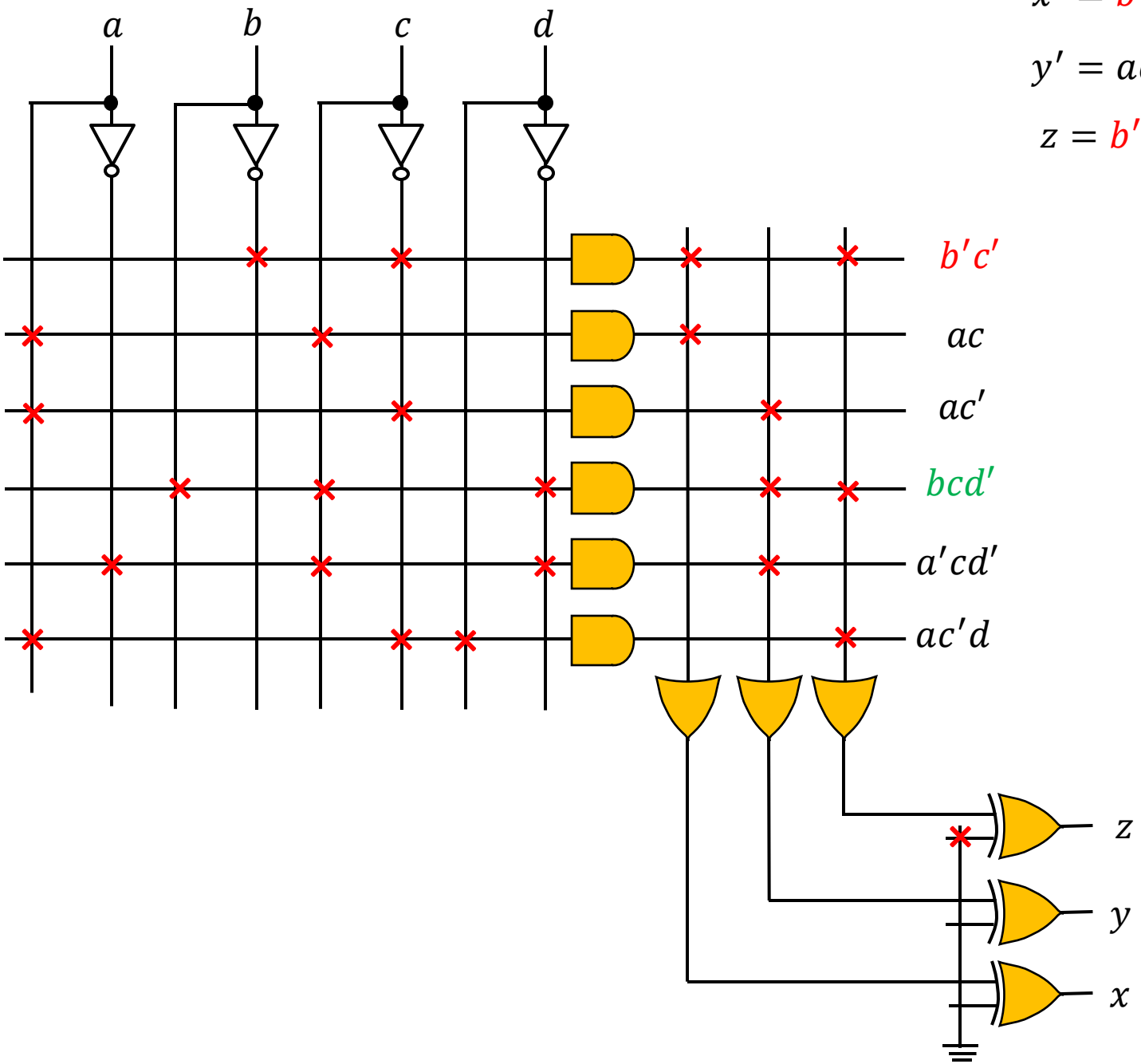
$y' = ac' + bcd' + a'cd'$

$z = b'c' + bcd' + ac'd$

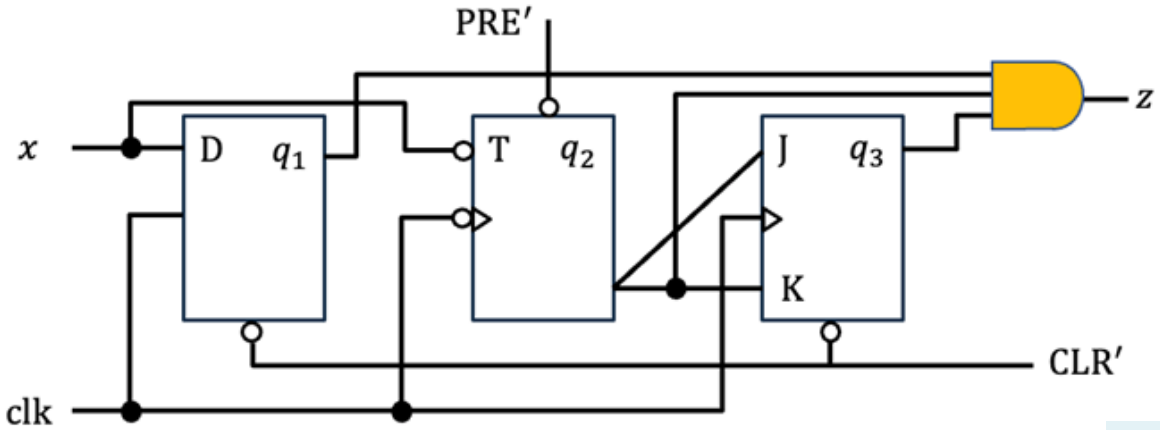
$$x' = b'c' + ac$$

$$y' = ac' + bcd' + a'cd'$$

$$z = b'c' + bcd' + ac'd$$



Test 2 – Question 1 (Past Year Exam Q)

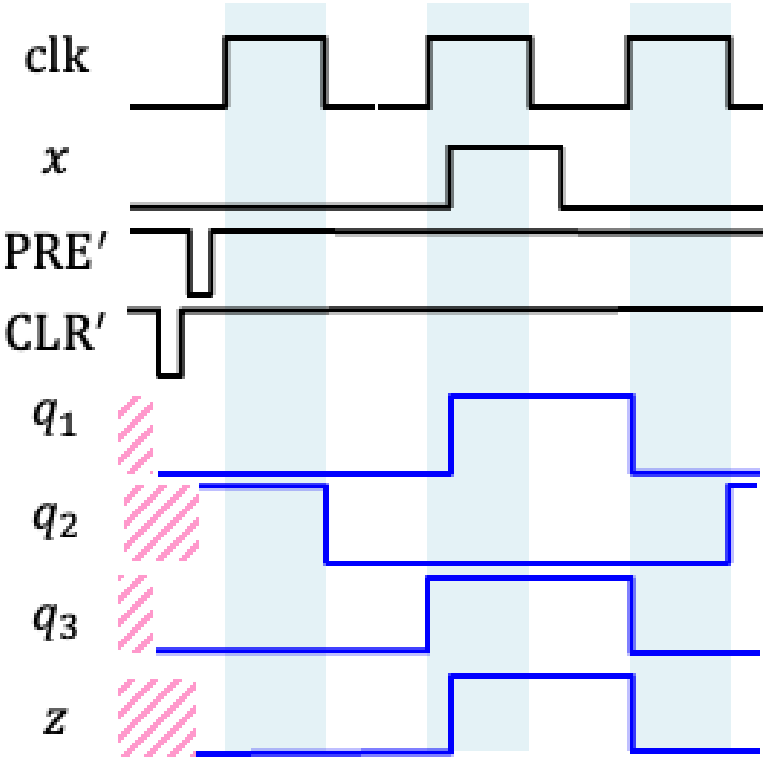


$$D = x$$

$$T = x'$$

$$J = K = q_2'$$

$$z = q_1 q_2' q_3$$



Test 2 – Question 3

Given the following VHDL code. Work out the truth table and specify the function of the circuits.

```
architecture Behavior of function1 is
signal s1: std_logic;
begin
      process (a, b)
      begin
     if a = '1' then
          s1 <= '1';
     elsif rising_edge(b) then
          s1 <= s1;
     elsif falling_edge(b) then
          if x = '0' then
               s1 <= s1;
          else
               s1 <= not s1;
          end if;
      end if;
z <= s1;
end process;
end Behavior;
```

Inputs: a, b, x

Output: z

a	b	x	s1	z
1	x	x	1	1
0	↑, 0 , 1	x	s1	z
0	↓	0	s1	z
0	↓	1	s1'	z'

Asynchronous active high preset input

Negative edge-triggered T-FF

Exercise (Past Year Question)

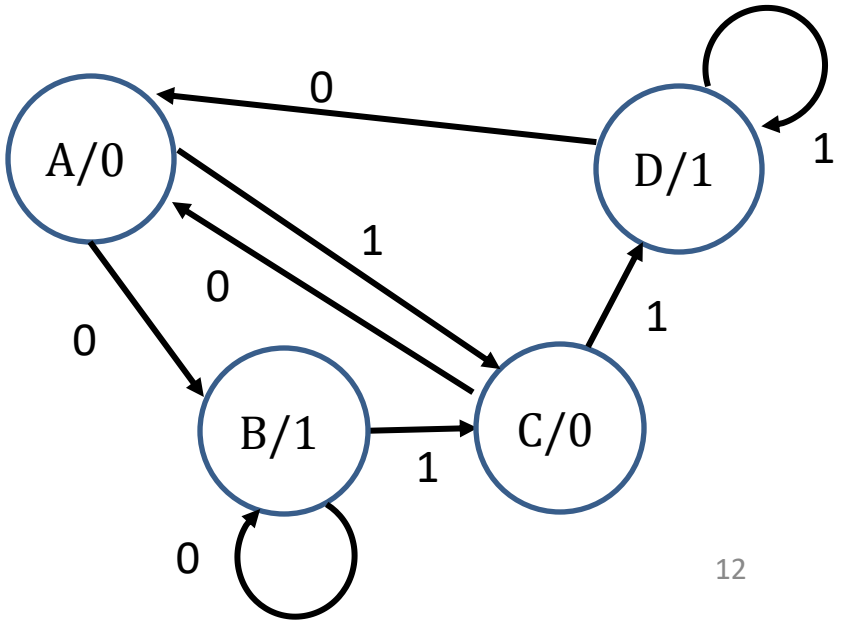
Design a Moore machine using D-FFs with 1 input x and 1 output *z* such that *z* = 1 if *x* has been '1' or '0' consecutively for two or more clock times. Provide the state diagram and the Boolean functions of the flip-flops' inputs and the circuit output. Draw the circuit diagram clearly. [10 marks]

A: First '0'

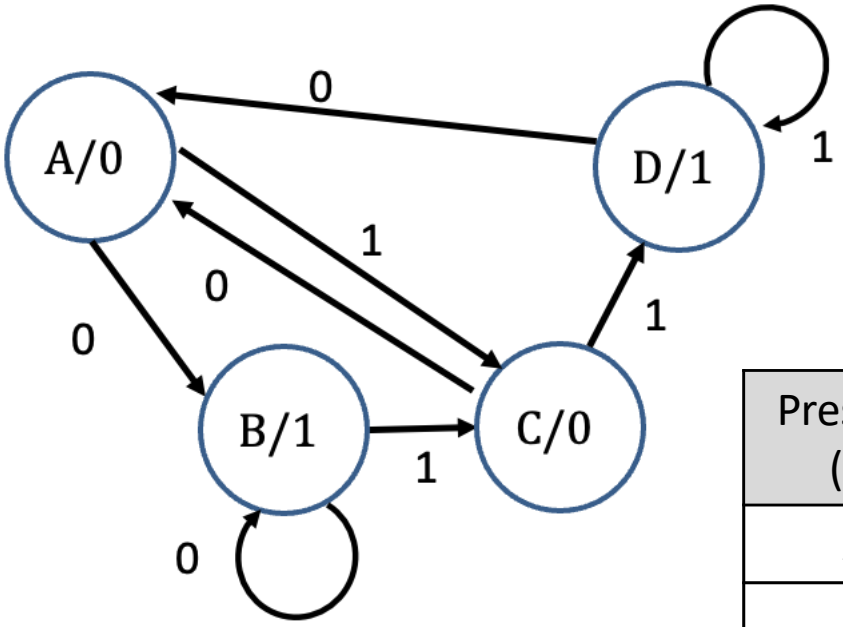
B: Second "00", output 1

C: First '1'

D: Second "11", output 1

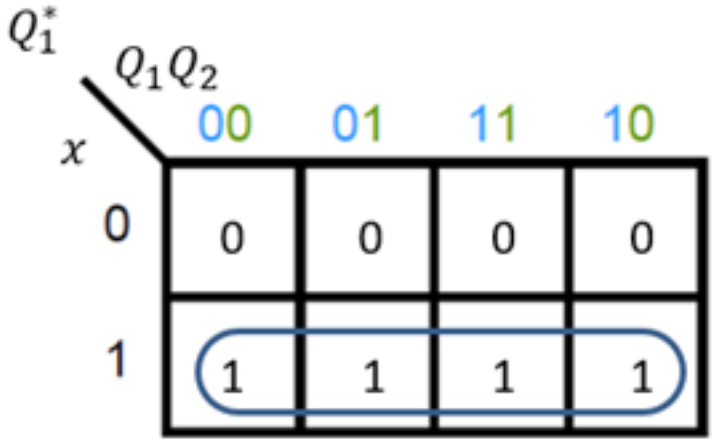


Exercise

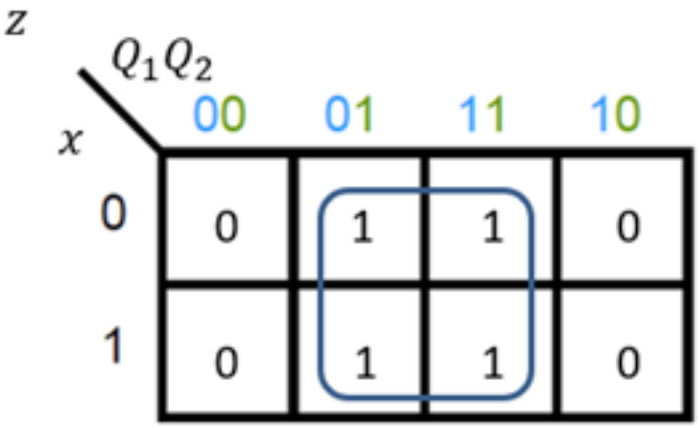


Present State (Q1 Q2)	Input x	Present Output z	Next State Q1* Q2*
A (0 0)	0	0	0 1
A (0 0)	1	0	1 0
B (0 1)	0	1	0 1
B (0 1)	1	1	1 0
C (1 0)	0	0	0 0
C (1 0)	1	0	1 1
D (1 1)	0	1	0 0
D (1 1)	1	1	1 1

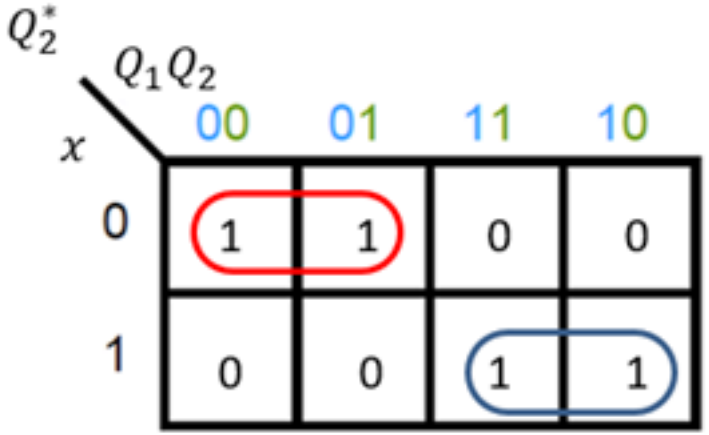
Exercise



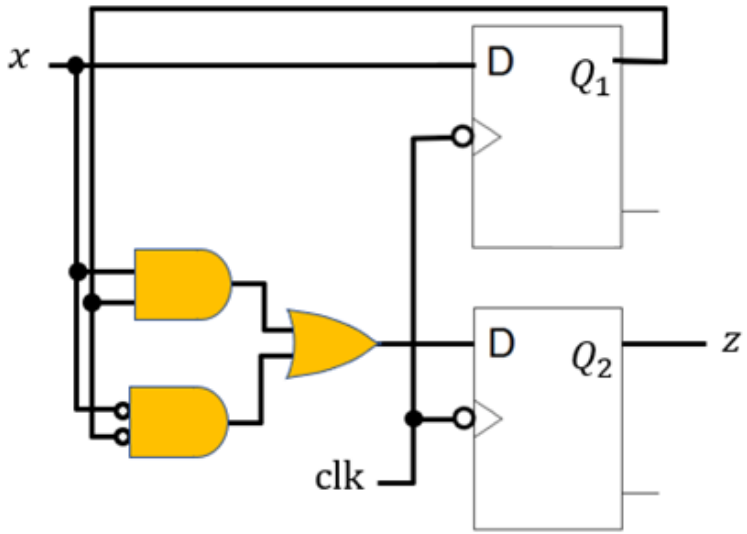
$$D_1 = Q_1^* = x$$



$$z = Q_2$$



$$D_2 = Q_2^* = xQ_1 + x'Q_1'$$

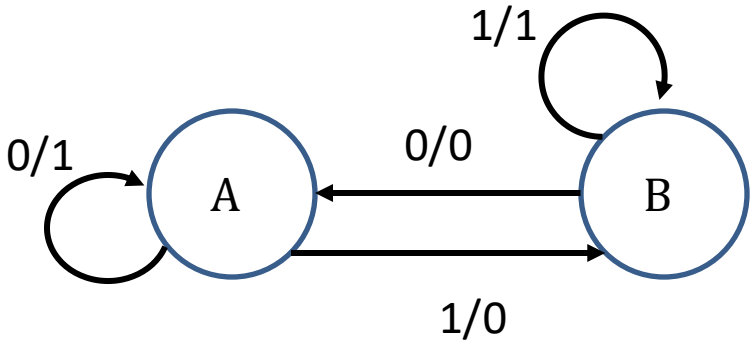


Exercise

Design the same sequence detector using a Mealy machine with T-FFs. Provide the state diagram and the Boolean functions of the flip-flops' inputs and the circuit output. A circuit diagram is not needed. [7 marks]

A: Reset to 1st zero *if next input is 0, remains at A output 1 else B

B: one '1' is detected *if next input is 1, remains at B output 1 else A



Present State (Q)	Input X	Next state Q^*	Output Z
A (0)	0	0	1
A (0)	1	1	0
B (1)	0	0	0
B (1)	1	1	1

$$T = xQ' + Qx'$$

$$z = Q'x' + Qx$$

```
        if (Bin = "01") then
                s1 <= s1(1 downto 0) & Cin;
            elsif (Bin = "10") then
                s1 <= Din & s1(2 downto 1);
            elsif (Bin = "11") then
                s1 <= Ain;
            end if;
        end if;
Eout <= s1;
end process;
```

Asynchronous active-high reset input

Negative edge-triggered

3-bit bidirectional register

Bin "01" shift left

Bin "10" shift right

Bin "11" parallel load

Bin "00" HOLD

Inputs						Signal	Output
Ain (3-bits)	Bin (2-bit)	Cin	Din	clk	rst	s1 (3-bit)	Eout (3-bit)
xxx	xx	x	x	x	1	000	000
xxx	xx	x	x	↑, 0 , 1	0	s1	Eout
xxx	01	Cin	Din	↓	0	s1(1)s1(0)Cin	E(1)E(0)Cin
xxx	10	Cin	Din	↓	0	Dins1(2)s1(1)	DinE(2)E(1)
A(2)A(1)A(0)	11	Cin	Din	↓	0	A(2)A(1)A(0)	A(2)A(1)A(0)
xxx	00	x	x	↓	0	s1	Eout

Exercise (Past Year Question)

count from 12 to 68 (*e.g.*, 23 in decimals equivalent to 0010 0011 in BCD 8421). Note that the clear (CLR) and load (LOAD) are synchronous inputs.