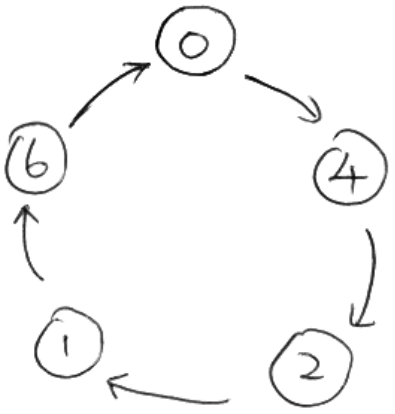
EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 10

Q1. All the unused states are treated as don't care condition.

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

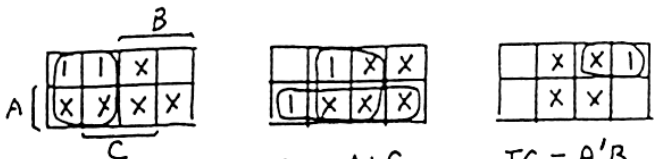
JK Excitation Table



P.S.			N.S.			FFA		FFB		FFC	
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	1	1	0	1	X	1	X	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	1	0	X	1	1	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

A B C	JA KA	JB KB	JC KC
0 0 0	1 X	0 X	0 X
1 0 0	X 1	1 X	0 X
0 1 0	0 X	X 1	1 X
0 0 1	1 X	1 X	X 1
1 1 0	X 1	X 1	0 X

$d(A,B,C) = \Sigma(3,5,7)$



$JA = B'$ $\quad JB = A+C$ $\quad JC = A'B$

$KA = KB = KC = 1$ by inspection

$011 \rightarrow 000$ $\quad 101 \rightarrow 010$ $\quad 111 \rightarrow 000$

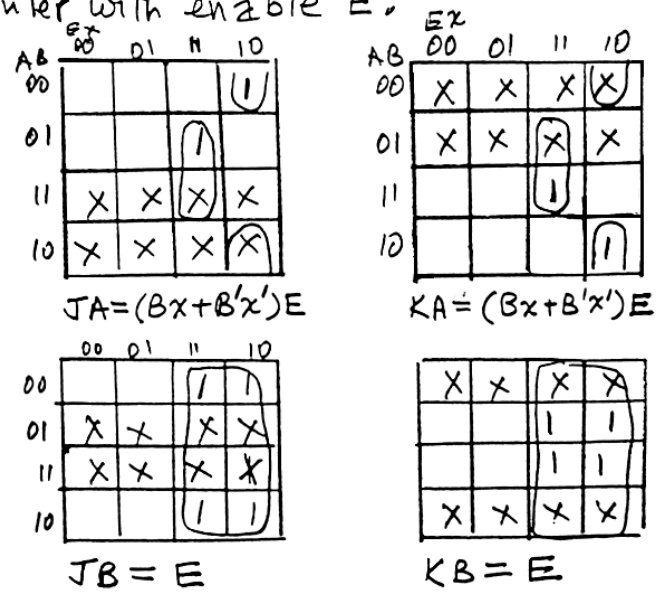
(self-starting)

P.S.			B'	1	A+C	1	A'C	1	NS		
A	B	C	JA	KA	JB	KB	JC	KC	A	B	C
0	1	1	0	1	1	1	1	10	0	0	0
1	0	1	1	1	1	1	0	1	0	1	0
1	1	1	0	1	1	1	0	1	0	0	0

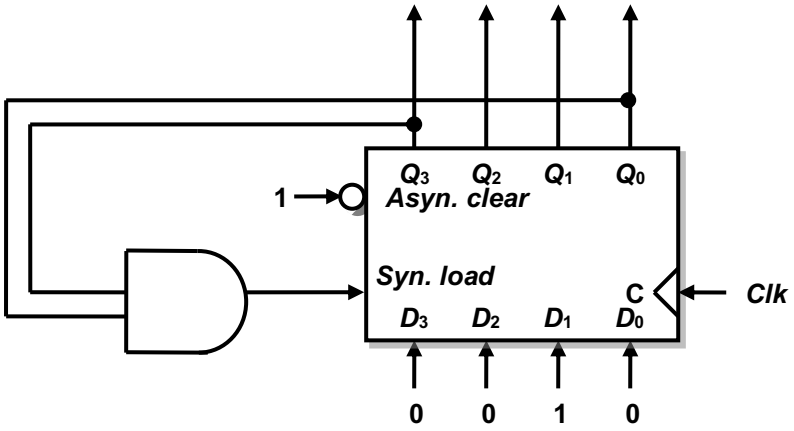
Q2.

Binary up-down counter with enable E.

P.S		Inps	N.S		FF Inps			
A	B	E	X	A	B	JA	KA	JB	KB
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1



Q3



Q4

Inputs		**Internal signal**	**Output**
rst	**clk**	**tmp**	**Q**
1	X	0000	0000
0	0, 1, ↓	X	Q
0	↑	0000	1000
0	↑	1000	1100
0	↑	1100	1110
0	↑	1110	1111
0	↑	1111	0111
0	↑	0111	0011
0	↑	0011	0001
0	↑	0001	0000

- 4-bit Johnson Ring Counter
- Positive-edge triggered
- Asynchronous active-high reset input