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Student Name: _____

Student ID: _____

EE2000 Logic Circuit Design

Mid-Term Test 1 (Semester A 2024/25)

Instructions:

1. You are responsible for receiving the exam paper, **hand-writing your name and SID** and returning it to the examiner in the hall.

2. Total time: **60 min**

3. This paper consists of **5** questions. Answer **ALL** questions in the space given after each question.

4. Please show all steps or else marks will be deducted.

5. **Remain seated** until the end of the test. You are not allowed to leave the hall earlier.

*This is a **closed-book** examination.*

No materials or aids are allowed during the whole examination. If any unauthorized materials or aids are found on a student during the examination, the student will be subject to disciplinary action.

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Summary of Properties of Boolean Algebra

Commutative	$a + b = b + a$	$ab = ba$
Associative	$a + (b + c) = (a + b) + c$	$a(bc) = (ab)c$
Identity	$a + 0 = a$	$a(1) = a$
Null	$a + 1 = 1$	$a(0) = 0$
Complement	$a + a' = 1$	$a(a') = 0$
Idempotency	$a + a = a$	$a(a) = a$
Involution	$(a')' = a$	
Distributive	$a(b + c) = ab + ac$	$a + bc = (a + b)(a + c)$
Adjacency	$ab + ab' = a$	$(a + b)(a + b') = a$
Simplification	$a + a'b = a + b$	$a(a' + b) = ab$
DeMorgan	$(a + b)' = a'b'$	$(ab)' = a' + b'$
Absorption	$a + ab = a$	$a(a + b) = a$
Consensus	$ab + a'c + bc = ab + a'c$	

Decimal Numbers	8421	2421	Excess-3	Gray Code
0	0000	0000	0011	0000
1	0001	0001	0100	0001
2	0010	0010	0101	0011
3	0011	0011	0110	0010
4	0100	0100	0111	0110
5	0101	1011	1000	0111
6	0110	1100	1001	0101
7	0111	1101	1010	0100
8	1000	1110	1011	1100
9	1001	1111	1100	1101

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QUESTION 1

Simplify the Boolean function of the given logic circuit using Boolean algebra in minimum SOP expression. Please write each step clearly.

$$f(a, b, c) = [(b + c')(a' + bc)]'$$

(5 marks)

$$= (b + c')' + (a' + bc)'$$
$$= b'c + a(bc)'$$
$$= b'c + a(b' + c')$$
$$= b'c + ab' + ac'$$
$$= b'c + ac'$$

QUESTION 2

Write the architecture declaration (architecture name "Behavior") of the following VHDL code to implement the output function $f(w, x, y, z) = wx' + yz$ using a minimum number of NAND OPERATOR only and using intermediate signals (s1, s2, etc.) for the output of each NAND OPERATOR.

```
library ieee;
use ieee.std_logic_1164.all;

entity logic_c is
        port(
                w,x,y,z: in std_logic;
                f: out std_logic);
end logic_c;
```

(8 marks)

```
architecture Behavior of logic_c is
signal s1, s2, s3 : std_logic;
begin
    s1 <= x NAND x;
    s2 <= w NAND s1;
    s3 <= y NAND z;
    f <= s2 NAND s3;
end Behavior;
```

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QUESTION 3

Student A wants to design a combinational circuit for a 4-bit Gray code (ABCD) to BCD-2421 (WXYZ) converter. Draw the truth table and simplify the Boolean functions of outputs X and Y using K-map and express them in minimum SOP expressions.

(13 marks)

Decimal digit	Input (Gray code)				Minterm	Output (2421 code)			
	A	B	C	D		W	X	Y	Z
0	0	0	0	0	m_0	0	0	0	0
1	0	0	0	1	m_1	0	0	0	1
2	0	0	1	1	m_3	0	0	1	0
3	0	0	1	0	m_2	0	0	1	1
4	0	1	1	0	m_6	0	1	0	0
5	0	1	1	1	m_7	1	0	1	1
6	0	1	0	1	m_5	1	1	0	0
7	0	1	0	0	m_4	1	1	0	1
8	1	1	0	0	m_{12}	1	1	1	0
9	1	1	0	1	m_{13}	1	1	1	1
Unused	X	X	X	X	m_8	X	X	X	X
Unused	X	X	X	X	m_9	X	X	X	X
Unused	X	X	X	X	m_{10}	X	X	X	X
Unused	X	X	X	X	m_{11}	X	X	X	X
Unused	X	X	X	X	m_{14}	X	X	X	X
Unused	X	X	X	X	m_{15}	X	X	X	X

$X(A, B, C, D)$

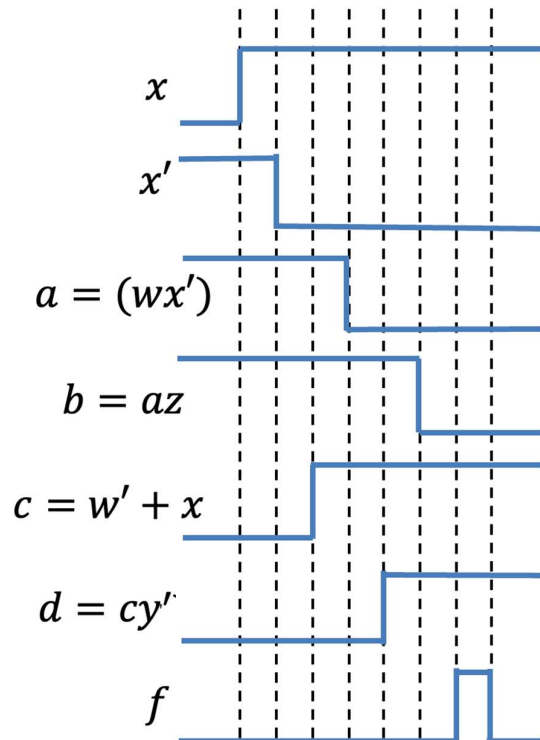$X(A, B, C, D) = BC' + BD'$

$Y(A, B, C, D)$

$Y(A, B, C, D) = A + CD + B'C$

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QUESTION 4

Given the following combinational circuit, work out the timing diagram to identify the presence of any timing hazard when the input condition changes from $(w, x, y, z) = (1, 0, 0, 1)$ to $(1, 1, 0, 1)$. Assume that the propagation delay for NOT gate is $\Delta\tau$, and other gates is $2\Delta\tau$.
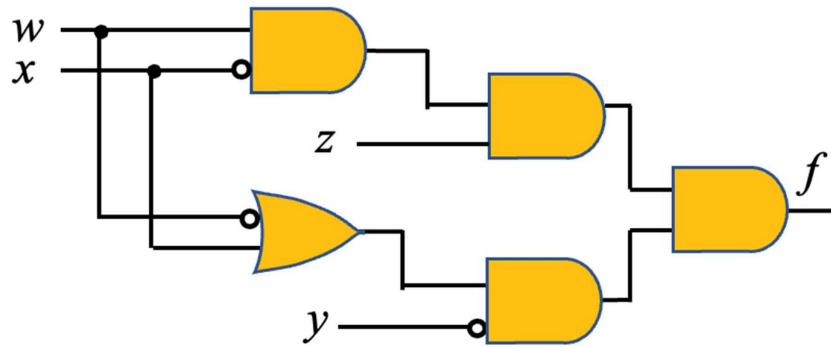
(7 marks)

Static-0 hazard

QUESTION 5

Consider odd parity, if a Hamming code of 110100110 is received, determine whether single error bit is present, work out the correct Hamming code, if any, and the original data code.

(7 marks)

$c_1 = (H9, H7, H5, H3, H1) = (1, 0, 0, 1, 0) = 1$
$c_2 = (H7, H6, H3, H2) = (0, 1, 1, 1) = 0$
$c_3 = (H7, H6, H5, H4) = (0, 1, 0, 0) = 0$
$c_4 = (H9, H8) = (1, 1) = 1$
$c_4 c_3 c_2 c_1 = (1001)_2 = 9$ (error bit)

Correct data code: 010100110
Original data code: 00101