EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 8

1. (a) Given the following VHDL code, specify which functional block is being implemented and its function in detail.

```
entity FSB is
    port ( A: in std_logic;
           D0, D1: out std_logic);
end FSB;

architecture Behavioral of FSB is
begin
    D0 <= NOT A;
    D1 <= A;
end Behavioral;
```

(b) Given the following VHDL code that uses FSB in (a) as a component, specify which functional block is being implemented and its function in detail.

```
entity func1 is
    port ( A0, A1: in std_logic;
           D0, D1, D2, D3: out std_logic);
end func1;

architecture Behavioral of func1 is

component FSB is
    port (A: in std_logic;
          D0: out std_logic;
          D1: out std_logic);
end component;

signal SigA0: std_logic_vector(1 downto 0);
signal SigA1: std_logic_vector(1 downto 0);

begin
    uut1: FSB port map(A0, SigA0(0), SigA0(1));
    uut2: FSB port map(A1, SigA1(0), SigA1(1));

    D0 <= SigA1(0) and SigA0(0);
    D1 <= SigA1(0) and SigA0(1);
    D2 <= SigA1(1) and SigA0(0);
    D3 <= SigA1(1) and SigA0(1);
end Behavioral;
```

2. (a) Given the following VHDL code, specify which functional block is being implemented and its function in detail.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity FSB is
    port ( S: in std_logic_vector (2 downto 0);
           Q: out std_logic_vector (7 downto 0));
end FSB;

architecture Behavioral of FSB is
begin
    process (S)
    begin
        case S is
            when "000" => Q <= "00000001";
            when "001" => Q <= "00000010";
            when "010" => Q <= "00000100";
            when "011" => Q <= "00001000";
            when "100" => Q <= "00010000";
            when "101" => Q <= "00100000";
            when "110" => Q <= "01000000";
            when "111" => Q <= "10000000";
            when others => null;
end Behavioral;
```

(b) Draw the logic circuit being implemented by the following VHDL codes.

```
entity func1 is
    port ( x, y, z: in std_logic;
           F1, F2: out std_logic);
end func1;

architecture Behavioral of func1 is

component FSB is
    port (S: in std_logic_vector (2 downto 0);
          Q: out std_logic_vector (7 downto 0));
end component;

signal S: std_logic_vector(2 downto 0);
signal Q: std_logic_vector(7 downto 0);

begin
    uut: FSB port map(S, Q);
    S <= x & y & z;
    F1 <= Q(0) or Q(5) or Q(7);
    F2 <= Q(1) or Q(3) or Q(4);
end Behavioral;
```

3. Write the entity and architecture declaration for a decimal-to-gray code encoder module named DTG_encoder that has one 10-bit input named D_in and one 4-bit output named G_out.

4. Given the following VHDL code, specify which functional block is being implemented and its function in detail.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity func1 is
    port ( x, y: in std_logic;
           clk: in std_logic;
           a: in std_logic;
           z: out std_logic);
end func1;

architecture Behavioral of func1 is
signal tmp: std_logic;
begin
    process (x, y, clk, a)
    begin
        if (a = '1') then
            tmp <= '0';
        elsif (falling_edge(clk)) then
            if (x /= y) then
                tmp <=  x;
            elsif (x = '1' and y = '1') then
                tmp <= not tmp;
            end if;
        end if;
        z <= tmp;
        end process;
end Behavioral;
```