Student Name:	
Student ID:	

EE2000 Logic Circuit Design

Mid-Term Test 2 (Semester A 2024/25)

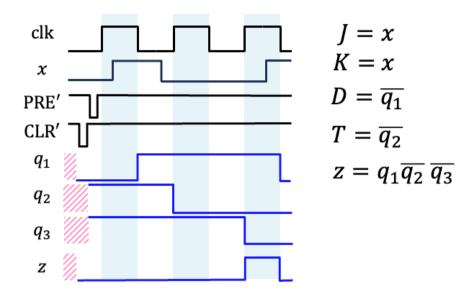
Instructions:

- 1. You are responsible for receiving the exam paper, **hand-writing your name and SID** and returning it to the examiner in the hall.
- 2. Total time: 60 min
- 3. This paper consists of **4** questions. Answer <u>ALL</u> questions in the space given after each question.
- 4. Please show all steps or else marks will be deducted.
- 5. **Remain seated** until the examiner allows you to leave at the end of the test. You are not allowed to leave the hall earlier.

This is a **closed-book** examination.

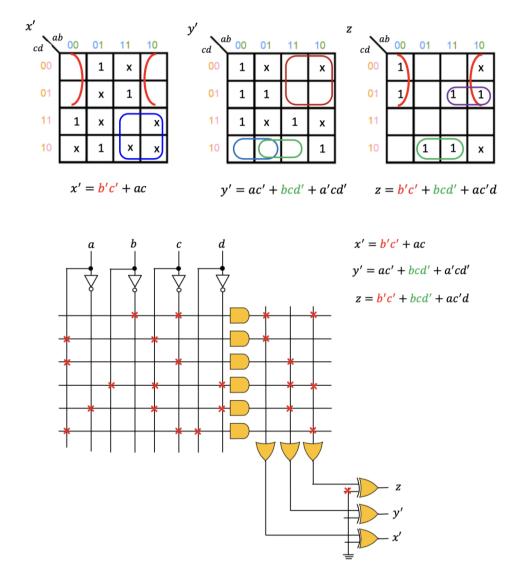
No materials or aids are allowed during the whole examination. If any unauthorized materials or aids are found on a student during the examination, the student will be subject to disciplinary action.

QUESTION 1



QUESTION 2

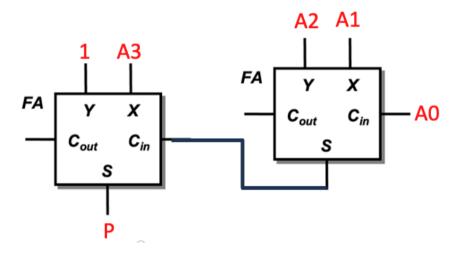
(13 marks)

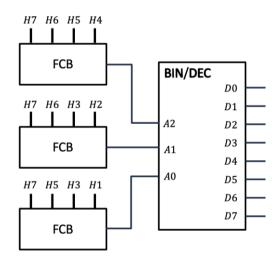


QUESTION 3

- Asynchronous active high preset/set input
- Falling/Negative/Trailing edge triggered T Flip-flops

QUESTION 4





- END -