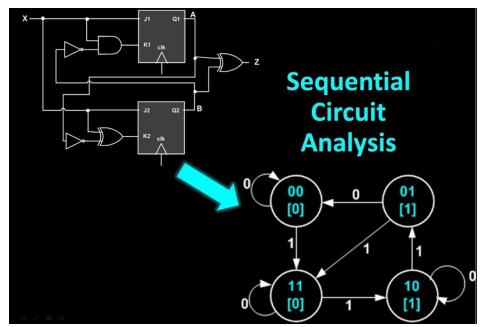
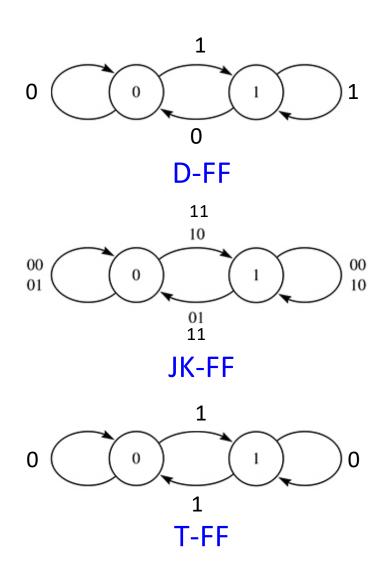
EE2000 Logic Circuit Design

Lecture 9 – Sequential Logic Circuit Design



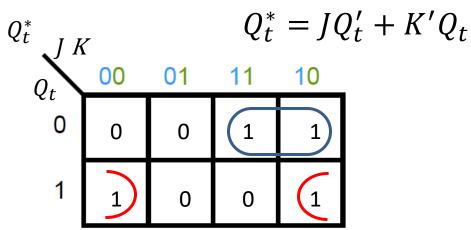
Other FFs

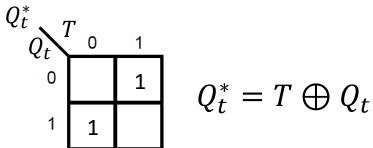
State diagram

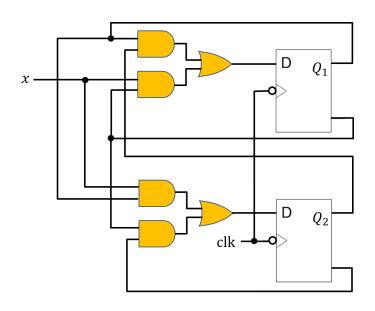


Characteristic equation

$$Q_t^* = D$$



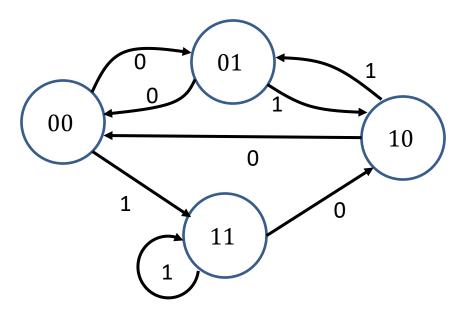




$$Q_1^* = D_1 = Q_1 Q_2 + x Q_1'$$

 $Q_2^* = D_2 = Q_1' Q_2' + x Q_1$

Present State	Input X				
$Q_1 \ Q_2$	0	1			
(0 0)	(0 1)	(1 1)			
(0 1)	(0 1) (0 0) (0 0)	(1 0)			
(1 0)	(0 0)	(0 1)			
(1 1)	(1 0)	(1 1)			



Design a Mealy machine to detect the sequence "111" (Overlapping)

In other words,

Design a system with one input x and one output z such that z = 1 if x has been 1 for at least three consecutive clock times.

х	0	1	1	0	1	1	1	0	1	1	1	1	1	0
\boldsymbol{Z}	0	0	0	0	0	0	1	0	0	0	1	1	1	0

x	0	1	1	0	1	1	1	0	1	1	1	1	1	0
Z	0	0	0	0	0	0	1	0	0	0	1	1	1	0

STEP 1: Determine what needs to be stored in memory and how to store them.

A: input is '0' *if next input is 0, remains at A else B

B: one '1' is detected *if next input is 0, back to A else C

C: two '1's are detected

* if next input is 0, back to A and output '0', else remains at C and output '1'

STEP 2: Work out the State Diagram

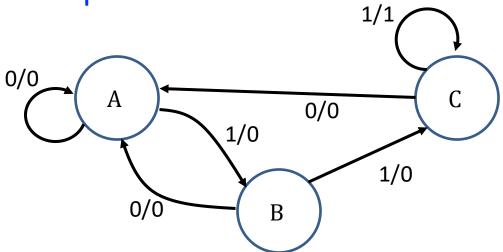
A: Input is '0' *if next input is 0, remains at A else B

B: one '1' is detected *if next input is 0, back to A else C

C: two '1's are detected

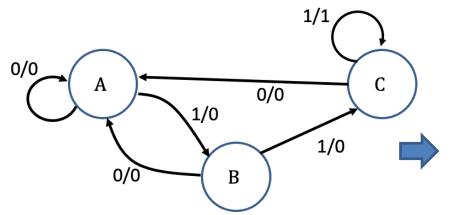
* if next input is 0, back to A and output '0',

else remains at C and output '1'



STEP 3: Work out the analysis table with assigned FFs

3 states \rightarrow 2 FFs (We use D-FFs in this example)



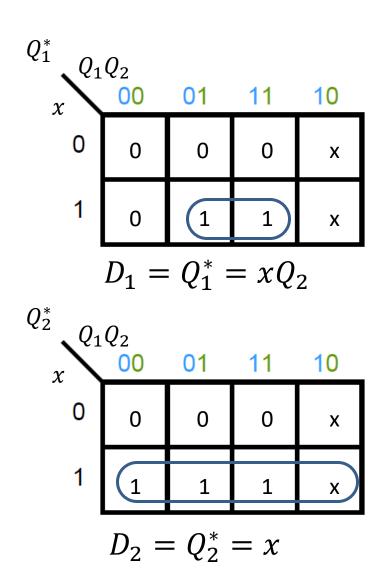
Present	Input	Next	state	Present
State (Q_1Q_2)	X	$\boldsymbol{Q_1^*}$	$\boldsymbol{Q_2^*}$	Output Z
A (0 0)	0	0	0	0
A (0 0)	1	0	1	0
B (0 1)	0	0	0	0
B (0 1)	1	1	1	0
(10)	Х	х	х	х
C (1 1)	0	0	0	0
C (1 1)	1	1	1	1

Assign State A:

 $Q_1 \rightarrow 0$ and $Q_2 \rightarrow 0$ etc

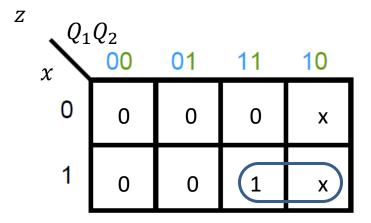
STEP 4: Work out D_1 and D_2

Present	Input	Next	State	
State (Q_1Q_2)	X	$oldsymbol{Q_1^*}$	$\boldsymbol{Q_2^*}$	Output Z
A (0 0)	0	0	0	0
A (0 0)	1	0	1	0
B (0 1)	0	0	0	0
B (0 1)	1	1	1	0
(10)	Х	х	X	Х
C (1 1)	0	0	0	0
C (1 1)	1	1	1	1



STEP 5: Work out *z*

Present	Input	Next	State	
State (Q_1Q_2)	X	$oldsymbol{Q_1^*}$	$\boldsymbol{Q_2^*}$	Output Z
A (0 0)	0	0	0	0
A (0 0)	1	0	1	0
B (0 1)	0	0	0	0
B (0 1)	1	1	1	0
(10)	Х	х	Х	х
C (1 1)	0	0	0	0
C (1 1)	1	1	1	1



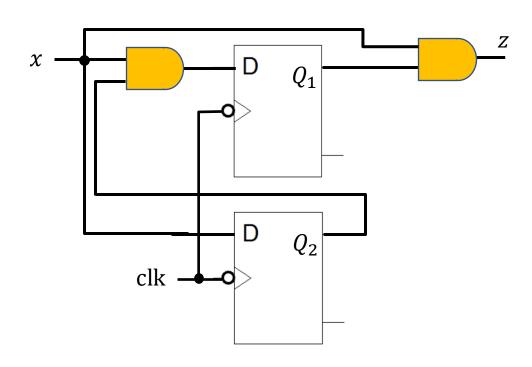
$$z = xQ_1$$

STEP 6: Draw the sequential logic circuits

$$D_1 = xQ_2$$

$$D_2 = x$$

$$z = xQ_1$$

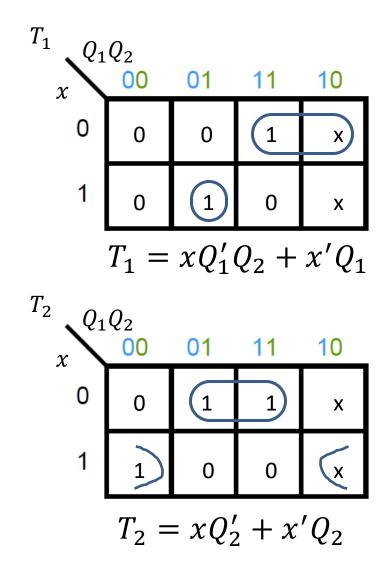


Use T FFs to design a Mealy machine to detect the sequence "111" (Overlapping)

Present State	Innut V	Next	State	Flip-	Flops	Output 7
(Q_1Q_2)	Input X	$\boldsymbol{Q_1^*}$	$\boldsymbol{Q_2^*}$	T_1	T_2	Output Z
A (0 0)	0	0	0	0	0	0
A (0 0)	1	0	1	0	1	0
B (O 1)	0	0	0	0	1	0
B (O 1)	1	1	1	1	0	0
(10)	х	х	Х	х	х	х
C (1 1)	0	0	0	1	1	0
C (1 1)	1	1	1	0	0	1

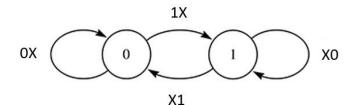
T	Q_{t+1}	$\overline{Q_{t+1}}$	State
0	Q_t	$\overline{Q_t}$	Hold
1	$\overline{Q_t}$	Q_t	Toggle

Present State	Input V	Flip-	Flops
(Q_1Q_2)	Input X	T_1	T_2
A (0 0)	0	0	0
A (0 0)	1	0	1
B (O 1)	0	0	1
B (O 1)	1	1	0
(10)	x	х	х
C (1 1)	0	1	1
C (1 1)	1	0	0

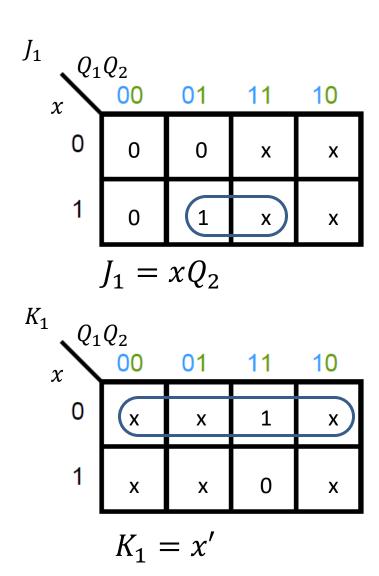


Use JK FFs to design a Mealy machine to detect the sequence "111" (Overlapping)

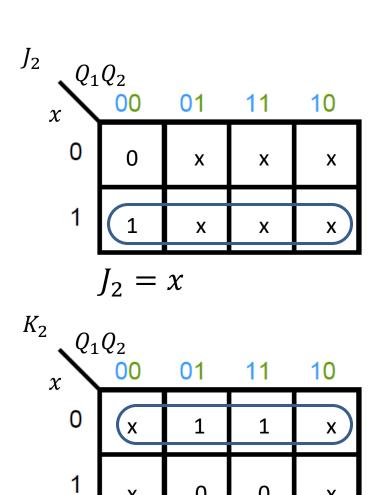
Present State	Input		ext ate	Flip-Flops			Output <i>Z</i>	
(Q_1Q_2)	X	$oldsymbol{Q_1^*}$	$\boldsymbol{Q_2^*}$	J_1	K_1	J_2	K_2	
A (0 0)	0	0	0	0	Х	0	Х	0
A (0 0)	1	0	1	0	х	1	х	0
B (0 1)	0	0	0	0	х	х	1	0
B (0 1)	1	1	1	1	х	х	0	0
(10)	Х	Х	X	х	х	х	Х	х
C (1 1)	0	0	0	х	1	х	1	0
C (1 1)	1	1	1	Х	0	Х	0	1



Present	Input		Flip-l	Flops	
State (Q_1Q_2)	X	J_1	K_1	J_2	K_2
A (0 0)	0	0	Х	0	Х
A (0 0)	1	0	Х	1	Х
B (0 1)	0	0	Х	X	1
B (0 1)	1	1	Х	X	0
(10)	Х	Х	Х	Х	Х
C (1 1)	0	Х	1	Х	1
C (1 1)	1	Х	0	Х	0



Present	Input		Flip-	Flops	
State (Q_1Q_2)	X	J_1	K_1	J_2	K_2
A (0 0)	0	0	Х	0	Х
A (0 0)	1	0	Х	1	Х
B (0 1)	0	0	Х	Х	1
B (0 1)	1	1	Х	Х	0
(10)	Х	Х	Х	Х	Х
C (1 1)	0	х	1	Х	1
C (1 1)	1	Х	0	Х	0



$$K_2 = x'$$

0

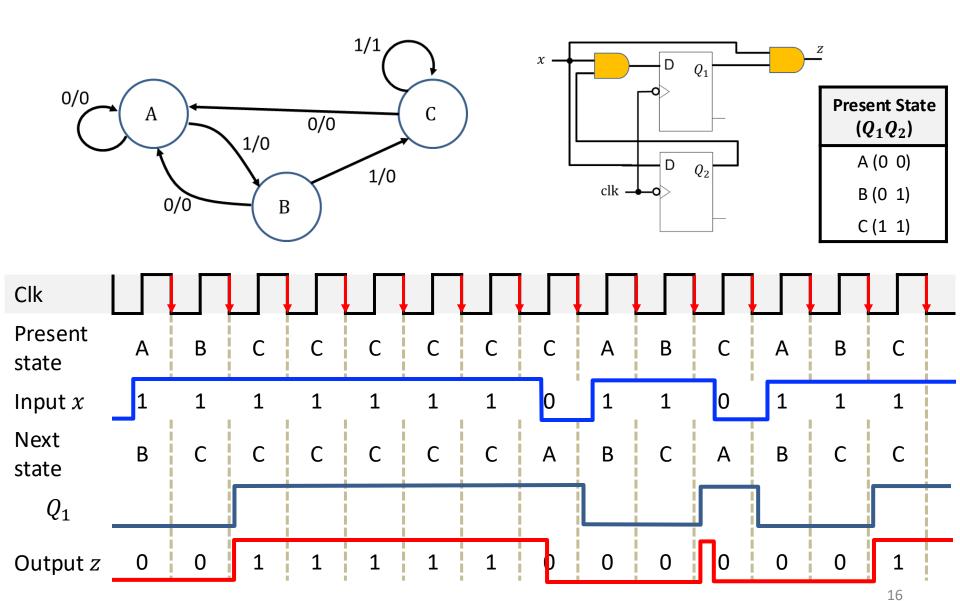
Χ

0

X

Exercise (Timing Diagram)

 $z = xQ_1$



Design a Moore machine to detect the sequence "11" or "000" (Overlapping)

In other words,

Design a system with one input x and one output z such that z = 1 if x has been 1 for at least two consecutive clock times or 0 for at least three consecutive clock times.

x	0	0	0	0	1	0	1	1	0	0	1	1	1	0
\boldsymbol{Z}		?	?	1	1	0	0	0	1	0	0	0	1	1

x	0	0	0	0	1	0	1	1	0	0	1	1	1	0
\boldsymbol{Z}			?	1	1	0	0	0	1	0	0	0	1	1

(Hint: 5 states)

A: Input is '0'

B: Second '0'

C: Third '0' output 1

D: First '1'

E: Second '1' output 1

D/0 0 A/0 E/1 0 B/0 C/1

^{*} if next input is 0, back to A and output '1',

Present State	Inp	ut X	Present	
	0	1	Output Z	
А	I	С	0	
В	В	I	0	
С	С	G	0	
D	I	С	1	
E	D	Е	1	
F	ı	С	1	
G	Е	F	1	
н	Н	Α	0	
I	Α	С	0	

Reduce the state table using partitioning method

$$P_0 = (A B C D E F G H I)$$

Group states based on same output

Present State	Inp	ut X	Present	
	0	1	Output Z	
Α	I	С	0	
В	В	I	0	
С	С	G	0	
н	Н	Α	0	
I	Α	С	0	
D	I	С	1	
E	D	Е	1	
F	I	С	1	
G	Е	F	1	

Reduce the state table using partitioning method

$$P_1 = (A B C H I)(D E F G)$$

A B C H I \rightarrow Output 0

D E F G \rightarrow Output 1

Present State	Inp	ut X	Present
	0	1	Output Z
А	I	С	0
В	В	I	0
н	Н	Α	0
I	Α	С	0
С	С	G	0
D	I	С	1
F	I	С	1
E	D	Е	1
G	Е	F	1

Reduce the state table using partitioning method

$$P_2 = (A B H I)(C)(D F)(E G)$$

Present State	Inp	ut X	Present	
	0	1	Output Z	
А	I	С	0	
I	Α	С	0	
В	В	I	0	
Н	Н	Α	0	
С	С	G	0	
D	I	С	1	
F	I	С	1	
E	D	Е	1	
G	Е	F	1	

Reduce the state table using partitioning method

$$P_3 = (A I)(B H)(C)(D F)(E)(G)$$

Present State	Inp	ut X	Present
	0	1	Output Z
A = I	А	С	0
B = H	В	Α	0
С	С	G	0
D = F	Α	С	1
E	D	Ε	1
G	Е	D	1

Reduce the state table using partitioning method

$$P_3 = (A I)(B H)(C)(D F)(E)(G)$$