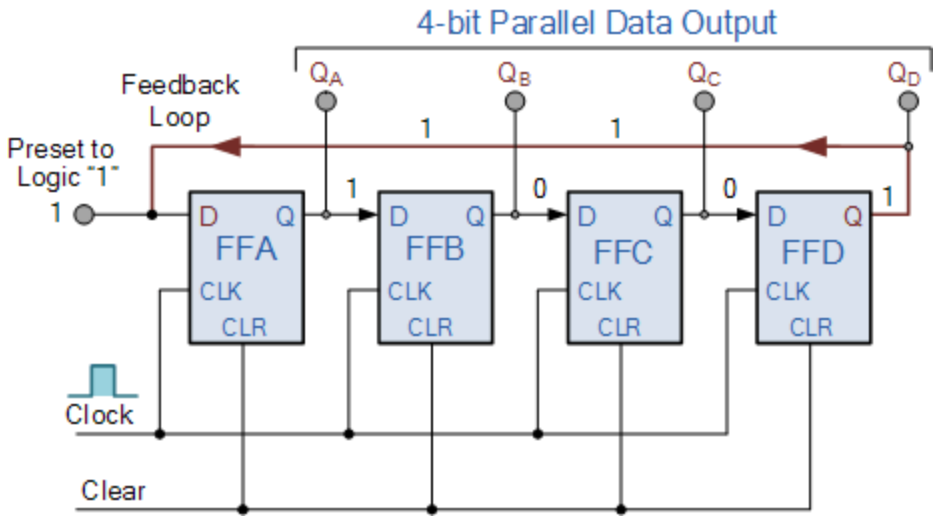
EE2000 Logic Circuit Design

Lecture 10 – Sequential Functional Blocks: Registers and Counters



Exercise

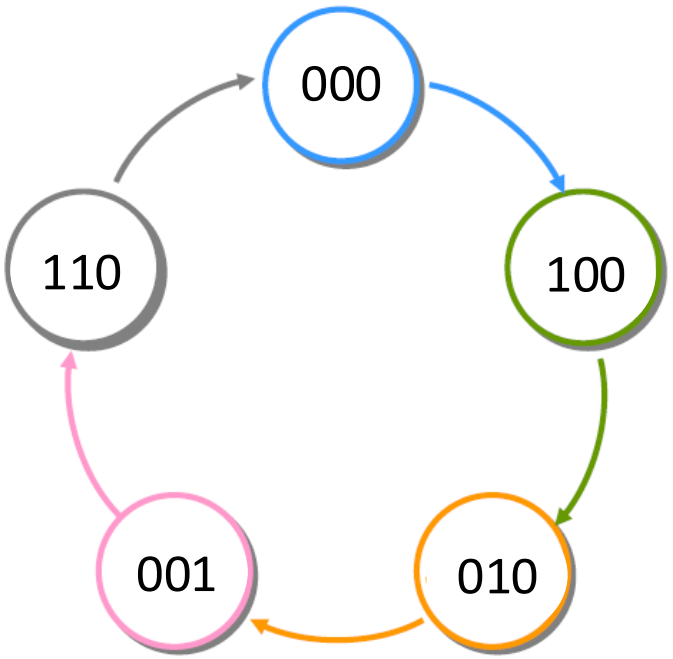
Use T FFs and logic gates to design a synchronous counter with counting sequence 0, 4, 2, 1, 6…

Step 1:

- States: 5 states → 3 flip-flops
- Largest number 6 → $(110)_2$ → 3 outputs
- Behavior: 000 → 100 → 010 → 001 → 110...

Exercise

STEP 2: Work out the State Diagram and Table



Present State			Next State		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	1	x	x	x
1	0	0	0	1	0
1	0	1	x	x	x
1	1	0	0	0	0
1	1	1	x	x	x

Exercise

STEP 3: Work out T_A, T_B, T_C

Present State			Next State			Flip-Flop		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	T_A	T_B	T_C
0	0	0	1	0	0	1	0	0
0	0	1	1	1	0	1	1	1
0	1	0	0	0	1	0	1	1
0	1	1	x	x	x	x	x	x
1	0	0	0	1	0	1	1	0
1	0	1	x	x	x	x	x	x
1	1	0	0	0	0	1	1	0
1	1	1	x	x	x	x	x	x

T_A Q_AQ_B Q_C

Q_C \ Q_AQ_B	00	01	11	10
0	1	0	1	1
1	1	x	x	x

$$T_A = Q'_B + Q_A$$

T_B Q_AQ_B Q_C

Q_C \ Q_AQ_B	00	01	11	10
0	0	1	1	1
1	1	x	x	x

$$T_B = Q_A + Q_B + Q_C$$

T_C Q_AQ_B Q_C

Q_C \ Q_AQ_B	00	01	11	10
0	0	1	0	0
1	1	x	x	x

$$T_C = Q'_A Q_B + Q_C$$

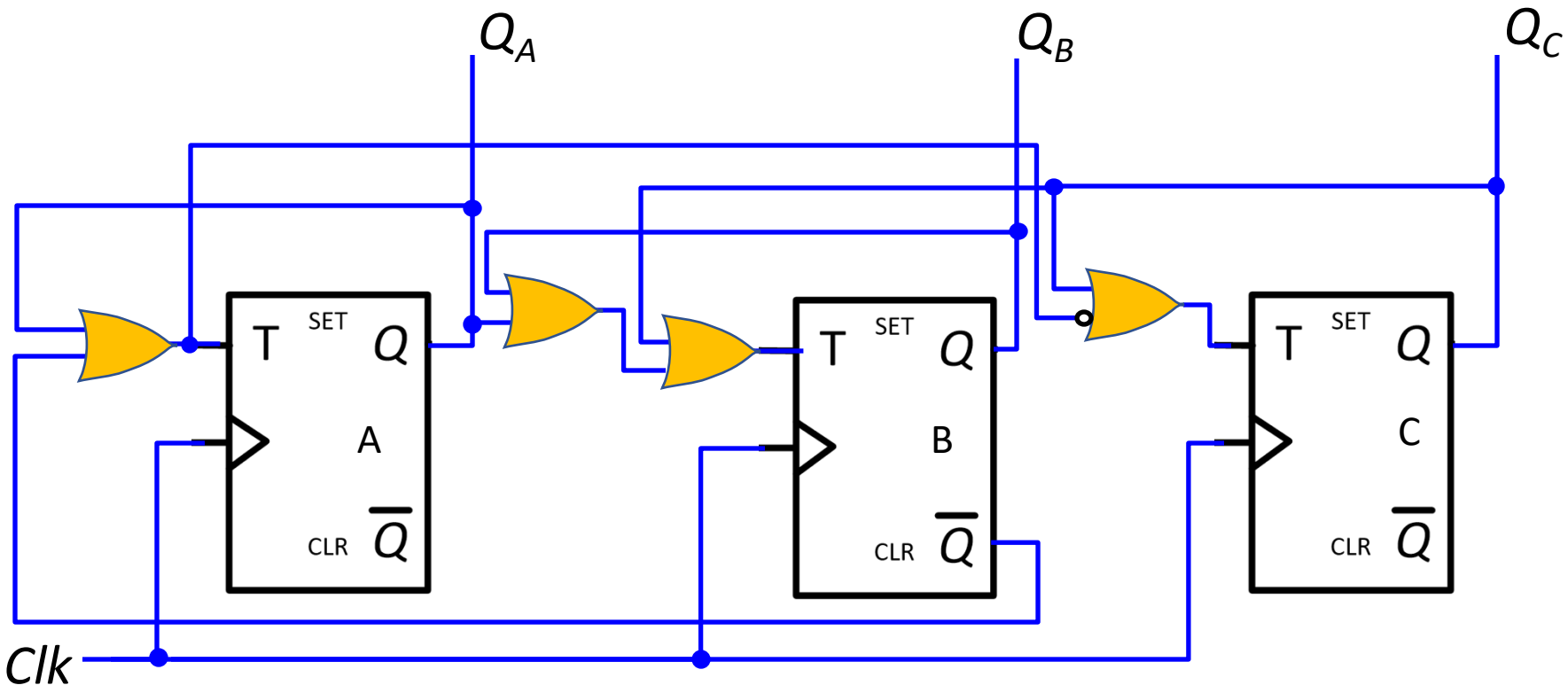
Exercise

$$T_A = Q'_B + Q_A$$

$$T_B = Q_A + Q_B + Q_C$$

STEP 4: Draw the Circuit

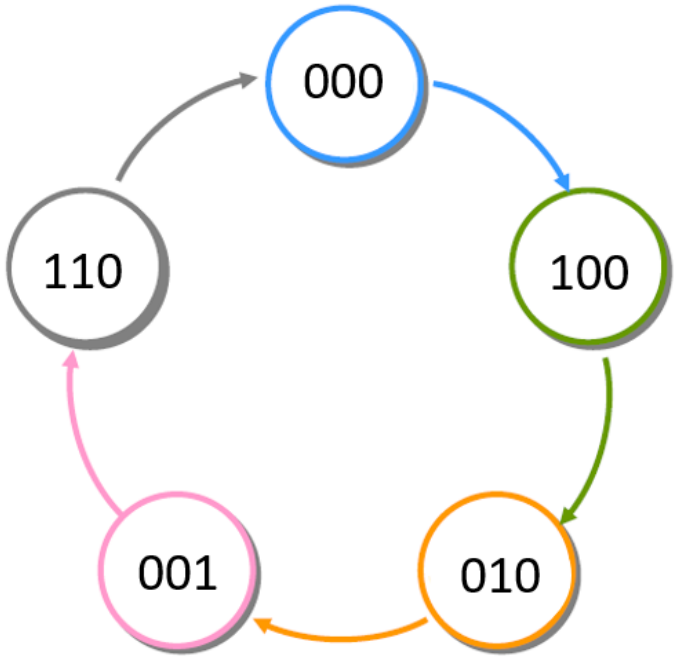
$$T_C = Q'_A Q_B + Q_C = (Q_A + Q'_B)' + Q_C$$



Exercise

Determine the state transition of remaining states

Present State			Next State			Flip-Flop		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	T_A	T_B	T_C
0	0	0	1	0	0	1	0	0
0	0	1	1	1	0	1	1	1
0	1	0	0	0	1	0	1	1
0	1	1						
1	0	0	0	1	0	1	1	0
1	0	1						
1	1	0	0	0	0	1	1	0
1	1	1						



$$T_A = Q'_B + Q_A$$

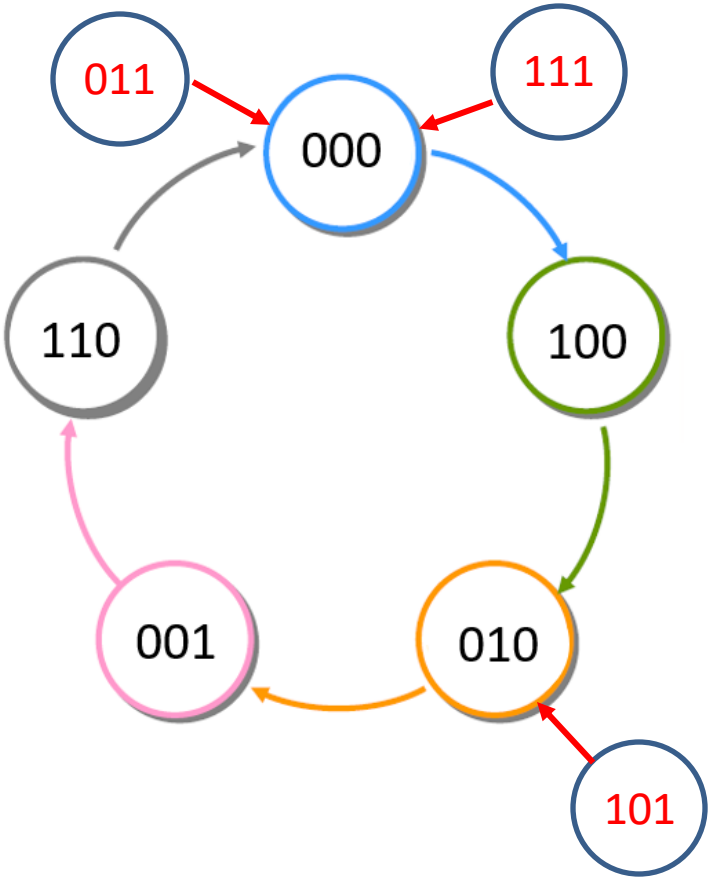
$$T_B = Q_A + Q_B + Q_C$$

$$T_C = Q'_A Q_B + Q_C$$

Exercise

Determine the state transition of remaining states

Present State			Next State			Flip-Flop		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	T_A	T_B	T_C
0	0	0	1	0	0	1	0	0
0	0	1	1	1	0	1	1	1
0	1	0	0	0	1	0	1	1
0	1	1	0	0	0	0	1	1
1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	1	1
1	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	1



$$T_A = Q'_B + Q_A$$

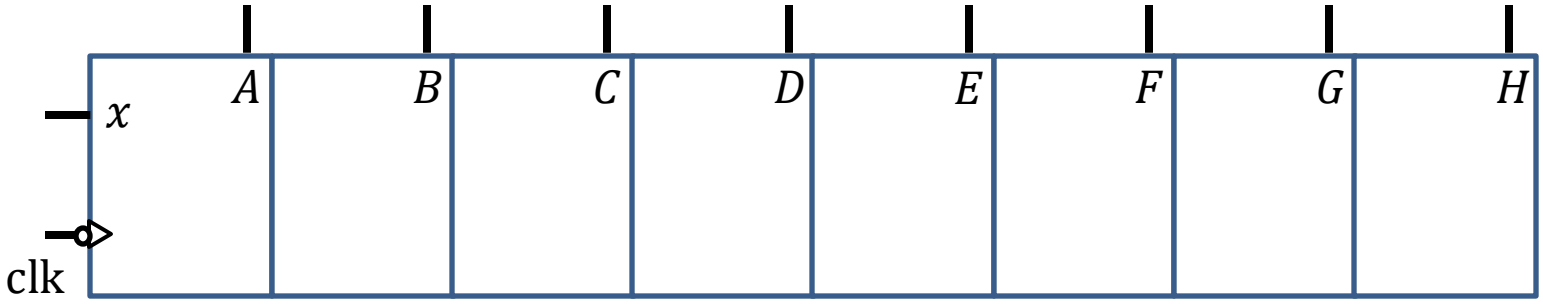
$$T_B = Q_A + Q_B + Q_C$$

$$T_C = Q'_A Q_B + Q_C$$

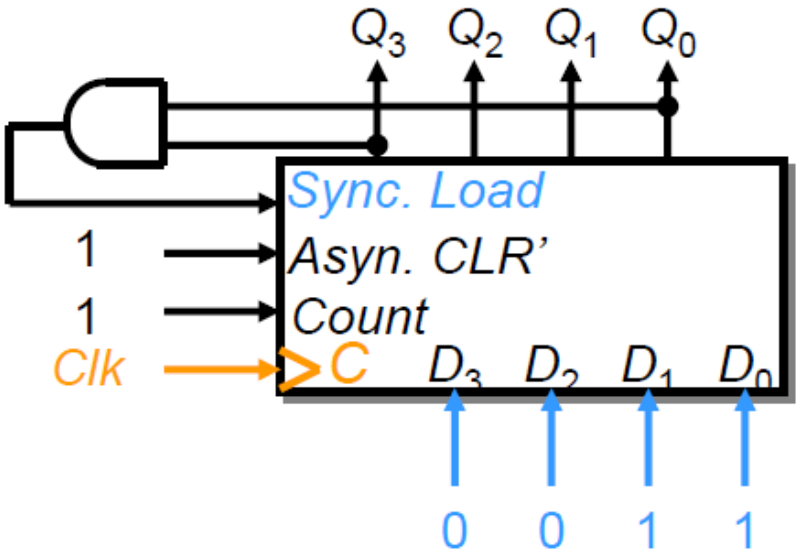
Exercise

Given an 8-bit serial-in parallel-out shift register as shown below, design a system with one output z, which is 1 only if the input x has been alternating for seven clock times (including the present one).

$$z = x\bar{A}B\bar{C}D\bar{E}F + \bar{x}A\bar{B}C\bar{D}E\bar{F}$$



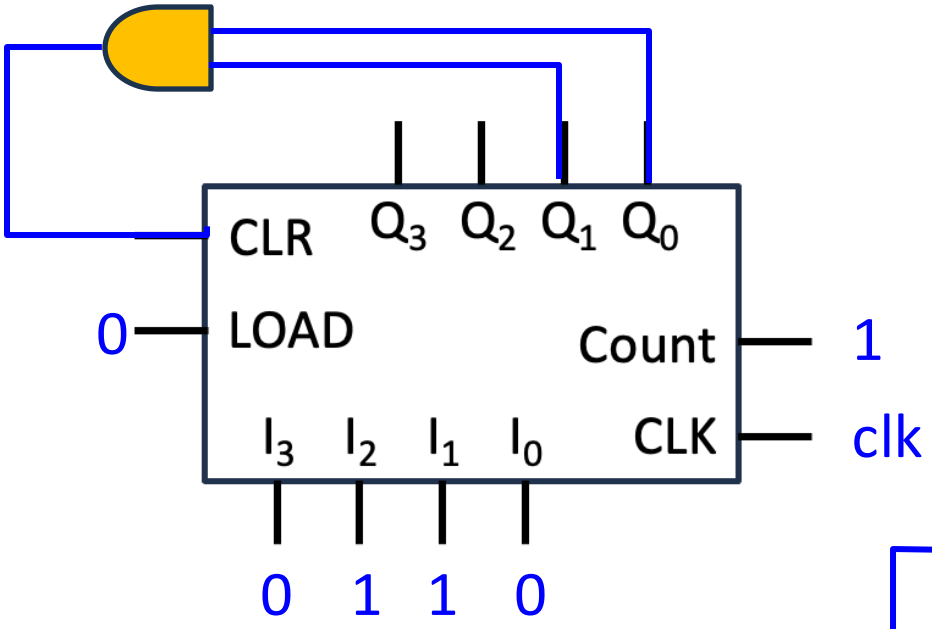
Exercise



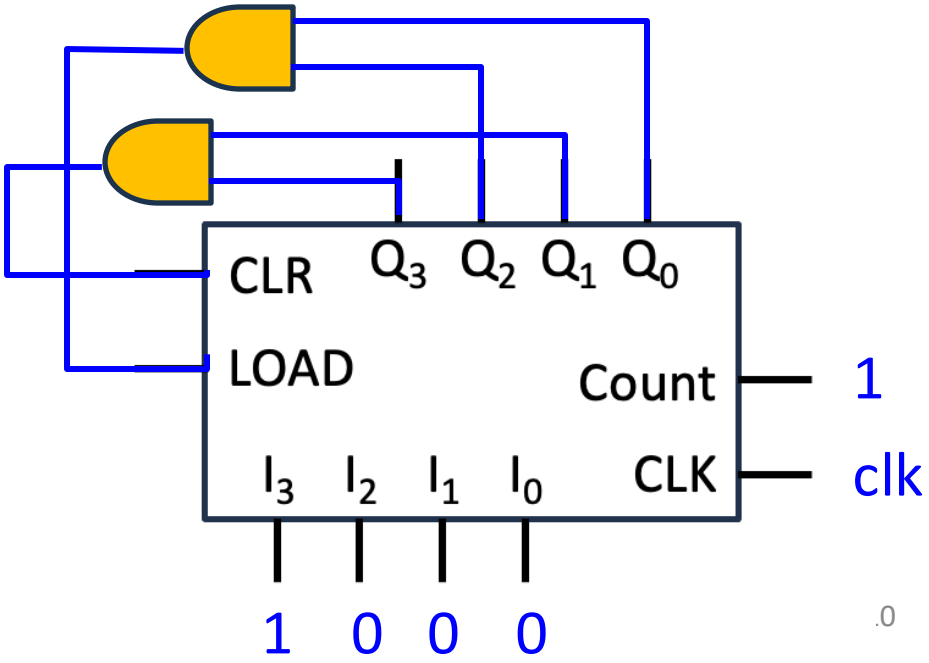
- Initial input: 0011
- Synchronous Load Bit: $Q_3 Q_0$

  → Reset to 0011 after 1xx1
- Counter: 0011 → 0100 → 0101 → 0110 → 0111 → 1000 → 1001 → 0011
- Mod-7 counter

Exercises



Counter: 0000 → 0001 → 0010 → 0011 → 0000



Counter: 1000

→ 1001 → 1010 → 0000
→ 0001 → 0010 → 0011
→ 0100 → 0101 → 1000