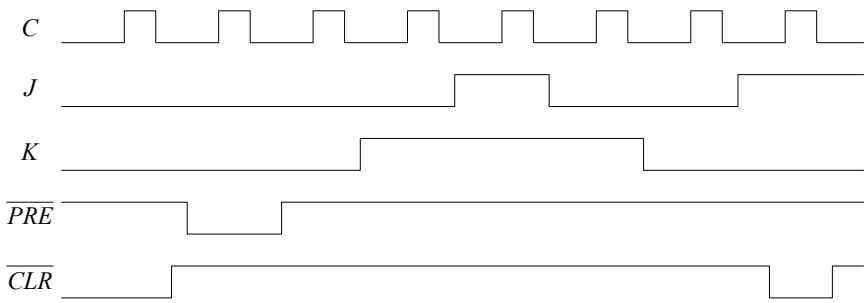
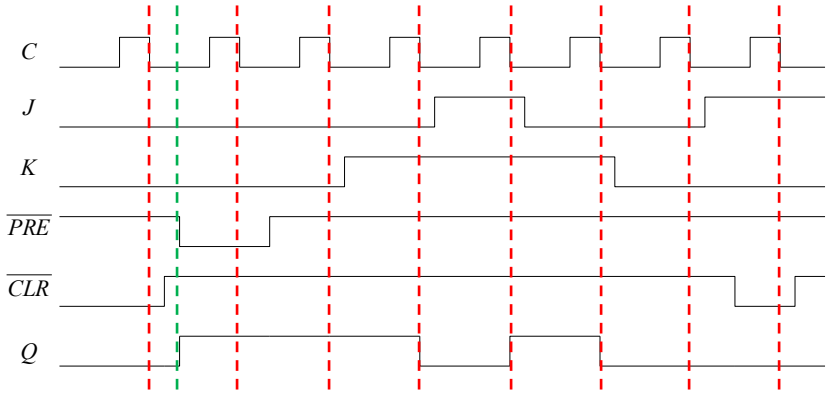
EE 2000 Logic Circuit Design
Semester A 2024/25

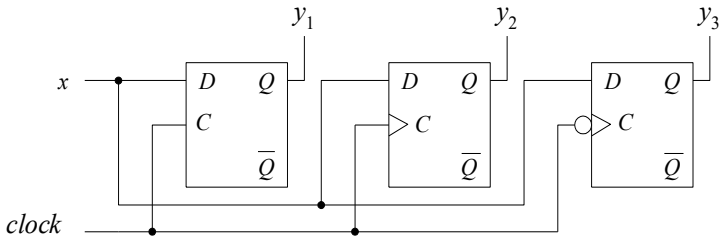
Tutorial 7

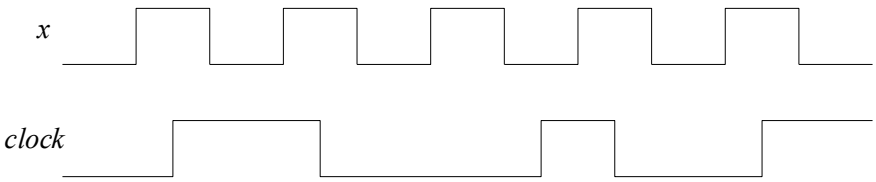
1. The waveforms are applied to the inputs of an SN7476 *JK* flip-flop (negative-edge triggered). Complete the timing diagram by drawing the waveforms of flip-flop output *Q*.

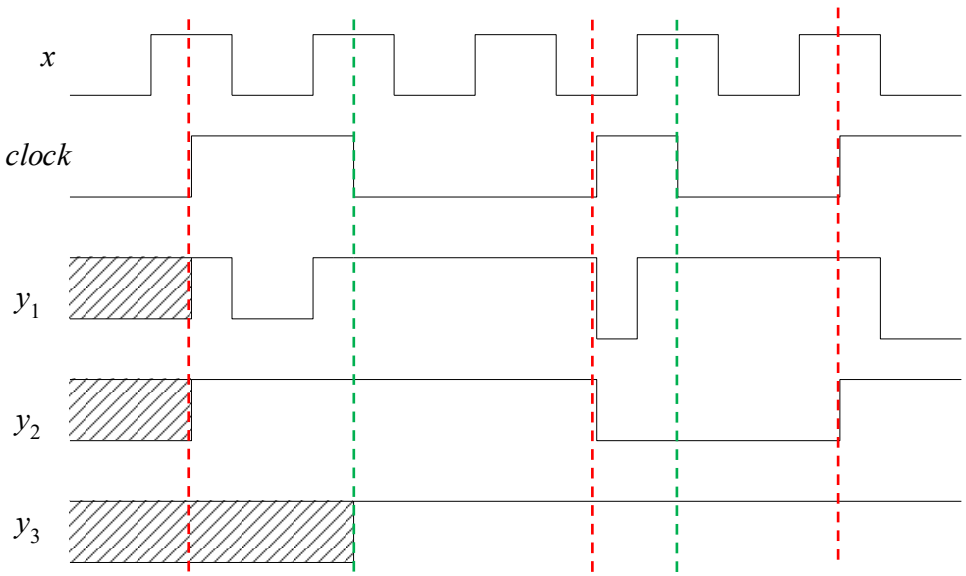




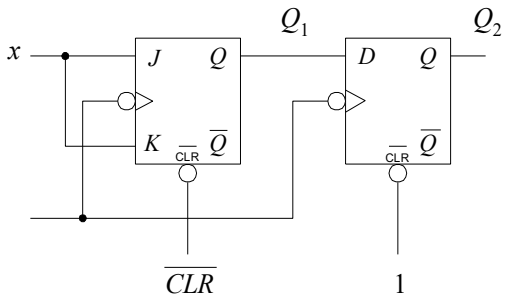
2. The circuit contains a *D* latch, a positive-edge-triggered *D* flip-flop, and a negative edge-triggered *D* flip-flop. Complete the timing diagram for the waveform of signals y_1, y_2 and y_3.

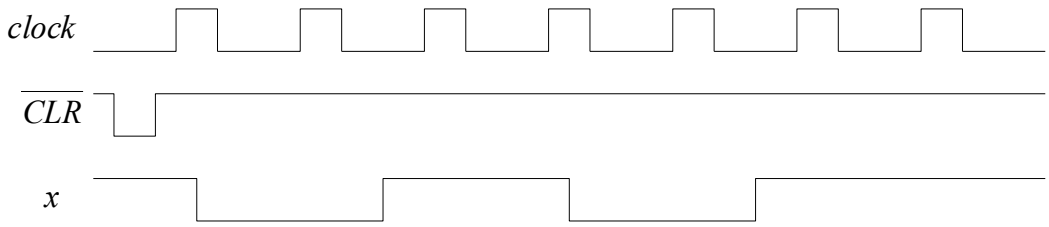


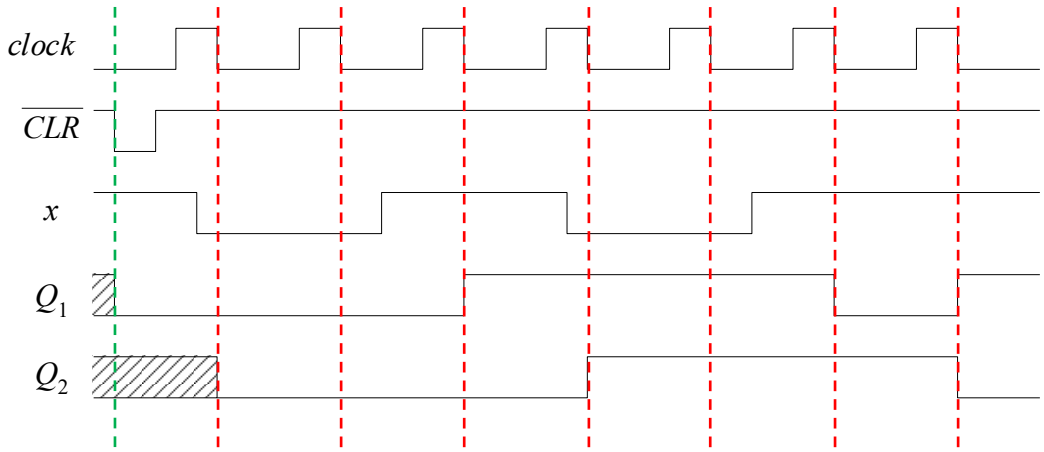




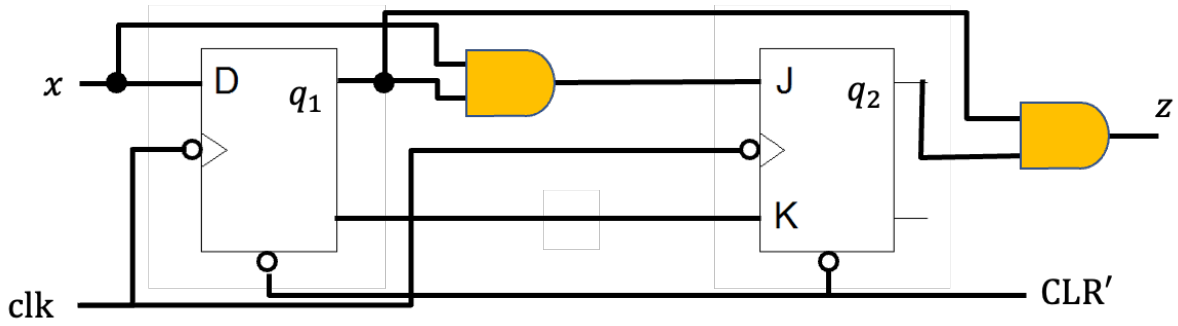
3. The circuit contains a negative edge–triggered *JK* flip-flop and a *D* flip-flop. Complete the timing diagram by drawing the waveforms of signals Q_1 and Q_2.

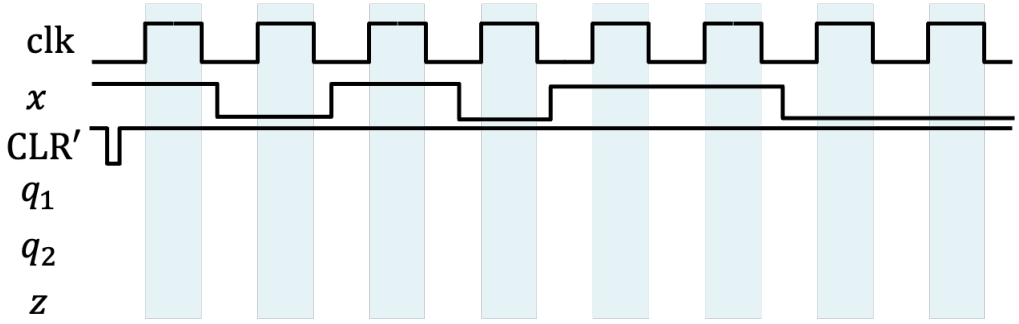






4. Complete the timing diagram by drawing the waveforms of signals q_1 and q_2.





$D = x$ $K = \overline{q_1}$ $J = xq_1$ $z = q_1q_2$