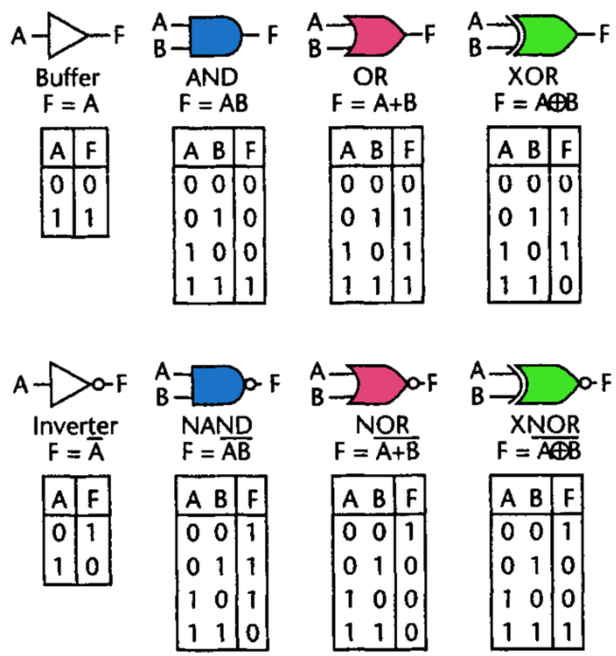
EE2000 Logic Circuit Design

Lecture 1 – Logic Function and Boolean Algebra



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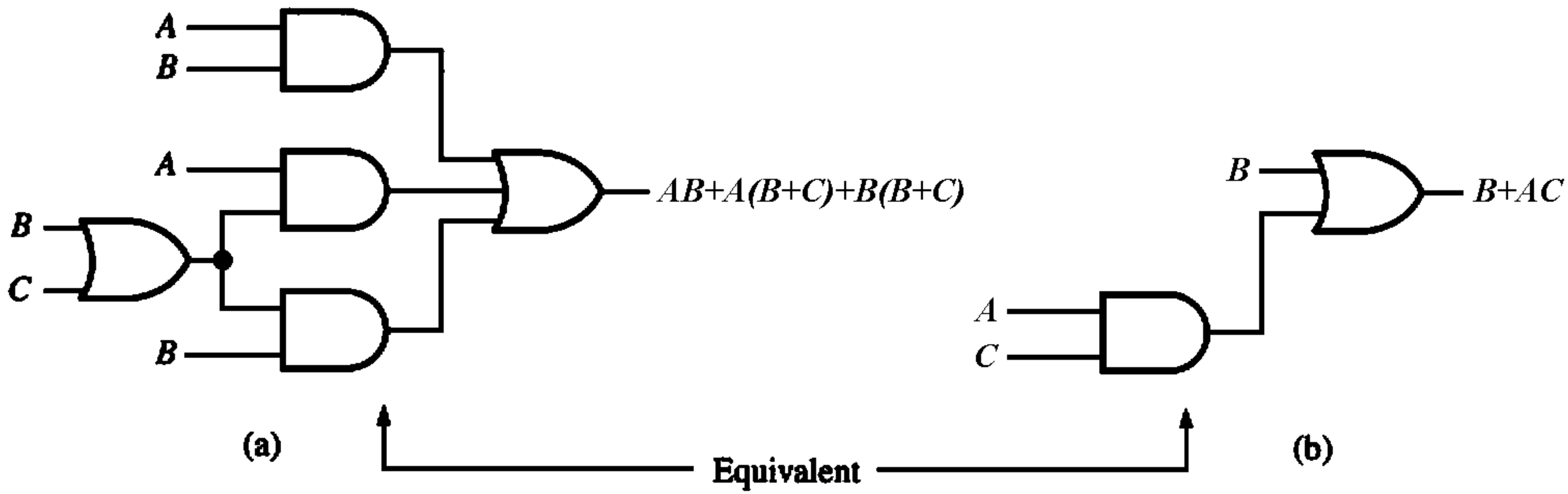
Summary (Given in Test and Exam)

Commutative	$a + b = b + a$	$ab = ba$
Associative	$a + (b + c) = (a + b) + c$	$a(bc) = (ab)c$
Identity	$a + 0 = a$	$a(1) = a$
Null	$a + 1 = 1$	$a(0) = 0$
Complement	$a + a' = 1$	$a(a') = 0$
Idempotency	$a + a = a$	$a(a) = a$
Involution	$(a')' = a$	
Distributive	$a(b + c) = ab + ac$	$a + bc = (a + b)(a + c)$
Adjacency	$ab + ab' = a$	$(a + b)(a + b') = a$
Simplification	$a + a'b = a + b$	$a(a' + b) = ab$
DeMorgan	$(a + b)' = a'b'$	$(ab)' = a' + b'$
Absorption	$a + ab = a$	$a(a + b) = a$
Consensus	$ab + a'c + bc = ab + a'c$	

Exercise



Prove that the above Circuit (a) is equivalent to Circuit (b).

Consensus

$$xy + x'z + yz = xy + x'z + yz(x + x')$$ complement

$$= xy + xyz + x'z + x'yz$$ distributive

$$= xy + x'z$$ adsorption

Consensus term: For any two product terms where **exactly** one variable appears uncomplemented in one and complemented in the other, the Consensus term is the product of the remaining literals. **The consensus term could be eliminated.**

Term 1	Term 2	Consensus Term
$xy'z$	wx'	$wy'z$
wxy'	xyz'	wxz'
wxy'	$xy'z$	$-$
$xy'z$	$wx'y$	$-$

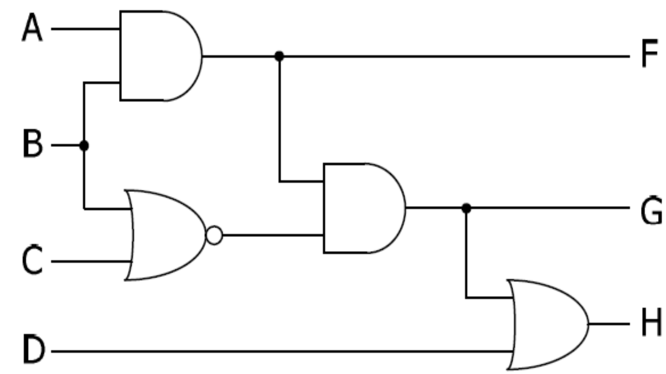
Exercise

Simplify the following function.

$$f(w,x,y,z) = wxy' + w'y'z + wx'y' + xy'z + w'z$$

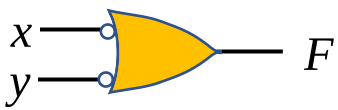
Exercise

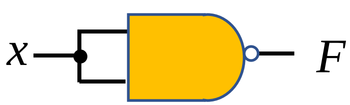
1. Derive the Boolean functions to describe the operations of the logic circuit as shown.
2. Simplify the functions and draw the circuit.

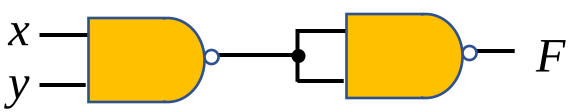


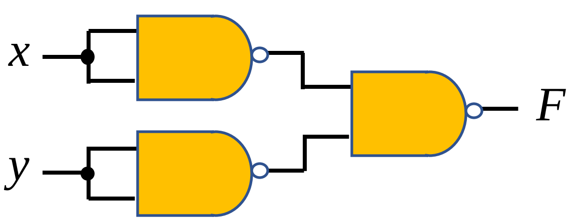
Exercise

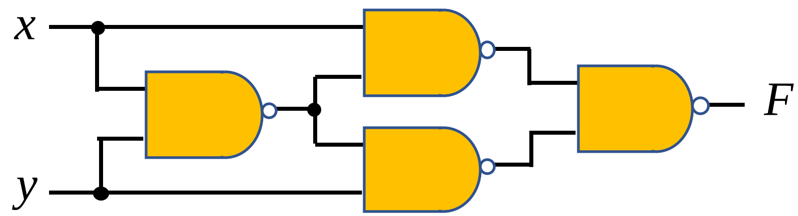
Work out the Boolean functions of the following circuits. Which standard logic gate does each of them represent?











Exercise

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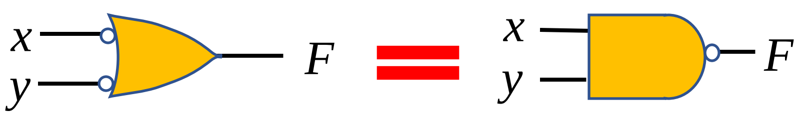
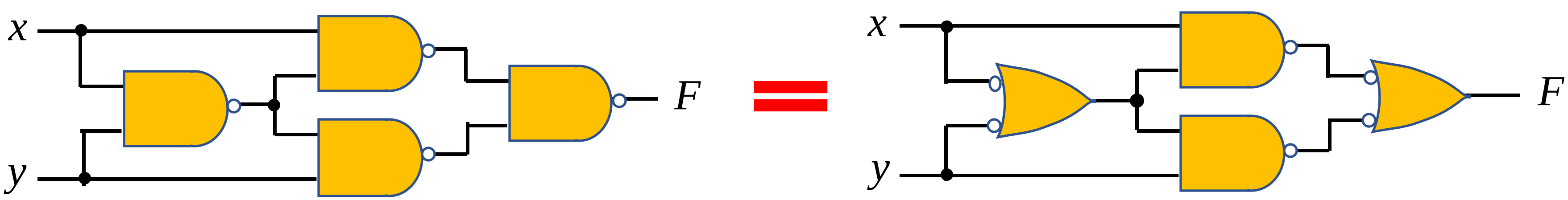


$F = x' + y' = (xy)'$



$$F = x(x' + y') + y(x' + y')$$
$$= xy' + yx' = x \oplus y$$

- ➢ Any Boolean function can be implemented using NAND gates (Functional completeness)
- ➢ NAND gates are used for SOP function
- ➢ Same for NOR gate but for POS function

Exercise

1. Express the Canonical Sum and Product based on the Truth Table provided.
2. Simplify the Function in SOP form.
3. Design the logic circuit using NAND and NOT gates.

Inputs			*Output*
x	y	z	$f(x, y, z)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1