B

Student Name: _____

Student ID: _____

EE2000 Logic Circuit Design

Mid-Term Test 2 (Semester A 2024/25)

Instructions:

1. You are responsible for receiving the exam paper, **hand-writing your name and SID** and returning it to the examiner in the hall.
2. Total time: **60 min**
3. This paper consists of **4** questions. Answer **ALL** questions in the space given after each question.
4. Please show all steps or else marks will be deducted.
5. **Remain seated** until the examiner allows you to leave at the end of the test. You are not allowed to leave the hall earlier.

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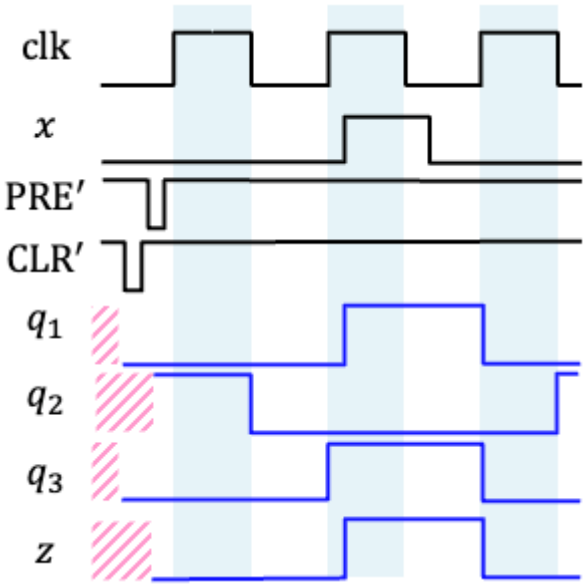
*This is a **closed-book** examination.*

No materials or aids are allowed during the whole examination. If any unauthorized materials or aids are found on a student during the examination, the student will be subject to disciplinary action.

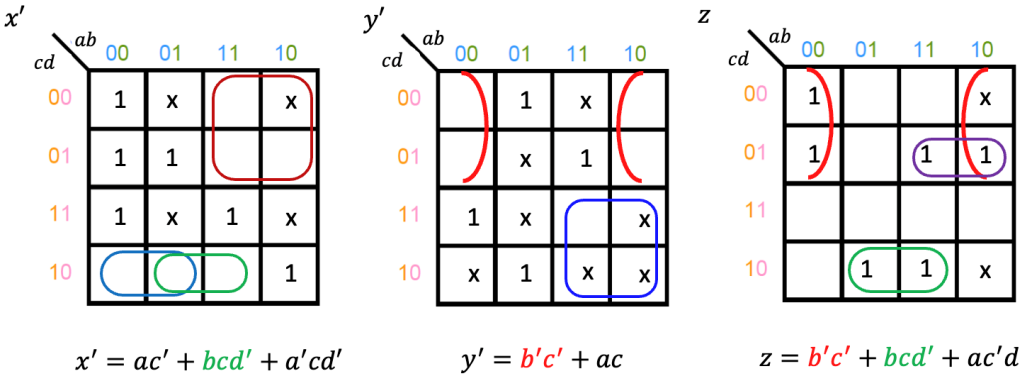
B

QUESTION 1

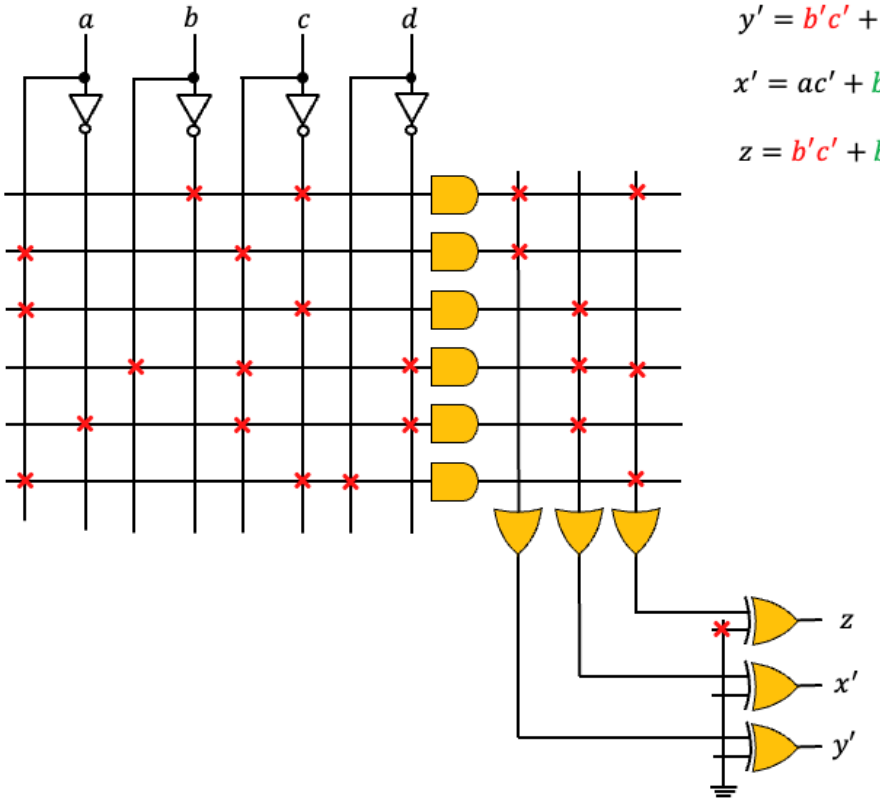


B

QUESTION 2



$x' = ac' + bcd' + a'cd'$ $y' = b'c' + ac$ $z = b'c' + bcd' + ac'd$



$y' = b'c' + ac$

$x' = ac' + bcd' + a'cd'$

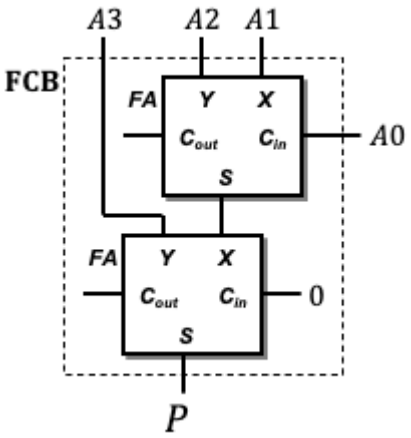
$z = b'c' + bcd' + ac'd$

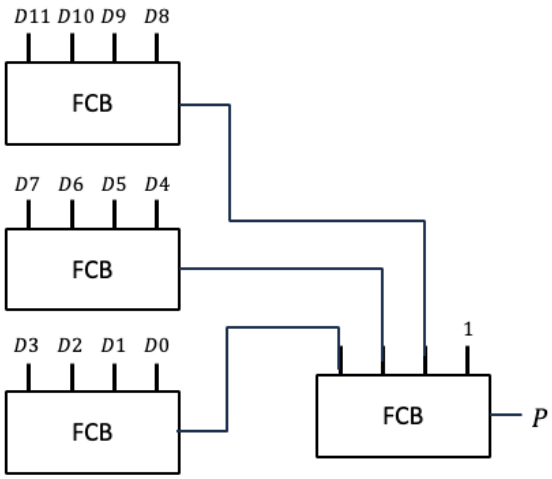
QUESTION 3

- Synchronous active low clear/reset input
- Rising/Positive/leading edge triggered T Flip-flop

B

QUESTION 4





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