EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 4

1. What are the mistakes for this VHDL?

```
Library ieEe;
use IEEE.std-logic_1164.all;

ENTITY and_gate IS
    port (a&b : in STD_LOGIC;
          S: out STD_LOGIC;);
end;

architecture CKT of anD_Gate IS
begin
          s <= a AND b;
end ckt;
```

```
Library ieEe;
use IEEE.std_logic_1164.all;

ENTITY and_gate IS
    port (a, b : in STD_LOGIC;
          S: out STD_LOGIC);
End and_gate;

architecture CKT of anD_Gate IS
begin
          s <= a AND b;
end ckt;
```

2. Using VHDL to write the library and entity declarations for a logic design entity named MoZone that has the following inputs and outputs.
   (a) A1 is an array of 8-bit std_logic data with the highest index number holding the most significant bit.
   (b) A2 is a 5-bit bit vector with the lowest index number holding the most significant bit
   (c) O1 is a 1-bit std_logic output

```
library ieee;
use IEEE.std_logic_1164.all;

ENTITY mozone is
    port (A1 : in std_logic_vector(7 downto 0);
          A2 : in bit_vector(0 to 4);
          O1 : out std_logic);
End mozone;
```

3. Write a complete VHDL design module (with entity and architecture) to implement a circuit with the following Boolean expressions. Use concurrent statements and without NAND and NOR operators in your design.

   - x1 = A'B'C + A(BC)'
   - x2 = (A'B + C')(BC' + A)'
   - x3 = (A(BC)' + A'C')'

```
ENTITY Prob_3 is
   port (A, B, C : in bit;
         x1, x2, x3 : out bit);
End Prob_3;

architecture behavior of Prob_3 is
begin
         x1 <= (NOT A AND NOT B AND C) OR (A AND NOT (B AND C));
         x2 <= (NOT A AND B OR NOT C) AND NOT (B AND NOT C OR A);
         x3 <= NOT ((A AND NOT (B AND C)) OR (NOT A AND NOT C));
end behavior;
```

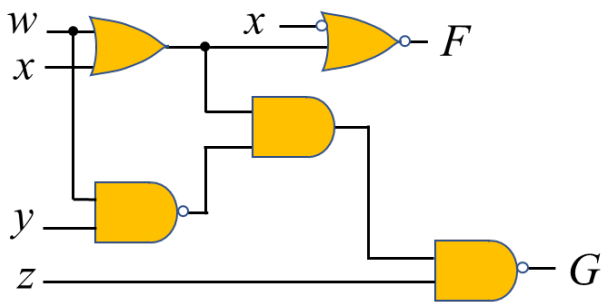
4. Write a complete VHDL design module to implement a circuit with the following Boolean expressions. Assign a signal name sigW1 to represent the common logic term in your design. Use concurrent statements without NAND and NOR operators in your design.

   - A = (XY'Z')' + XZ
   - B = (XY'Z')'(X + Z)
   - C = ((XY'Z')'+X')'

```
ENTITY Prob_4 is
   port (X, Y, Z : in bit;
         A, B, C : out bit);
End Prob_4;

architecture behavior of Prob_4 is
signal sigW1 : bit;
begin
         sigW1 <= NOT (X AND NOT Y AND NOT Z);
         A <= sigW1 OR (X AND Z);
         B <= sigW1 AND (X OR Z);
         C <= NOT (sigW1 OR NOT X);
end behavior;
```

5. Write a complete VHDL design module to implement the combinational circuit shown. Assign signals for intermediate outputs. Use concurrent statements (i) without NAND and NOR operators in your design; and (ii) with NAND and NOR operators.




```
ENTITY Prob_5 is
    port (w, x, y, z : in bit;
          F, G : out bit);
End Prob_5;

architecture behavior of Prob_5 is
signal s1, s2, s3 : bit;
begin
          s1 <= w OR x;
          F <= NOT (NOT x OR s1);
          s2 <= NOT (w AND y);
          s3 <= s1 AND s2;
          G <= NOT (s3 AND z);
end behavior;
```

```
ENTITY Prob_5 is
    port (w, x, y, z : in bit;
          F, G : out bit);
End Prob_5;

architecture behavior of Prob_5 is
signal s1, s2, s3 : bit;
begin
          s1 <= w OR x;
          F <= NOT x NOR s1;
          s2 <= w NAND y;
          s3 <= s1 AND s2;
          G <= s3 NAND z;
end behavior;
```