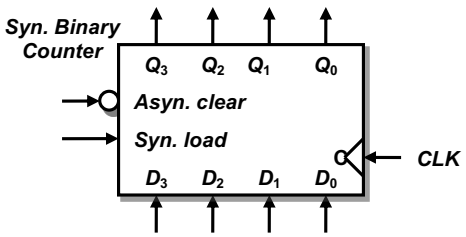
EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 10

1. Using JK FFs and with the minimum number of states to design a counter with counting sequence: 0,4,2,1,6 and repeat. State whether the circuit is a self started circuit.

2. Design a sequential circuit with two JK FFs, A & B, and two inputs, x & E. if E=0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E =1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

3. Using a synchronous binary counter as shown, design and draw a counter to generate the following repeating sequences 2 to 9 repeatedly for a free running clock.



4. Given the following VHDL code, Specify which functional block is being implemented and its function in detail.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity func1 is
port ( clk: in std_logic;
       rst: in std_logic;
       Q: out std_logic_vector (3 downto 0));
end func1;

architecture Behavioral of func1 is
signal temp: std_logic_vector(3 downto 0) := "0000";
begin
    process(clk, rst)
        if rst = '1' then
                temp <= "0000";
        elsif rising_edge(clk) then
                temp(2) <= temp(3);
                temp(1) <= temp(2);
                temp(0) <= temp(1);
                temp(3) <= not temp(0);
        end if;
    end process;
    Q <= temp;
end Behavioral;
```