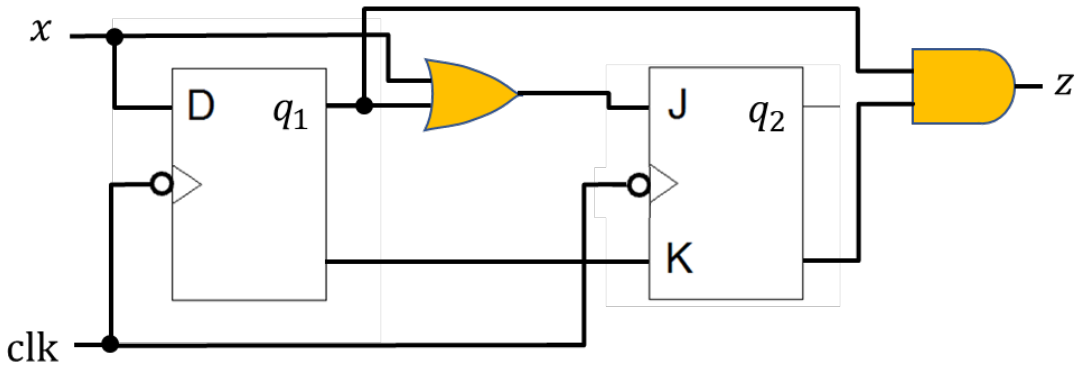
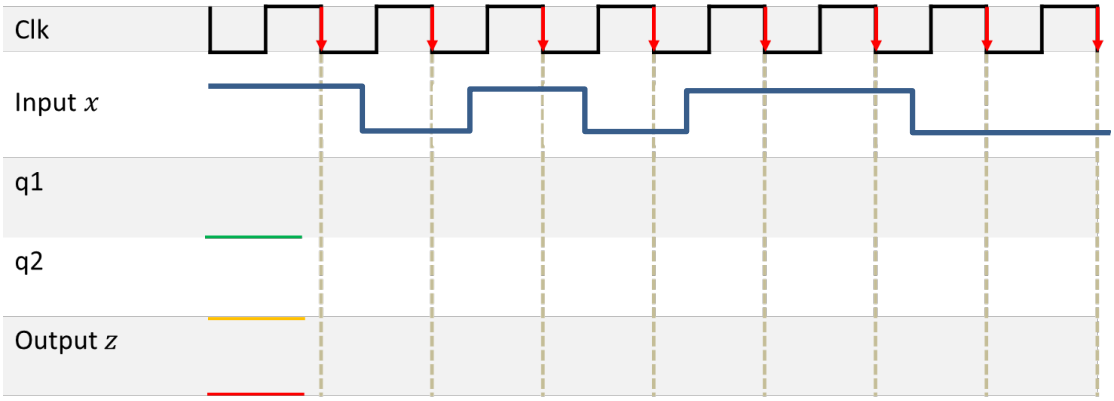
EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 9

1. For the following circuits, (a) determine the state table and state diagram (calling the states 00, 01, 10, 11), (b) complete the timing diagram as shown.





2. Design a Mealy system using D-FFs with one input x and one output z such that z = 1 if x has been 1 for exactly two consecutive clock-times. A sample input/output trace for such a system is shown below.

x	0	1	1	1	1	0	1	1	0	0	1	0
z	0	0	0	0	0	0	0	0	1	0	0	0

3. Design a Moore system with one input x and one output z such that z = 1 if a sequence of "101" has been detected (overlapping is allowed). A sample input/output trace for such a system is shown below.

x	0	1	0	1	1	0	1	0	1	0	0	0
z	0	0	0	0	1	0	0	1	0	1	0	0

4. Use the partitioning method to minimize the number of states in the state table shown.

	Next state		Output	
Present state	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	F	B	0	0
B	D	C	0	0
C	F	E	0	0
D	G	A	1	0
E	D	C	0	0
F	F	B	1	1
G	G	H	0	1
H	G	A	1	0