EE 2000 Logic Circuit Design
Semester A 2024/25

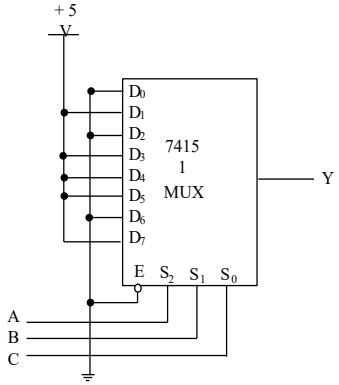
Tutorial 5

1. With the following functions, design a circuit with a 3-to-8-line decoder and external gates.

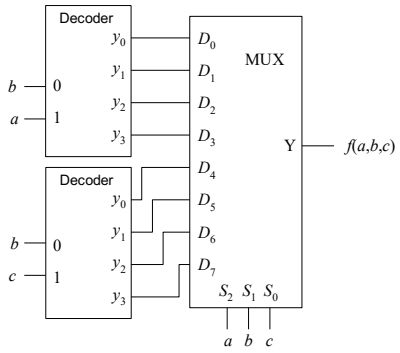
$F_1(x, y, z) = x'yz' + xz'$

$F_2(x, y, z) = xyz' + x'z$

2. (a) Complete the truth table of the following circuit.
(b) Write down the logic expression of the following circuit and simplify as much as possible.
(c) Draw the simplified logic expression obtained in (b) using 2-input NAND gate(s) only.



3. (a) Show the Boolean function $f(a,b,c)$ of the following circuit.
(b) Simplify your answer in (a) by K-Map.



4. Implement the following Boolean function with a 4×1 MUX and external gates. Connect inputs A and B to the selection lines and inputs C and D to the data input lines of the MUX.

$$F(A,B,C,D) = \Sigma\, m(1,3,5,11,12,13,14,15)$$

5. What is the largest number of data inputs which a multiplexer with k input selection inputs can handle?

How many selection lines are contained in a multiplexer with 1024 inputs and one output?

For the multiplexer circuits shown in the following figure below, what are $Y_1(A, B, C)$ and $Y_2(A, B, C)$ respectively? Please list in standard sum of products form.