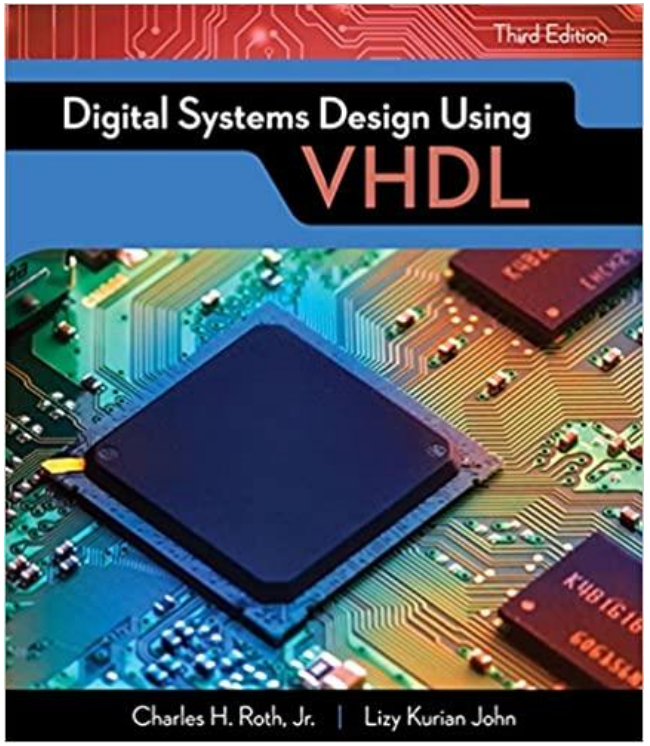
EE2000 Logic Circuit Design

Lecture 8– VHDL 2



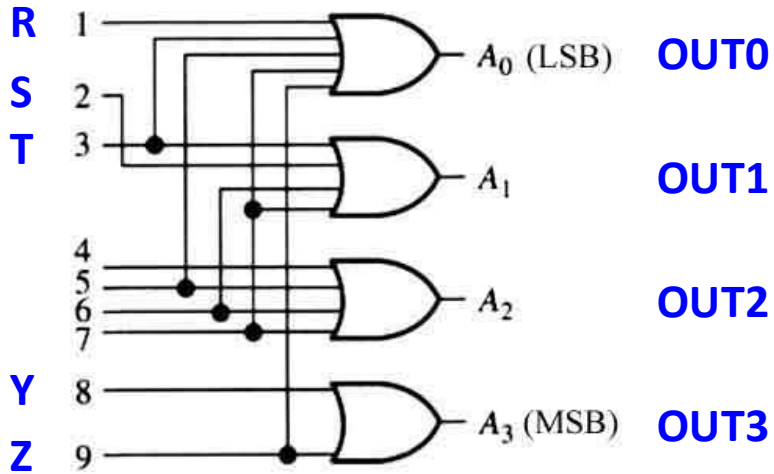
Encoder (Decimal-to-BCD Encoder)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ENC3 is
    Port ( Q : in std_logic;
           R : in std_logic;
           S : in std_logic;
           T : in std_logic;
           U : in std_logic;
           V : in std_logic;
           W : in std_logic;
           X : in std_logic;
           Y : in std_logic;
           Z : in std_logic;
           OUT0 : out std_logic;
           OUT1 : out std_logic;
           OUT2 : out std_logic;
           OUT3 : out std_logic);
end ENC3;
architecture Behavioral of ENC3 is
begin
           process (Q,R,S,T,U,V,W,X,Y,Z)
           begin

           end process;
end Behavioral;
```

Enter your codes here




```
OUT0 <= R OR T OR V OR X OR Z;
OUT1 <= S OR T OR W OR X;
OUT2 <= U OR V OR W OR X;
OUT3 <= Y OR Z;
```

T-Flip Flop with RESET

Rising edge FF

Asyn Active High Reset

C	T	Q_{t+1}	$\overline{Q_{t+1}}$	State
0	x	Q_t	$\overline{Q_t}$	Hold
1	0	Q_t	$\overline{Q_t}$	Hold
1	1	$\overline{Q_t}$	Q_t	Toggle

```
library ieee;
use ieee.std_logic_1164.all;

entity TFF is
port(   T: in std_logic;
        clk: in std_logic;
        areset: in std_logic;
        Q: out std_logic;
end TFF;
```

```
architecture behavioral of TFF is
signal tmp : std_logic;
begin
process(clk, areset)
begin
 if areset = '1' then
   TMP <= '0';
 elsif rising_edge(clk) then
   if (T = '1') then
     TMP <= not TMP;
   end if;
 end if;
Q <= TMP;
end process;
end behavioral;
```