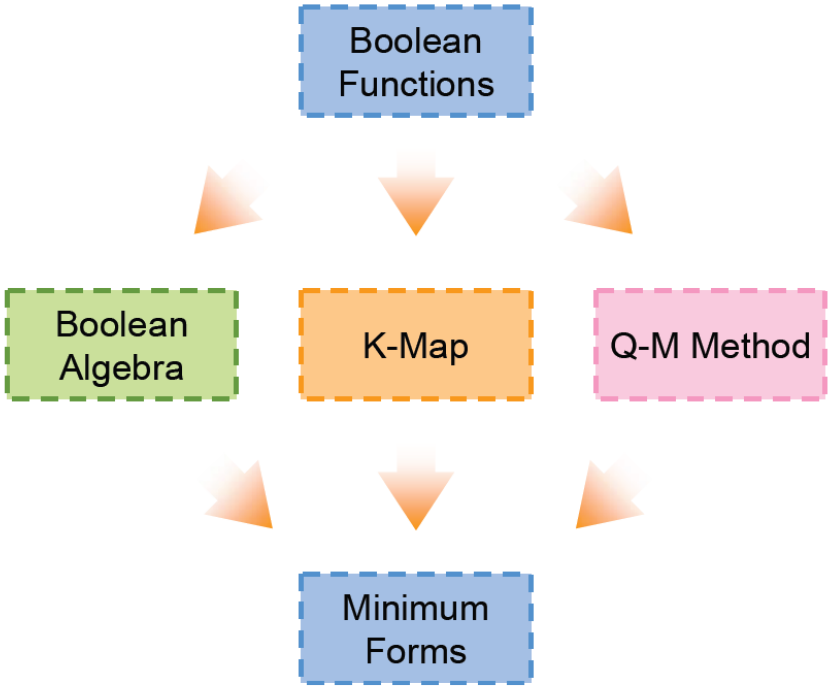
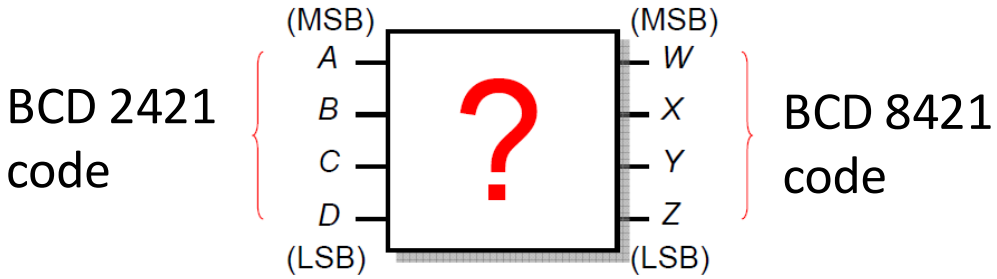
EE2000 Logic Circuit Design

Lecture 3 – Combinational System Design



Exercise

- Design a logic circuit that perform code conversion



- Input is BCD 2421 code
- Output is BCD 8421 code

*Using only Two-input Gates and NOT Gates.

State the case

Design a circuit to convert the BCD 2421 to the BCD 8421 code

- *A, B, C, D* are the input.
- *W, X, Y, Z* are the output.
- The output functions are:

  W (*A, B, C, D*)
  X (*A, B, C, D*)
  Y (*A, B, C, D*)
  Z (*A, B, C, D*)

Formulation

Decimal numbers	Minterms	Inputs (2421)				Outputs (8421)			
		A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1
2	2	0	0	1	0	0	0	1	0
3	3	0	0	1	1	0	0	1	1
4	4	0	1	0	0	0	1	0	0
5	11	1	0	1	1	0	1	0	1
6	12	1	1	0	0	0	1	1	0
7	13	1	1	0	1	0	1	1	1
8	14	1	1	1	0	1	0	0	0
9	15	1	1	1	1	1	0	0	1
Unused	5	x	x	x	x	x	x	x	x
Unused	6	x	x	x	x	x	x	x	x
Unused	7	x	x	x	x	x	x	x	x
Unused	8	x	x	x	x	x	x	x	x
Unused	9	x	x	x	x	x	x	x	x
Unused	10	x	x	x	x	x	x	x	x

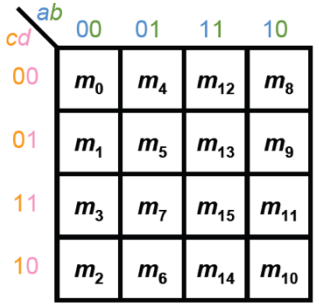
$$W(A,B,C,D) = \sum m(14,15) + \sum d(5,6,7,8,9,10)$$

$$X(A,B,C,D) = \sum m(4,11,12,13) + \sum d(5,6,7,8,9,10)$$

$$Y(A,B,C,D) = \sum m(2,3,12,13) + \sum d(5,6,7,8,9,10)$$

$$Z(A,B,C,D) = \sum m(1,3,11,13,15) + \sum d(5,6,7,8,9,10)$$

Simplification



$W(A,B,C,D)$

CD \ AB	00	01	11	10
00				x
01		x		x
11		x	1	
10		x	1	x

$X(A,B,C,D)$

CD \ AB	00	01	11	10
00		1	1	x
01		x	1	x
11		x		1
10		x		x

$Y(A,B,C,D)$

CD \ AB	00	01	11	10
00			1	x
01		x	1	x
11	1	x		
10	1	x		x

$Z(A,B,C,D)$

CD \ AB	00	01	11	10
00				x
01	1	x	1	x
11	1	x	1	1
10		x		x

$$W = BC$$

$$X = BC' + AB'$$

$$Y = AC' + A'C$$

$$Z = D$$

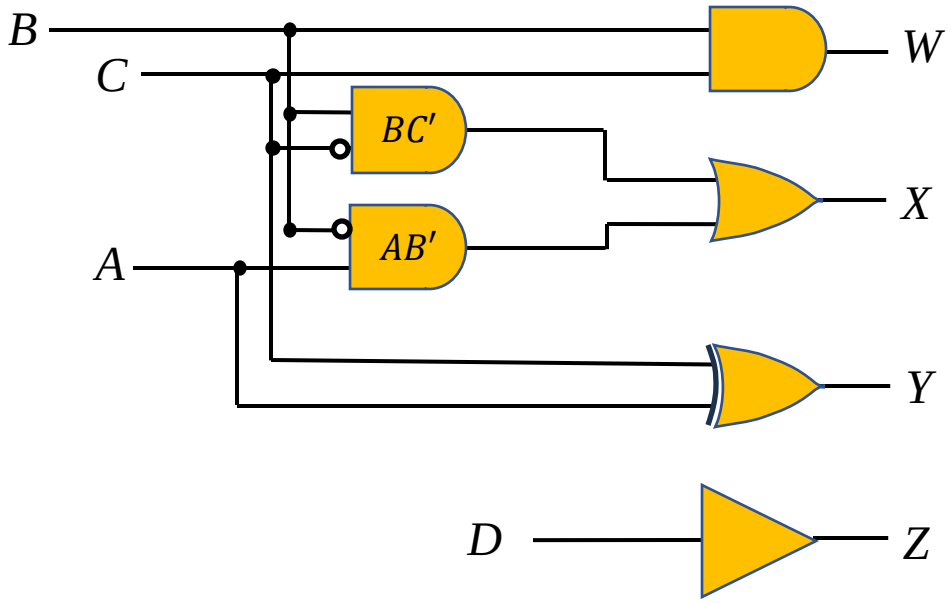
Logic Circuit

$W = BC$

$X = BC' + AB'$

$Y = AC' + A'C$

$Z = D$



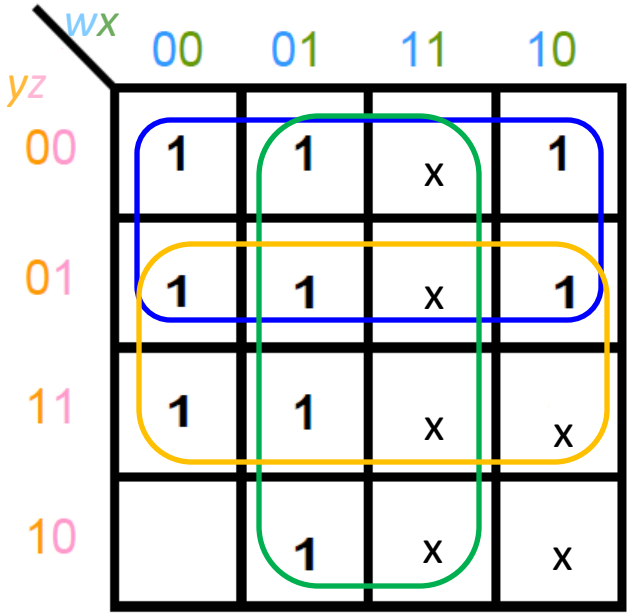
*Using only Two-input Gates and NOT Gates.

K-map for segment ‘c’

cd \ ab	00	01	11	10
00	m_0	m_4	m_{12}	m_8
01	m_1	m_5	m_{13}	m_9
11	m_3	m_7	m_{15}	m_{11}
10	m_2	m_6	m_{14}	m_{10}

$$c\,(w,x,y,z) = \Sigma m(0,1,3,4,5,6,7,8,9) + \Sigma d(10,11,12,13,14,15)$$

yz \ wx	00	01	11	10
00	1	1	x	1
01	1	1	x	1
11	1	1	x	x
10		1	x	x



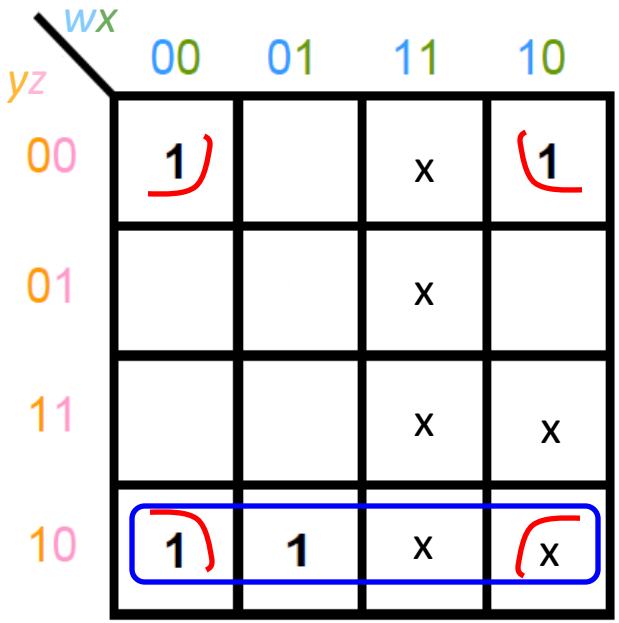
$$c(w,x,y,z) = x + y' + z$$

K-map for segment ‘e’

cd \ ab	00	01	11	10
00	m_0	m_4	m_{12}	m_8
01	m_1	m_5	m_{13}	m_9
11	m_3	m_7	m_{15}	m_{11}
10	m_2	m_6	m_{14}	m_{10}

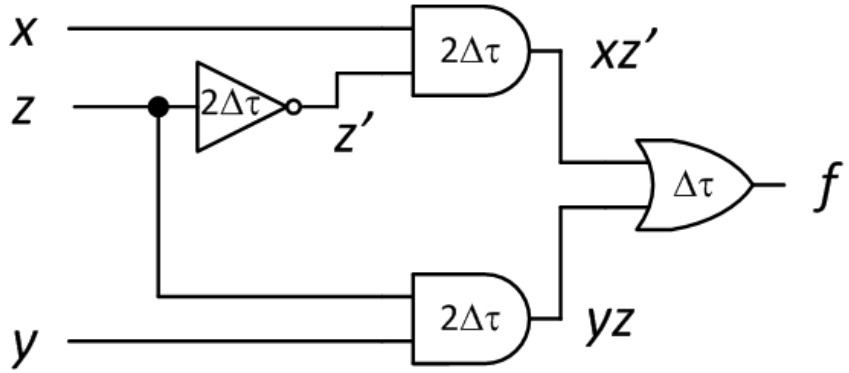
$$e\,(w,x,y,z) = \Sigma m(0,2,6,8) + \Sigma d(10,11,12,13,14,15)$$

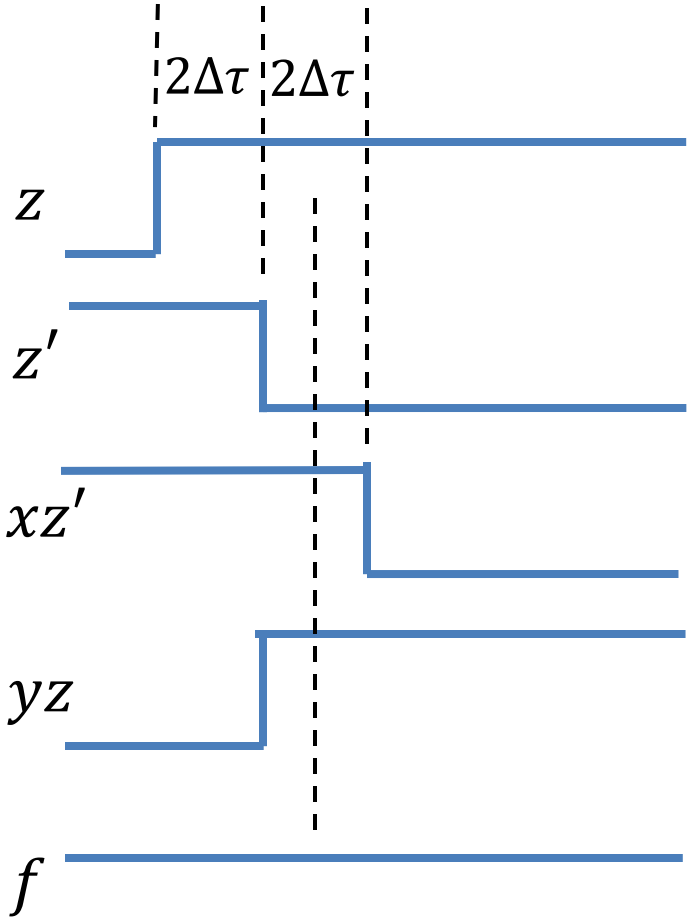
yz \ wx	00	01	11	10
00	1		x	1
01			x	
11			x	x
10	1	1	x	x



$$e(w,x,y,z) = x'z' + yz'$$

Exercise



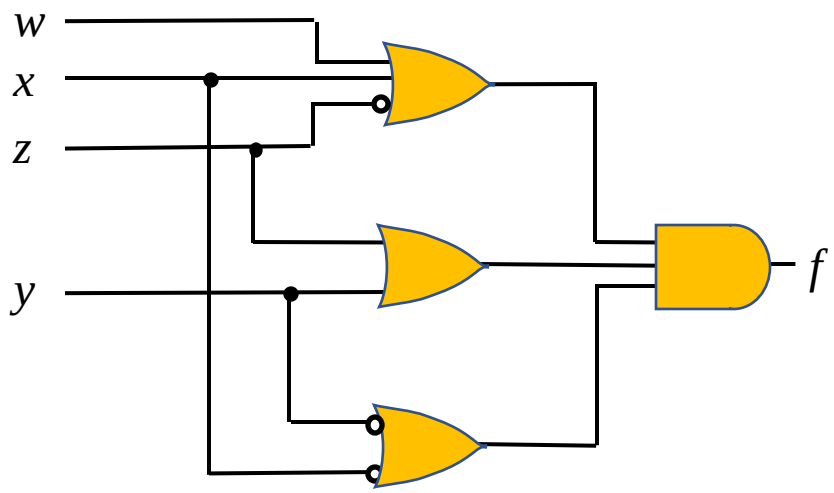


Assume that the propagation delay of each gate are as shown above.

Work out the timing diagram to identify the presence of any timing hazard when the input condition changes from $(x, y, z) = (1,1,0)$ to $(1,1,1)$.

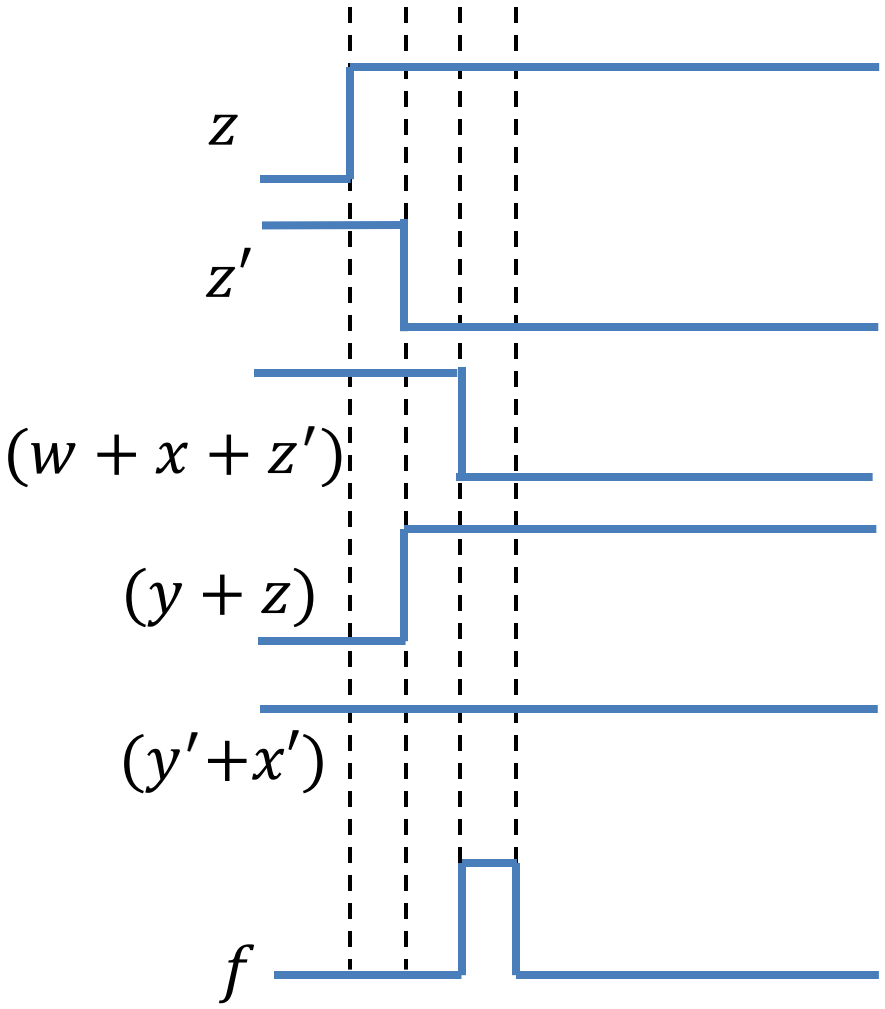
No hazard!!!

Exercise



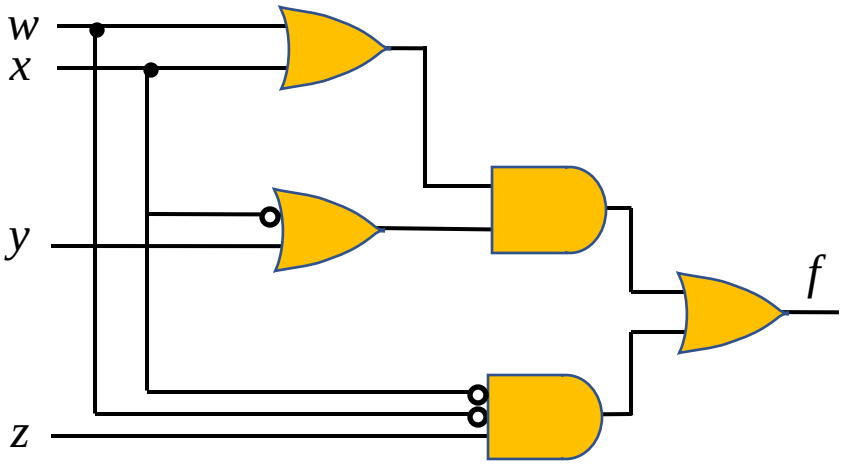
Assume that the propagation delay of all gates is $\Delta\tau$.

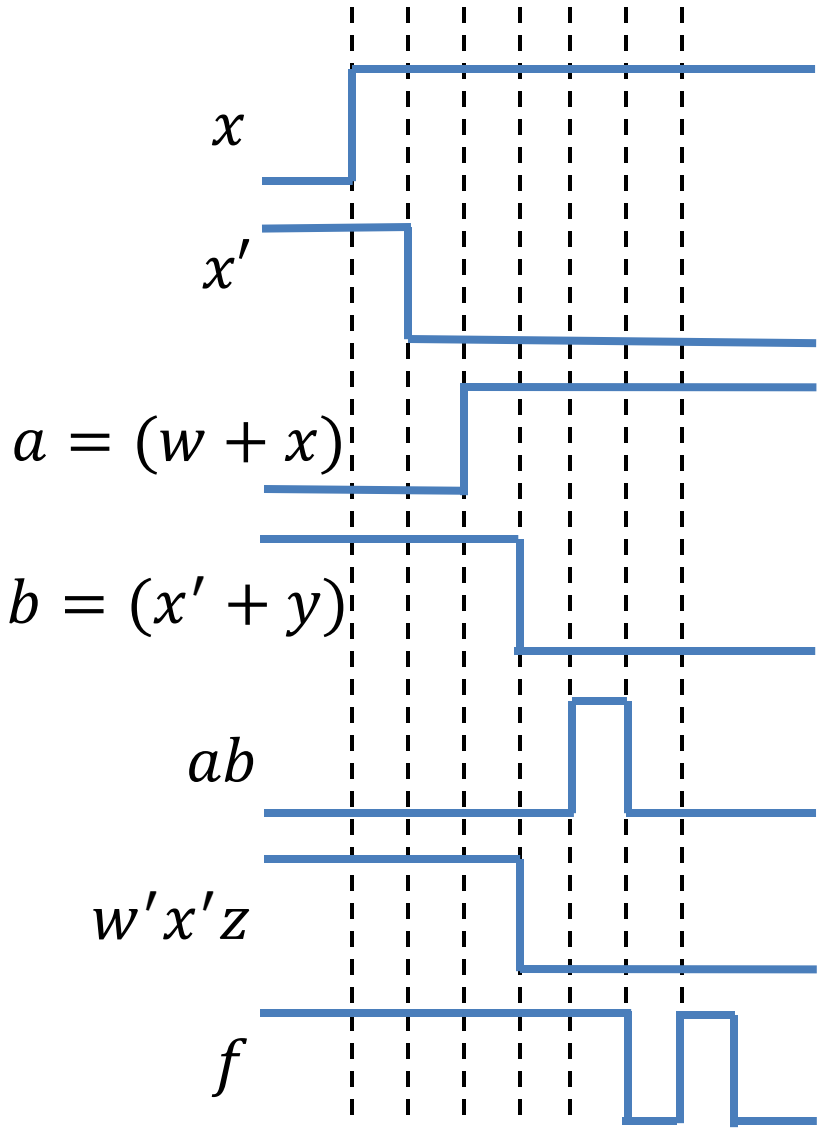
Work out the timing diagram to identify the presence of any timing hazard when the input condition changes from $(w, x, y, z) = (0,0,0,0)$ to $(0,0,0,1)$.



Static-0 hazard!!!

Exercise





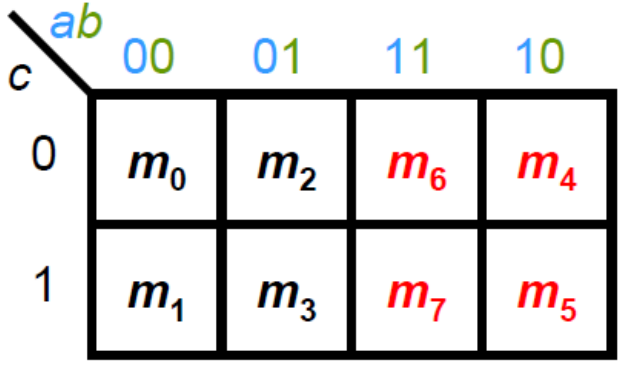
Assume that the propagation delay of NOT gate is $\Delta\tau$ and $2\Delta\tau$ for others .

Work out the timing diagram to identify the presence of any timing hazard when the input condition changes from $(w, x, y, z) = (0,0,0,1)$ to $(0,1,0,1)$.

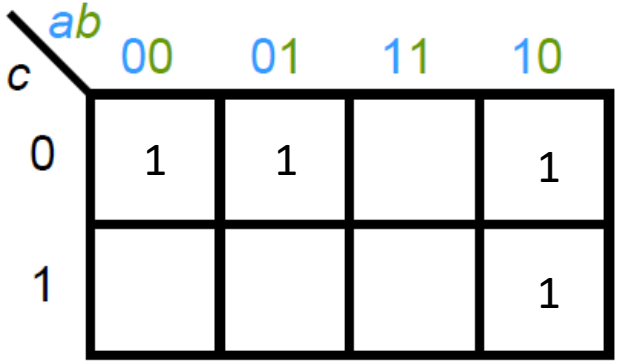
Dynamic hazard!!!

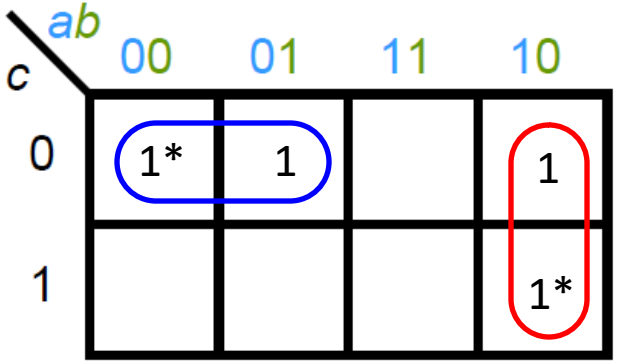
Exercise

Given $f(a, b, c) = \Sigma\, m\,(0,2,4,5)$



a) Minimize the function *f*





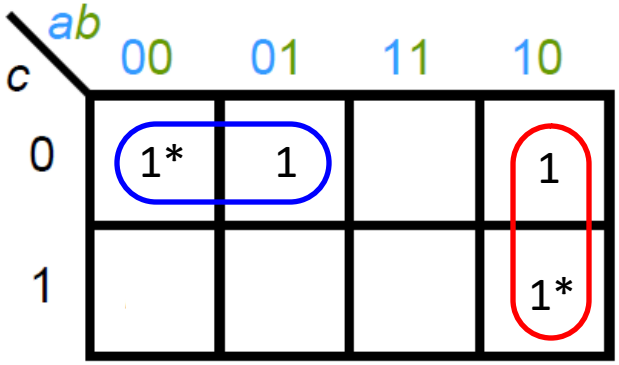
$f(a, b, c) = a'c' + ab'$

Exercise

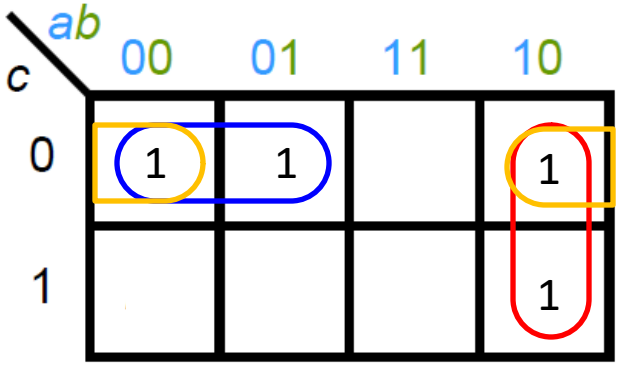
c \ ab	00	01	11	10
0	m_0	m_2	m_6	m_4
1	m_1	m_3	m_7	m_5

Given $f(a, b, c) = \Sigma\, m\,(0,2,4,5)$

b) Realize *f to a* hazard-free circuit



$$f(a,b,c) = a'c' + ab'$$



$$f(a,b,c) = a'c' + ab' + b'c'$$