

EE 2000 Logic Circuit Design
Semester A 2024/25

Tutorial 1

1. Simplify the following expressions using boolean algebra

$$\begin{aligned} \text{(a) } f(w, x, y, z) &= xy + \bar{w}\bar{y}z + \bar{w}x\bar{y} + wxy\bar{z} + \bar{w}yz + wz \\ &= xy + z + \bar{w}x\bar{y} \end{aligned}$$

$$\begin{aligned} \text{(b) } f(x, y, z) &= (x + y + z)(x + y + \bar{z})(x + \bar{y} + z)(x + \bar{y} + \bar{z}) \\ &= x \end{aligned}$$

$$\begin{aligned} \text{(c) } f(a, b, c, d) &= ab + bcd + ab'c' + abd + bc + abc' \\ &= ac' + bc \end{aligned}$$

$$\begin{aligned} \text{(d) } f(a, b, c) &= (a + b + c)(a + \bar{b} + c)(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + \bar{c}) \\ &= (a + c)(\bar{b} + \bar{c}) \end{aligned}$$

2. Given a function $f(x, y, z) = \sum m(0, 2, 4, 6)$

(a) Show the truth table.

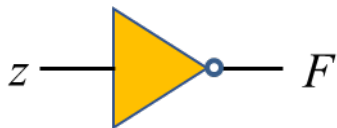
Inputs			Minterms		Output
x	y	z	Term	Designation	$f(x, y, z)$
0	0	0	$x'y'z'$	m_0	1
0	0	1	$x'y'z$	m_1	0
0	1	0	$x'yz'$	m_2	1
0	1	1	$x'yz$	m_3	0
1	0	0	$xy'z'$	m_4	1
1	0	1	$xy'z$	m_5	0
1	1	0	xyz'	m_6	1
1	1	1	xyz	m_7	0

(b) Show the algebraic expression in standard SOP form.

$$f(x, y, z) = x'y'z' + x'yz' + xy'z' + xyz'$$

(c) Show the minimum SOP expression and draw the circuit diagram.

$$\begin{aligned} f(x, y, z) &= x'y'z' + x'yz' + xy'z' + xyz' \\ &= z' \end{aligned}$$



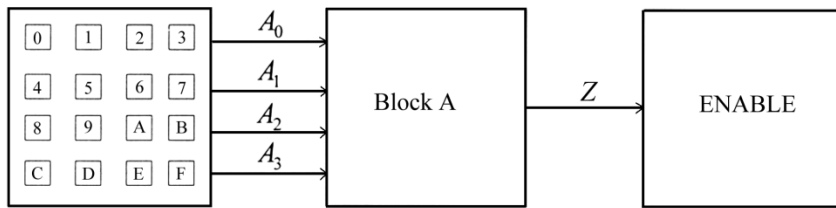
(d) Show the algebraic expression in standard POS form.

$$f(x, y, z) = (x + y + z')(x + y' + z')(x' + y + z')(x' + y' + z')$$

(e) Show the minimum POS expression.

$$\begin{aligned} f(x, y, z) &= (x + y + z')(x + y' + z')(x' + y + z')(x' + y' + z') \\ &= z' \end{aligned}$$

3. A simple locker system that has an output signal $Z = 1$ when the hexadecimal keypad input is either 0, 1, 2, 3, 7, 8, 9, A or E; otherwise $Z = 0$. Assume that $A_3 A_2 A_1 A_0$ represent a 4-digit binary number output from the keypad (A_3 as the MSB). Block A decodes these signals and outputs the signal Z .



- (a) Write down the truth table of Block A.

Input	Inputs				Output
	A_3	A_2	A_1	A_0	Z
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
B	1	0	1	1	0
C	1	1	0	0	0
D	1	1	0	1	0
E	1	1	1	0	1
F	1	1	1	1	0

- (b) Find the SOP and POS expression of Block A.

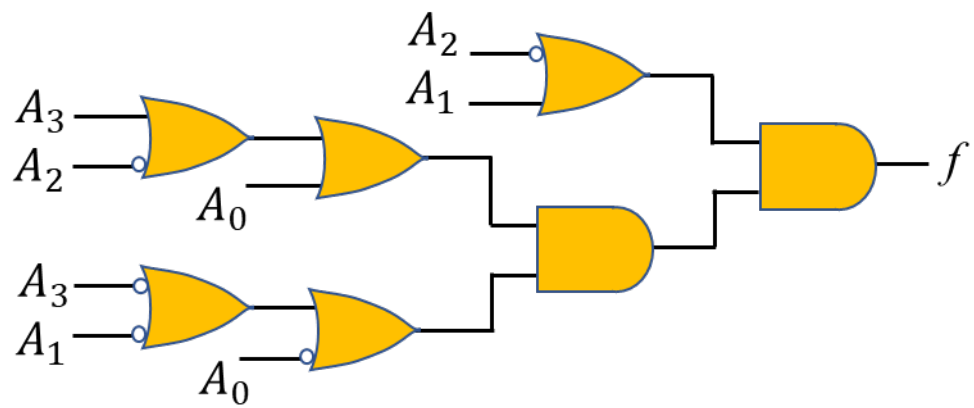
$$f(A_3, A_2, A_1, A_0) = f(w, x, y, z) = w'x'y'z' + w'x'y'z + w'x'yz' + w'x'yz + w'xyz + wx'y'z' + wx'y'z + wx'yz' + wxyz'$$

$$f(A_3, A_2, A_1, A_0) = A_3'A_2' + A_3'A_1A_0 + A_3A_2'A_1' + A_3A_1A_0'$$

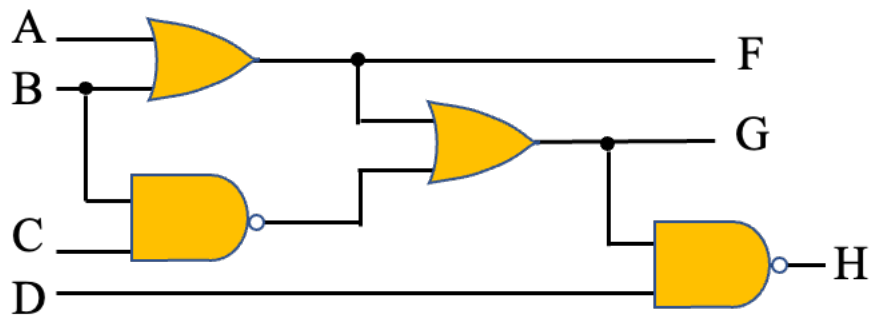
$$\begin{aligned} f(A_3, A_2, A_1, A_0) &= f(w, x, y, z) \\ &= (w + x' + y + z)(w + x' + y + z')(w + x' + y' + z)(w' + x + y' + z')(w' + x' + y + z)(w' + x' + y + z')(w' + x' + y' + z') \end{aligned}$$

$$f(A_3, A_2, A_1, A_0) = (A_2' + A_1)(A_3 + A_2' + A_0)(A_3' + A_1' + A_0')$$

(c) Design the circuit of Block A using minimum number of 2-input AND, OR gates and NOT gates.



4. (a) Derive Boolean functions to describe the operations of the combinational circuit as follow:

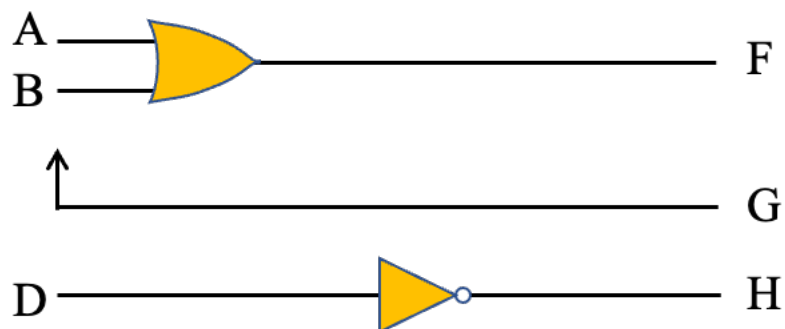


$$F = A + B$$

$$G = (A + B) + (BC)' = A + B + B' + C' = 1$$

$$H = (1 \cdot D)' = D'$$

- (b) Hence, simplify and draw a new logic circuit.



- (c) Redraw the logic circuit with only 2-input NAND gates.

