Date: 2021/06/08

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~6

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (6/8/21)

N-extension dependency?

DoD validation with SAIL, Zephyr OS?

Meeting minutes

Imperas shared short presentation how they test interrupts in verilog testbenches and ISS:

- Discussed external interrupt stimulator/interrupt agent/async event generator which acts as a virtual peripheral and the use of macros in test programs to allow different designs different methods to stimulate interrupts.
- Discussed separating DV testing from compatibility testing.
- Desire for at least some subset of compatibility tests to run on actual hardware/FPGA. and a class of tests that require something generating interrupts.
- Confirm with architectural test group that the direction they are taking still allows for implemented hardware to be tested as well.

Email question: > Is there an update about the RNMI proposal? What is the status of it? Since end of January I don't see anything about it.

- Being covered by Priv group 1.12. Krste will reply to this email.
- Recap: RISC-V already has non-resumable NMI. NMI however stomped bits so was not resumable. Some expressed interest in a resumable NMI. So RNMI proposal adds more CSRs to save state, then can keep going or return. RNMI handler needs more explanation, i.e., the software story of how it works. Feeling that HW RNMI proposal doesn't need to change but software implementation of how it would be used needs to be added.

Discussed CLIC Definition of Done (DoD) status:

- Should we try to move CLIC DoD Moving from kickoff to plan? Where does it fit in roadmap? RISCV has prioritized RVA22 for application type/Linux software world. In the embedded space things are more ad Hoc. Will probably package microcontroller type extension in a profile and ratify as a group, e.g. CLIC, Zfinx, new compressed. p-extension. rv32e. One problem in embedded is the software ecosystem isn't as strong and embedded needs flexibility. So CLIC is still on roadmap but probably next gen riscv grouping. Continue working on issues and refining spec.

Hypervisor support?

- One simple option is CLIC doesn't work with H? Both CLIC and AIA are evolving. CLIC problematic places: table read hardware vectoring. Otherwise no real complication. If systems have both AIA and CLIC, how would it work. Maybe don't need to worry about it? No shipping hypervisor support yet.

Discussion of comparison with other interrupt controllers: AIA, ACLINT, APLIC

- CLIC for embedded space. AIA for hypervisor/like GIC. E.g., AIA doesn't have preemption besides between priv modes.

Discussed issue #156 – will add clarification to spec about how memory apertures are intended.

- Need to revert a previous spec update that removed s/u-mode clic memory mapped region description. Pull #157 created after the meeting to try to revert and clarify.

Github updates since last meeting:

Issue #156 opened. priv/clic mem mapped registers clarification

Issues discussed in meeting:

Specification updates since last meeting:

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#49 – clarification of memory map – closed with pull #129,157? Related to new issue #148, #156

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129, #157?

#79 – supervisor/user mode alignment – closed with pull #129, #157?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

#142 – effect of MPRV and SUM on hardware vector table access. load has to obey MPRV and SUM bits. Added this clarification to the spec 05/25/2021.

#149 – 32-bit writes to memory-mapped CLIC registers. need to add to spec: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect.

#156 – Clarify isolation mechanism over CLIC memory mapped registers, related to #77? Fixed with pull #157?

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec

#107 – heritage of features

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#99, 100, 101, 102, 103, 106 – enhancements for future versions?

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#148 – Elaborate address map possibilities

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

Issues related to work in other TGs:

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#108 – pushint/popint?