Date: 2022/05/24

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 4

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (06/07/22)

Easy?:

Pull #218 – clicintattr typo fix

Pull #198 (issues #197/#232) - xRET SAIL-like pseudo-code

#214/#215 – mscratchcsw pseudo-code clarification.

#212,213/pull #216 – parameter text fix/clarification

#220 – ok to generate exceptions to clic mem mapped regs?

Longer review:

Discuss issue #29/pull #190 – clicinttrig

Discuss #195/pull #196 – clarification of intthresh and xstatus.xie

Discuss xcliccfg pull. (for issue #96) - mcliccfg/scliccfg/ucliccfg

Discuss #211 – xnxti side effects

Discuss #160/#200/pull #201 – user mode interrupts

Discuss mlvl proposal (#226 – formerly #96) - wait for community feedback

#191 – question about sw vectoring now that hw vector table can be execute only. (discuss with krste)

Meeting minutes

No discussion of issues because Krste couldn't attend. Discussed Dev partner support and SAIL. Created new issue # 242 – is spike support is required if SAIL is waived.

Github updates since last minutes:

Specification updates since last minutes:

Issue #225 – bounded time to respond to interrupts

Issue #233 – mnxti pseudo-code clarification (added meaning of clic.priv,clic.level,clic.id)

Issue #235 – change "exception" to "trap" to match priv spec wording.

Open issue status:

Issues that can be closed? (simpler **issues to discuss in blue)**

#29/#155 – clarify inttrig details. Created Pull #190. debug spec added tmexttrigger.intctl to support triggers from attached interrupt controllers. Will this provide the desired tightly integrated behavior? Need to mention behavior in clic spec, e.g., breakpoint before 1st instruction of interrupt executed?

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

#197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv. Also closes issue #232?

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

#214/pull #215 – xscratchcsw pseudo-code (similar to #197 pseudo-code)

#195 – update spec to allow implementing a minimum number of bits of intthresh. Close with pull #217? 1 bit implemented: interrupts can be set to 255 or 127. xintthresh needs to be set to 255 to block all, 127 to block ints at 127, a smaller number to allow all interrupts. with 2 bits xintthresh, can set to 255, 191, 127, 63.

#202/pull #238 –writes/reads to clic mem mapped registers. (discuss if 64b store ordering is required. Pull is different from TG discussion)

#212 – NUM_INTERRUPT parameter values. Close with pull #216?

#213 – how does CLICMTVECALIGN match AIA and code-size reduction. Close with pull #216?

Pull #218 – easy clicintattr typo fix

#232 – return addr computation – Close with pull #198?

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve usage of immediate bits (0-UIE?),2,4 in xnxti imm usage since those mstatus bits are WPRI. Related to #205/211

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#239 – Dret should honor inhv

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0).

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

#191 – reopened. question about sw vectoring.

#205 – xnxti side-effect question. `csrrsi rd, mnxti, uimm[4:0]`. Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interupt). Is this restriction necessary? Related to #100/#211?

#211 – xnxti text vs. Pseudo-code clarification required. Related to #100/205?

#219 – Interrupt ID ordering recommendations

#220 – Access to reserved address space – OK for implementation to generate access fault (not required but allowed?)

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63?

#222 – legacy s-mode/u-mode timer interrupt setup

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#228 – dpc treatment - can breakpoints be set in hw vector table? (related to #230). Code-reduction TG chose to not allow setting breakpoints on hw vector table. https://github.com/riscv/riscv-code-size-reduction/issues/161

#229 – clicintattr.mode WARL behavior (moot if #226 accepted)

#230 – can hwvector table loads be interrupted by higher priv interrupts? Can table load be interrupted by debug mode? so dret should check xcause.xinhv to interpret dpc correctly? Related to issue #228.

#239 – dret should honor inhv.

#240/pull #241 – change mscratchcsw to use mstatus.mpp in pseudocode?

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1