Date: 2021/07/06

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~7

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (7/20/21)

More open issue discussion?

Meeting minutes

N extension dependency – N extension is not ratified. If N extension goes ahead to get ratified, it would need a task group. Can see use cases for embedded traps, e.g. floating point trap and other traps that don't need to go to the system level, but it is more theoretical because there is no existing widespread use. Interrupt priv levels are useful but can bare s-mode be used instead of u-mode? If there are valid use cases, interested members should push for task group.

For CLIC, write clic spec to not presume n exists and add commentary if N existed how it would affect CLIC so if N gets ratified, CLIC is compatible.

Discussion of TEE group WX after m-mode lockdown and whether CLIC vector tables would ever need to be WX. After meeting Bill Huffman sent email with summary: CLIC does not have any need because vector tables are read and used as an entry point address.

Discussed #158 – if CLICINTCTLBITS parameter is writable, spec would have to define what happens when it is changed. Could have CLICINTCTLBITS in discovery method and fixed at boot time. Bill Huffman to review text and locate text that limits making CLICITCTLBITS flexible, e.g. Changed section 6 to say clic parameters instead of clic imp. Parameters.

Discussed #80 - Current ask is that things that are discoverable. add a section of what is discoverable. e.g. Section 6 parameters section. Discovery TG is asking to list the set of discoverable parameters for the extension so should probably remove clicinfo, clicbase since it will be replaced with discovery mechanism). add sclicbase, uclicbase parameters.

Closed #156/77/79 - memory map text clarifications

Github updates since last minutes:

#160 - can rewrite to allow for but not assume n-extension is available.

Specification updates since last minutes:

#158 – changed CLIC Implementation parameters to CLIC Parameters to not assume the parameters are always hardwired.

#156/77/79 – CLIC memory map text clarifications.

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129, #157?

#79 – supervisor/user mode alignment – closed with pull #129, #157?

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Update text to clarify when interrupt is set to 0.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#107 – heritage of features. keep researching and adding references to bibliography

#148 – Elaborate address map possibilities. Platform should be doing the layout.

#154 – inhv clarifications

#156 – Clarify isolation mechanism over CLIC memory mapped registers, related to #77? Fixed with pull #157?

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#102 - preemptible interrupt handler code (for section 7.2)

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#158 – add option to reuse unused clicintattr.mode bits with clicintctrl to determine level value when 3 modes are supported but only 1 or 2 modes are selected by clicctrl.nmbits?

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?