Date: 2023/03/14

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 4

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (03/28/23)

Pull #297/ parameter discussion.

Meeting minutes

#295/pull #310 – clear xintthresh on priv changes. Added additional text clarification after implementing pull.

Discussed issue #309 – NMI interrupt level. Added text in CLIC about NMIs.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red)**

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Issue #290: non-aligned access to hw vector table. In TG meeting decided to create a pull to create a trap.

Issue #304 – will try to re-write how mem-mapped registers . platform can mandate to 4k boundaries if it is virtual memory but spec can leave it open. use same language as in m-mode.

#307 – NUM_INTERRUPT listed in two sections (text cleanup)

#311 - for cliccfg could put fields in different places in the word. put in one word with the byte for each priv mode. high byte is m mode, low byte is u-mode. byte 1 is s-mode.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

#304 – clarify changes to CLIC memory-mapped registers

#308 – xnxti service loop behavior

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – spike required if sail is waived?

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).