Date: 2021/09/28

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~8

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (10/12/21)

More open issue discussion?

Meeting minutes

Discussion of #96/pull #171.

CLIC spec suggests an implementation of memory map apertures (aliasing the same physical CLIC memory-mapped registers to different address ranges, with each address range given different permissions for each privilege mode) to allow for allowing privileged access to CLIC memory mapped registers without needing to pass priv mode info along with bus transactions.

With mcliccfg at 0x0000 and mclicint at 0x1000, scliccfg 0x2000, sclicint at 0x3000, ucliccfg 0x4000, uclicint at 0x5000, 24KB of memory map is used for 3 modes using memory map apertures (32KB when reserving space for HS). It may be desirable to reduce the memory map footprint and overlap the clic apertures, where the assumption is bus transactions carry priv mode attributes and and the clic interface modifies behavior based on bus transaction priv mode. For example with a core with only 32 interrupts, the CLIC memory map can be reduced to 0x0 thru 0x1080, or slightly more than 4KB, representing 4 cliccfg, 1 clicinfo and 32 clicint 32-bit memory mapped registers.

Since m-mode may need access to m/s/ucliccfg, it is helpful for the memory map overlapping if m/s/ucliccfg are not all at offset 0x0.

Pull #171 fit {uclicfg,sclicfg,mclicfg} in different bytes at 0x0 but TG discussed that this left little room for future fields.

One proposal is to put mcliccfg at 0x0, hscliccfg at 0x400, scliccfg at 0x800, ucliccfg at 0xC00. This does mean that code that doesn't know what mode it is in needs to get pointer offset to know where to program xcliccfg.

Would need to add explanation why overlapping vs. Non-overlapping apertures in the spec.

Github updates since last minutes:

Issue #171 created – CLICCFGLBITS parameter

Pull #172 created – m/s/ucliccfg pull for issue #96

Pull #173 created – xtvec clarification for issue #45

Pull #174 created – xnxti clicintip clarification for issue #48

Pull #175 created – parameter/general discovery comments for issue #80

Pull #176 created – inhv clarification for issue #154

Specification updates since last minutes:

Added link to development state definitions to CLIC title page (https://wiki.riscv.org/display/HOME/Specification+States)

Open issue status:

Issues that can be closed?

#148 – Elaborate address map possibilities. CLIC Memory map section has s/u memory maps added back and clarification that addresses can be used to limit different privilege access. Is this sufficient to close?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #173 tries to close.

#48 – logic/state diagram for clicintip signals (related to #149?), add more clarification about hardware clearing of IP bits. only xnxti writes can clear IP bits. Pull #174 tries to close.

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too? Pull #175 tries to address until platform discovery solidifies.

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Pull #172 tries to close

#107 – heritage of features. keep researching and adding references to bibliography.

#154 – inhv clarifications. Pull #176 tries to close.

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#97 – proposed reformat of xcause CSRs

#102 - preemptible interrupt handler code (for section 7.2)

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Pull #144 also tries to clarify behavior when interrupt level is set to 0.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#29/#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#171 – CLICCFGLBITS parameter

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?