Date: 2021/06/22

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~7

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (7/6/21)

N-extension dependency?

DoD validation with SAIL, Zephyr OS?

#158 – clicintctlbits may not always be fixed.

Meeting minutes

Jeff Scheel RISC-V program manager introduction.

Discussed issue #156 – pull request to add clarification to spec about how memory apertures are intended.

- Added pull to spec. Still need to fix text – memory does not contain priv, memory access. Need to add spec update to rev history.

Reopened #154 – question about if inhv hardware behavior is needed? clarification on which xinhv is being checked on xret. e.g. sret checks uinhv?

- Need to add text to clarify when hw vectoring starts, uie is cleared so sret restores uie to cleared state. so hw to load table vector is still required. add to text next to permissions-checking purposes.

Closed #139 – gpr shadow sets – closed. general trend away from this due to cost/power. probably push/pop would be better.

Closed #140 – automated GPR save/restore - closed. if add push/pop instructions.

Add future enhancement label to #99/101/106

Closed #103 – closed. interrupts are a use-case. try to bring up in bitmanip or code size TGs.

Closed #142 - closed with update 5/25

Closed #149 – 32-bit writes to memory-mapped CLIC registers. need to add to spec: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect. closed with spec update.

Closed #49 – clarification of memory map – closed with pull #129,157? Related to new issue #148, #156. closed with pull #157

Discussed #120/ pull #144 – if a machine interrupt is set to 0. need to update pull text. hw is going to mask the lower privilege modes. Pull text reads like there a level 0 interrupt is a possibility.

Github updates since last meeting:

Issue #154 reopened.

Issue #156 opened. priv/clic mem mapped registers clarification.

Issue #158 – clicintctlbits – valid to make a variable that changes with nmbits?

Specification updates since last meeting:

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129, #157?

#79 – supervisor/user mode alignment – closed with pull #129, #157?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Update text to clarify when interrupt is set to 0.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#107 – heritage of features. keep researching and adding references to bibliography

#148 – Elaborate address map possibilities. Platform should be doing the layout.

#154 – inhv clarifications

#156 – Clarify isolation mechanism over CLIC memory mapped registers, related to #77? Fixed with pull #157?

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#102 - preemptible interrupt handler code (for section 7.2)

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#158 – add option to reuse unused clicintattr.mode bits with clicintctrl to determine level value when 3 modes are supported but only 1 or 2 modes are selected by clicctrl.nmbits?

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?