Date: 2023/01/31

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (02/14/23)

Meeting minutes

BIG SPEC rewrite. No functional change intended. Please review!

Reviewing pull to split into sections. Make revision not a numbered chapter.

In future, switch to start in u-mode, then s-mode then m-mode. what are the granularity of options we want to specify. e.g. xscratchcsw/l. probably don't want too many options. want to group things together. clic special csrs don't add much cost. maybe base and extended?

Base: everything but hardware vectoring.

Extended: vectored.

We don't do hardware stacking of contexts. might be later extension. we have hardware vectoring.

Next step figuring out the options.

Please review. No functional change intended. We can always go back if we need to and try again.

Discussed #290 based on question about previous comments. added additional comments. keeping closed.

Talked about status of sig arch-test tests. TG for the spec is splitting doc into two sections.

Created new issue #293 for adding separate cliccfg for other priv modes. closing #49, #96.

Discussed WFMI status (mentioned in CLIC spec under WFI section). no one pushing it but it could be a fast track if anyone wants. (new WFMI instruction - wait for mode's interrupts · Issue #700 · riscv/riscv-isa-manual · GitHub) on wfmi branch.

Discussed #221 – ok to have bitmap view but should be done with memory-mapped access. Don't add CSR access to these bits. this would represent alternative view of the same bits. seems ok. add reference to prior art in bibliography.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red)**

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#**293** – mcliccfg/scliccfg/ucliccfg (cliccfg in each priv mode to be able to control cliccfg.nlbits separately)

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).