Date: 2021/12/21

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (01/04/22)

More open issue discussion? Discuss if pulls resolve discussed issues.

#97 – proposed reformat of xcause CSRs (bigger discussion).

Meeting minutes

Add SAIL, Architecture test development, QEMU updates as issues? probably good idea. created issues #185,#186, #187 for tracking these definition of done work items.

#180 closed.

#109 – closed. FYI, krste has been working on profiles documents. the way arch spec is written, needs restructuring to make it work with profiles. may need to define a sslic for software

#45/#173 – missed august 17 comments. need to rewrite pull.

#49/ pull #96 – pull adds scliccfg/ucliccfg to memory map. pull only gives nlbits control to scliccfg/ucliccfg. should scliccfg be able to control some portion of nmbits? Proposal to have a boundary value setting instead of Nmbit that is compared to a 10-bit levels value. value, e.g. 60 where 60,61,62,63 are identified as m-mode interrupts but others handled in lower modes. then s-mode choses a boundary value between s-mode and u-mode. so would no longer have mode bits. all by level. this would be more flexible than previous scheme. More discussion/flushing out needed.

Github updates since last minutes:

Fixes for #109/ #180

Specification updates since last minutes:

Pulls to fix #109/#180

Open issue status:

Issues that can be closed?

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #183? need more discussion?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #173 updated with fixes for comments. need to update for Aug 17 comments.

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#107 – heritage of features. keep researching and adding references to bibliography.

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value?

#97 – proposed reformat of xcause CSRs (bigger discussion).

#102 - preemptible interrupt handler code (for section 7.2)

#29/#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#171 – CLICCFGLBITS parameter - related to #80, #158.

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1?

Issues need to be worked:

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

Issues related to work in other TGs:

#91 – DTS entry – have linux group review DTS example.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?