Date: 2021/09/14

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~8

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (09/28/21)

More open issue discussion?

Meeting minutes

Discussed meaning of clicinfo.num_interrupt field vs. Section 6, CLIC Parameters CLICMAXID/NUMINTERRUPT. Will we need clicinfo in the future or use a platform discovery mechanism? (issue #80)

Xintthresh is lsb. updated spec and closed #170.

Discussed pull #168. Implemented. Need to add text to describe how to calculate how many bits are available for level/priority. total bit count. subtract #mode bits to get #level bits. documented in open issue #158

Pull #169 implemented. xnxti pseudo code clarification added to spec.

Discussed #96 – makes sense different priv modes may want different level/priority control. mcliccfg, scliccfg, ucliccfg instead of single cliccfg. use similar aperture access mcliccfg/scliccfg read 0 in u-mode. larger spec change, small hw change. add a little bit of mux logic at end of comparison tree.

Github updates since last minutes:

#170 – xintthresh

#169 – xnxti description pull

#168 – clicintctl/nlbits pull

Specification updates since last minutes:

#170 – updated xintthresh.th description – clarified it is lsb 8 bits of register

#169 – xnxti description pull

#168 – cliccfg.nlbits only 0 or 8 level bits are currently supported. Other values reserved.

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches.

#48 – logic/state diagram for clicintip signals (related to #149?), add more clarification about hardware clearing of IP bits. only xnxti writes can clear IP bits.

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#96 – proposed reformat of cliccfg. bit spec change, small hw change.

#107 – heritage of features. keep researching and adding references to bibliography.

#148 – Elaborate address map possibilities. Platform should be doing the layout.

#154 – inhv clarifications

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#97 – proposed reformat of xcause CSRs

#102 - preemptible interrupt handler code (for section 7.2)

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Tried to update pull text to clarify when interrupt is set to 0.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down.

E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?