Date: 2022/04/12

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 8

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (04/26/22)

#191 – treat vector table with inst fetch permissions?

Discuss if can close #97

Planning on splitting mcliccfg/scliccfg. Split #96 into 2 issues: 1. xcliccfg 2. mlvl proposal

Discuss issue #29/pull #190 – clicinttrig

Discuss #195/pull #196 – clarification of intthresh and xstatus.xie

Discuss #197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

Discuss #160/#200/pull #201 – user mode interrupts

Meeting minutes

#206 pull/#208 issue – Note that FENCE.I may be needed to keep icache fetch with dcache. Related to https://github.com/riscv/riscv-code-size-reduction/issues/134. (related to closed clic issue #191). reopened #191 and put these comments. Will create a pull to match Zc and discuss more next time.

The inconsistency of NOTE requiring FENCE.I #206 whereas the access was considered a data access was noted. Either this requirement should be dropped (meaning hardware has to fetch from table coherent with data access) or the table access should be treated as an instruction fetch (as in the code size reduction table jump instructions `cm.jt` and `cm.jalt`).

Unifying the models between Zce and fast interrupts table lookup should simplify hardware implementations. Table lookups would not be affected by mprv/sum as they are now treated as instruction fetches. Emulation of the table lookup could not use mprv/sum, as that only models

load/store permissions not fetch permissions. Modifications to the table would require a FENCE.I.

Github updates since last minutes:

Issue #222 – legacy s-mode/u-mode timer interrupt setup

Issue #223 – mtval=0 still CLIC compliant?

Issue #224 – section 5.6 xepc CSR text

Issue #225 – clicint memory mapped details – bounded time/effects. related to #202 that more memory mapped behavior needs to be clarified.

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (simpler **issues to discuss in blue)**

#29/#155 – clarify inttrig details. Created Pull #190. debug spec added tmexttrigger.intctl to support triggers from attached interrupt controllers. Will this provide the desired tightly integrated behavior? Need to mention behavior in clic spec, e.g., breakpoint before 1st instruction of interrupt executed?

#197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

#214/pull #215 – xscratchcsw pseudo-code (similar to #197 pseudo-code)

#195 – update spec to allow implementing a minimum number of bits of intthresh. Close with pull #217? 1 bit implemented: interrupts can be set to 255 or 127. xintthresh needs to be set to 255 to block all, 127 to block ints at 127, a smaller number to allow all interrupts. with 2 bits xintthresh, can set to 255, 191, 127, 63.

#218 – typo fix (dependent on #96 resolution)

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve usage of immediate bits (0-UIE?),2,4 in xnxti imm usage since those mstatus bits are WPRI. Related to #205/211

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #96 first)

#202/pull #203 – generalize statement about 32-bit writes to clic mem mapped registers. Need to update pull based on TG discussion

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #183? Dependent on issue #96 discussion.

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #204 to go thru change implications.

#97 – proposed reformat of xcause CSRs (bigger discussion). Think some assumptions might be wrong. to discuss with John Hauser.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0)..

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #96 first)

#205 – xnxti side-effect question. `csrrsi rd, mnxti, uimm[4:0]`. Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interupt). Is this restriction necessary? Related to #100/#211?

#208 – add note about fence.i required after modification of the hardware vector table? Close with pull #206?

#211 – xnxti text vs. Pseudo-code clarification required. Related to #100/205?

#212 – NUM_INTERRUPT parameter values. Close with pull #216?

#213 – how does CLICMTVECALIGN match AIA and code-size reduction. Close with pull #216?

#219 – Interrupt ID ordering recommendations

#220 – Access to reserved address space – OK for implementation to generate access fault (not required but allowed?)

#221 – compressed clicintip status registers (1-bit per interrupt) similar to AIA eip0-eip63?

#222 – legacy s-mode/u-mode timer interrupt setup

#223 – mtval=0 compliant

#224 – section 5.6 xepc CSR text

#225 – clicint memory mapped details – bounded time/effects

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1