Date: 2021/10/12

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~9

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (10/26/21)

More open issue discussion?

Meeting minutes

Philosophical Interrupt testing question. Fake interrupt testing device. Need a way at a future time an event will be generated. interface is a macro probably be a memory mapped widget. as long as interface is a macro that implementor can define. one possible implementation is a csr write. e.g. Use for SAIL. spike can do that too. some CSR that can normally cause a trap. trap handler redirects. most environments can handle a memory map. testbed implementation issue.

Mock-device at a memory map that can see write to memory. macro is the interface. in SAIL can you call an external function, like floating point. if have tests that don't need the macro. some you want to cause interrupts and multiple interrupts. expose retired counter so can have device schedule when event happens.

Issue #177 – instead of requiring nlbits/nmbits reset values, make it a platform-specified option. platform-specific means it is dependent on the platform, platform-defined means in addition, behavior must be defined by the platform. platform can't be agnostic. can make a statement it can be random. platform-defined is a subset of platform specific. nlbits should reset to a legal value. looking at CLIC mandatory reset state, only xintstatus.xil resets to 0 seems mandatory.

Discussed execution environments. u/s/m – what firmware sees. updating description in priv spec. e.g. x86 running riscv s-mode is a riscv platform.

Discussion of #148/#96 – 0x800 – 0xFFF custom. suggestion is if you want to overlap regions, use custom region. Closing #148 to point to #96 for continued clic memory map region discussion.

Discussion of #80/158 - should determine what are the basic parameters from which others can be determined in Chapter 6 parameters. clicinfo goes away and instead use whatever the discovery mechanism is.

Github updates since last minutes:

Issue #177 created, spec updated, issue closed – nlbits and nmbits reset requirements

Issue #148 – closed and pointed to #92.

Specification updates since last minutes:

Updated for issue #177 – reduced mandatory reset requirements. Only xintstatus.xil is required to reset to 0.

Open issue status:

Issues that can be closed?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #173 tries to close.

#48 – logic/state diagram for clicintip signals (related to #149?), add more clarification about hardware clearing of IP bits. only xnxti writes can clear IP bits. Pull #174 tries to close.

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too? Pull #175 tries to address until platform discovery solidifies.

#96 – proposed reformat of cliccfg. bit spec change, small hw change.

#107 – heritage of features. keep researching and adding references to bibliography.

#154 – inhv clarifications. Pull #176 tries to close.

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#97 – proposed reformat of xcause CSRs

#102 - preemptible interrupt handler code (for section 7.2)

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Pull #144 also tries to clarify behavior when interrupt level is set to 0.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#29/#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#171 – CLICCFGLBITS parameter - related to #80.

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?