

Date: 2023/03/28

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 5

Meetings Disclaimers Video :

[https://drive.google.com/file/d/1y\\_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view](https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view)

Current issues on github: <https://github.com/riscv/riscv-fast-interrupt/issues>

Previous meeting minutes: <https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes>

Fast Interrupt DoD (Definition of Done) Status: (new location)

<https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG>

### **Next meeting agenda (04/11/23)**

Issue #314 – shv==0 requirement for xnxti

Issue #308 – xnxti service loop

Issue #290 – instruction fetch exception. Reference priv spec wording to create pull.

Pull #297/ parameter discussion. if parameters are accepted, update cliccfg section to say how the configs affect those parameters. clean up #307 also (NUM\_INTERRUPT listed twice)

### **Meeting minutes**

SAIL interrupt expert. will help implement AIA, PLIC, CLIC in SAIL.

Discussing #314 – in section 11.1 handler code – issue is software vs. Hardware vectoring has different ABI? will continue discussing to see if a change would break assumptions.

Implemented pull #313 for issue #295 – DRET clears xintthresh too.

Pull #312 for issue #304 – mem map alignment requirement text cleanup. merged. Added additional text cleanup.

Pull #316 for issue #311 – xcliccfg.nlbit layout change. merged and edited. since this is a big cliccfg format change, it isn't backward compatible so went ahead and shifted nlbit to be 3:0 instead of 4:1 of each priv byte.

### **Github updates since last minutes:**

### **Specification updates since last minutes:**

### **Open issue status:**

Issues that can be closed? (Simpler issues to discuss in red)

### **Need spec updates:**

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Issue #290: non-aligned access to hw vector table. In TG meeting decided to create a pull to create a trap.

#307 – NUM\_INTERRUPT listed in two sections (text cleanup)

Issue #314 – shv==0 requirement for xnxti

### **Need more discussion:**

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvi proposal (formerly #96)

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

#308 – xnxti service loop behavior

### **Issues need to be worked:**

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – spike required if sail is waived?

### **Issues punted for rev1, keep open for future enhancements:**

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

**#192** – allow mix of CLIC/CLINT at different priv modes punted for rev1

**#248** – CLIC hypervisor mode (related to #92).