Date: 2023/01/17

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 5

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (01/31/23)

#291 – single-stepping, can this be closed? Clarification needed?

#290 – non-naturally aligned access to the trap vector table, xret, inhv

#289 – semantics of reserved CSR accesses (can it be closed in clic since moved to priv spec?)

#247 – discuss more details on text clarification required? MPP and V=0 pseudo-code update?

#49? can what is remaining be moved to a new specific issue?

#255/pull #288 – clic/clint interaction (reopened)

#221/pull 270 – clicintie/ip summary regs.

Meeting minutes

Discussed #247- plan to add clic support of hypervisor mode would added as another extension option section so we can get ratified. Still need to break CLIC into different extension options anyway. Also need to rewrite CLIC spec so it can be more clean as to what is in each priv mode. software usually written in 1 mode at a time. so when writing extensions, write how it appears to each mode. e.g. what does s-mode see. e.g. hw counters. if low level machine turns it off, they disappear from s-mode. what is available at each priv mode is different and needs to be called out separately. most things are unpriv and available in all modes. but for things that aren't available in every mode or conditionally turned on. e.g. when all interrupts are m-mode, then it is like there is no clic in s-mode. so call those out as options. in other specs, found priv spec has a lot of optionality, but need give options names and concisely describe options and interactions between options (this implies this, etc.) so ignoring hypervisor for now, CLIC spec should be smclic, ssclic, suclic (when u-shows up). and describe what is visible.

Separate out features by mode it is in. document behavior. spec should be defined lowest mode up. what user mode expects. what supervisor mode changes to user-mode. higher mode have responsibility for what lower mode expects. ssstateen, smstaten. deleg registers. higher mode delegates to lower mode. Tagged issues #247, #248 as post 1.0.

#291 – single-stepping with mnxti. no change needed. closed.

#290 – xret with inhv. some implementations, natural thing would be to get trap. automatically masking off bits, some would be easier to mask, some would be easier to trap. trap is easier case. Closed.

#289 – don't trap on reserved. reserved is catch-all for don't do it and if you do it anything can happen. closed.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red)**

Need spec updates:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 **–** hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#247 – behavior when MPP is two-bits and hypervisor not implemented

#248 – CLIC hypervisor mode (related to #92).