Date: 2022/11/08

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (11/22/22) ?? Thanksgiving week may be cancelled.

Pull #281 – simple hypervisor proposal

#221/pull 270 – clicintie/ip summary regs.

#286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Meeting minutes

FYI, CLIC Summit presentation:

RISC-V Summit 2022: Update on Fast Interrupt Task Group (CLI... (sched.com)

Update on Fast Interrupt Task Group (CLIC Since Barcelona 2018 Wednesday, Dec 14, 2:20pm-2:40pm

Pull #285 commited. Note that all csr addresses might change during ratification.

Pull #284 commited. moved mclicbase to parameter.

Pull #287 commited. issue 235 closed.

Pull #283 committed.

Pull #273 committed.

Discussion of pull #286. if things can be reconfigured on the fly, corner cases occur. could have configuration has a lock bit that can't change without a reset?

Another way of writing it up, design has these parameters, just a platform issue of how they are setup.

If the config is something people want, they will want to standardize it. adding flexible levels adds complexity, more corner cases but gives more levels where you need them. saves hardware cost. Independent of the scheme, we should be clearer on dynamically changing things. e.g. cliccfg.nmbits/nlbits. if it is changeable, it has to be setup and frozen before use. we don't currently describe what happens when it changes. Add something to reset setion. set it and lock it (boot time can setup a configuration).

Better instead of putting everything in platform parameters. try to mention what is runtime variable and what is intended to be configurable.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red)**

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270

Need spec updates:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#247 – behavior when MPP is two-bits and hypervisor not implemented

#248 – CLIC hypervisor mode (related to #92).

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1