Date: 2023/04/11

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (04/25/23)

Issue #314 – shv==0 requirement for xnxti

Issue #308 – xnxti service loop

#322 – xcliccfg field text cleaning. text needs to be cleaned up due to newly added fields.

Pull #297/ parameter discussion. if parameters are accepted, update cliccfg section to say how the configs affect those parameters. clean up #307 also (NUM_INTERRUPT listed twice)

Meeting minutes

Fast interrupt TG annual election status:

3/31 - Priv IC chairs putting forward to the TSC for its approval the following:

Chair Dan Smathers

Vice-chair Jean-Baptiste Brelot Jean-Baptiste.Brelot@nordicsemi.no

Jean-Baptiste (JB) Brelot Biography: He has more than 15 years experience with designing processors for low power microcontroller applications at Arm, where he has been involved in the design and verification of most Cortex-M cores from the M0+, M7 and onwards. Currently at Nordic Semiconductor.

Fast interrupt spec open for a long time. goal to ratify what we have at the moment.

ACT sig has new chair (James Shi from Alibaba). options add complexity for testing.
SAIL interrupt development (AIA, CLIC, PLIC) - Saravana Kumar - saravanatnj.sit@gmail.com recent grad. Bill McSpadden is helping ramp him up. starting on timer interrupts.

Discussed pull #323 for #290 – should it be may raise address-misaligned exceptions vs must raise. Or should HW just zero the lsb 2 or 3 bits. hardware generated address. just ignoring the bits is probably

the easist implementation. Decided to merge pull and make edits to change to ignoring the lsb bits. closed.

Implemented pull #324 for issue #318. changed x0 references to zero.

Issue #320 – create a pull to add text – e.g. similarly adding mnstatus.mpp to nmcause

Issue #321 – change text to say setting xintthresh to minimum (e.g. no masking of interrupts) since some implementations may not implement all the xintthresh bits.

Issue #317 – will add a comment to the trampoline examples that it doesn't account for the presence of f registers. Created pull #326

Issue #308 – mnxti relies on mcause.pil. in service_loop. goal of tailchaining is to do all irqs above code that was preempted. former interrupt level gets put in pil. goal of service_loop is do all that were greater than preempted. loop tries to handle all irqs above that il. if gets interrupted by hw, stomps on mcause.pil. Hw vectored irq would have to save and restore mcause. Created pull #325.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

#308/pull #325 – xnxti service loop behavior

#317/pull #326 – clarification of trampoline examples

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

#307 – NUM_INTERRUPT listed in two sections (text cleanup)

Issue #314 – shv==0 requirement for xnxti

#320 – clarify CLIC with RNMI

#321 – clearing xintthresh when fewer than 8 thres bits are implemented.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

#322 – xcliccfg field text cleaning. text needs to be cleaned up due to newly added fields.

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – spike required if sail is waived?

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).