Date: 2022/01/18

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 7

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (02/01/22)

Discuss issue #29/pull #190 - clicinttrig

Plan to discuss #96 – option was considered where the boundary between levels was a value instead of done by fixed number of bits.

Discuss new comments for #186 CLIC arch tests - "arch-test SIG is supposed to be designing infrastructure to test interrupts. we'd appreciate any thought on what this TG thinks is necessary."

More open issue discussion? Discuss if pulls resolve discussed issues.

Meeting minutes

Discussed github automation to auto generate pdf. Stephano will add notes on using github submodules (e.g. docs-resources @ 6a2d5b1) to https://github.com/riscv/docs-spec-template

Discuss issue #191: hw vector memory access load vs. Zc* requiring execute permission.

- Zc is almost frozen. fast-int group expressed some concern with treating table fetch as instruction fetch. mpriv isn't affected by instruction fetch. mpriv allows emulation of supervisor hardware vectoring where it isn't supported by the hardware (although it is a rare corner case). Also, usually the tables want to be writable with loads and stores. maybe table is kept in a data area without execution permission. Closed issue #191 and continuing discussion in Zc github: https://github.com/riscv/riscv-code-size-reduction/issues/134

Add post-v1.0 label to issue #82, #100, #108?

- Closed #82. created new post-v1.0 issue (#192) for supporting different clic/clint at different priv modes.
- Discussed #100 – issue asks for reserving side effects of xnxti. can't just put post-v1.0 label because asking to reserve operation. benefit of following proposal in issue is to

constrain FW to only choose valid mstatus immediate values in xnxti. Could say only these encodings are defined currently. probably ok to constrain. try to create a pull.

- Leave #108 as is with no label for now.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

#29/#155 – clarify inttrig details. Created Pull #190. debug spec added tmexttrigger.intctl to support triggers from attached interrupt controllers. Will this provide the desired tightly integrated behavior? Need to mention behavior in clic spec, e.g., breakpoint before 1st instruction of interrupt executed?

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve immediate bits in xnxti usage

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #183? Dependent on issue #96 discussion.

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more.

#97 – proposed reformat of xcause CSRs (bigger discussion). Think some assumptions might be wrong. to discuss with John Hauser.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0)..

#171 – CLICCFGLBITS parameter - related to #80, #158.

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1