Date: 2020/11/24
Task Group: Fast Interrupts
Chair: Krste Asanovic
Co-Chair: Kevin Chen
Number of Attendees: ~10
Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues
Previous meeting minutes:
https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Issue discussed:

#108 usefulness of PUSHINT/POPINT

> These new instructions will not significantly increase the speed (except reducing cycles if there are wide memory buses). Also, they will not reduce much code size because people can always use selective-hardware-vectoring mode to jump to a common code. Therefore, maybe it is not worthwhile to allocate precious opcode space for these new instructions.
>
> Nevertheless, decided to log the messages in the discussion group into a github issue (#108) for further and more extensive discussion in the future.

#50 xcause save privilege modification bits

> MPRV is used for emulation of missing load/store instructions, and is usually run with interrupts disabled. If disabling interrupts is not acceptable, one approach is to delegate illegal instruction exceptions to lower privilege mode using medeleg.
>
> SUM is only for systems with supervisor mode. SUM only affects M-mode if using MPRV. Currently only affects page-based translation though there is a proposal to add S-mode PMPs, which would be possibly affected by SUM. Original usage model for SUM assumed that supervisor-mode interrupts would be off while SUM was turned on. If interrupts can be enabled while SUM is being used, then handlers have to save SUM, set/clear SUM as needed for handler, then restore SUM.

If don't want to use SUM and have page table, then can have replicated page table entries (one with supervisor access, one with user access). If don't want to use SUM and have S-mode PMPs without translation, then don't have same ability to prevent user from causing supervisor to touch that memory.

So, in case that have SUM, supervisor-mode interrupts need to save/restore SUM in handlers while interrupts are disabled.

MXR is only for systems with supervisor mode. Like SUM, MXR only affects M-mode if using MPRV and only affects page-based translation currently though might also impact S-mode PMP systems. Like SUM, supervisor-mode interrupts need to save/restore MXR in handlers while interrupts are disabled.