

Date: 2022/10/11

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :

[https://drive.google.com/file/d/1y\\_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view](https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view)

Current issues on github: <https://github.com/riscv/riscv-fast-interrupt/issues>

Previous meeting minutes: <https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes>

Fast Interrupt DoD (Definition of Done) Status: (new location)

<https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG>

### **Next meeting agenda (10/25/22)**

#274/pull 278 – inhv pseudo code?

#221/pull 270 – clicintie/ip summary regs.

#235 – xcause.x exceptions wording

### **Meeting minutes**

FYI, CLIC Summit presentation:

[RISC-V Summit 2022: Update on Fast Interrupt Task Group \(CLIC... \(sched.com\)](#)

Update on Fast Interrupt Task Group (CLIC Since Barcelona 2018 Wednesday, Dec 14, 2:20pm-2:40pm

CLIC status discussion – no AR review yet. need spec clean-up. all options are inline. hard to disentagle variants. what are sensible namings. some design work. figure out base and options. hope for Q1 for freeze.

#277 – CSIP – adding a note to clarify that all the interrupts on CLIC behave the same. Closed.

#279 – scratchsw/l csrrw access text clarification. Closed.

#275/pull #276. hwvector text clarification. Closed.

### **Github updates since last minutes:**

### **Specification updates since last minutes:**

### **Open issue status:**

**Issues that can be closed? (Simpler issues to discuss in red)**

**#221** – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270

#### **Need spec updates:**

**#49** – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

**#75** – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

**#158** – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

**#171** – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

**#160/200** - can rewrite to allow for but not assume n-extension is available. probably combine

#### **Need more discussion:**

**#96** – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

**#102** - preemptible interrupt handler code (for section 7.2)

**#205** – xnxti side-effect question. csrrsi rd, mnxti, uimm[4:0]. Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interrupt). Is this restriction necessary? Related to #100/#211?

**#226** – proposal to replace clicintattr.mode with xcliccfg.xlvl

**#235** – xcause.X updated on exceptions wording. help with more precise wording?

**#226** – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

**#247** – behavior when MPP is two-bits and hypervisor not implemented

**#248** – CLIC hypervisor mode (related to #92).

**#274** – xinhv sail pseudo code seems misleading

#### **Issues need to be worked:**

**#91** – DTS entry – have linux group review DTS example.

**#107** - heritage of features. keep researching and adding references to bibliography.

**#185** – SAIL model implementation of CLIC (probably waiver)

**#186** – CLIC architecture tests

**#187** – QEMU CLIC implementation update

**#242** – spike required if sail is waived?

**Issues waiting on ratification (encoding/opcode consistency review needed)**

**#88** – CSR address mapping

**Issues punted for rev1, keep open for future enhancements:**

**#92**/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

**#99** – horizontal interrupt window. punted for rev1

**#101** - xnxti to trigger on equal level. punted for rev1

**#106** – allow level change. Punted for rev1

**#108** – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

**#192** – allow mix of CLIC/CLINT at different priv modes punted for rev1