Date: 2021/07/20

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~7

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (08/03/21)

More open issue discussion?

Meeting minutes

Discussion of current state of Platform discovery TG and implications for CLIC – include file model. Chain the configs together in a way that one config directs to another config. IP providers need some way to put info into soc. give file or bitmap somewhere. since data is in memory map, there would have to be some definition of when it is available. Maybe put in rom accessible by core when core boots. It is a big requirement space because there are lots of different systems and use cases. Hard to come up with standard way. For some systems would have effect of optimizing for debugger instead of runtime software. But sometimes have applications of runtime software using discovery info. In general, unix crowd just wants device tree image.

Discussion of current state of Stateen CSR proposal and implications for CLIC. The purpose of Stateen is to try to avoid covert channels if an extension can contain lower priv. state e.g. supervisor, but hypervisor doesn't know about that state. CLIC won't have the problem because machine mode sets it up and priv mode on interrupt bits make it visible to lower modes. CLIC boots with only m-mode capability. Hypervisor shouldn't enable CLIC unless it knows lower modes can use it.

#161 – spec update clarifying that nxti only has write side effects. No functional change.

#158 – discussion of {clicintattr.mode,clicintctrl}. remove statement that says CLICINTCTLBITS is fixed? Add statement clicintctl can vary based on cliccfg changes? Still limit CLIC to up to 256 level + priority. How would this affect discovery. Discovery doesn't set parameters, just discovers what is possible. If the mode bits are shared but description is split, first set nmbits, read clicinfo.CLICINTCTLBITS, then set nlbits (can be set to different values based on nmbits.)

If implementation chooses to fix CLICINTCTLBITS, implies that # of bits of clicintattr.mode sent to priority encoder varies depending on cliccfg.nmbits.

Some have preference to instead make CLICINTCTLBITS is constant representing sum of implemented clicintattr.mode bits and clicintctrl bits. So priority encoder comparison is always the max of implemented bits and no additional logic is required to use 0, 1 or 2 bits of mode as cliccfg.nmbits changes. Programming access method doesn't change. cliccfg.nmbits set then write to WARL bits of clicintattr.mode[i], clicintctrl[i] . Prepare documentation pull and have additional discussion next meeting.

#107 – heritage of features. keep documenting prior art.

Discussion of #49 question about multiple harts. Added comment to issue that CLIC just specifies memory layout for a single hart. Punting on discovery details for now.

Github updates since last minutes:

#49 – prev spec had single control for multiple harts but current spec implies control per hart and implications.

#158 – additional detail on possible flexible nlbits/clicintctlbits implementation

#161 – spec clarification that only writes to nxti have side-effects

Specification updates since last minutes:

#161 – clarifying that nxti only has write side effects.

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129, #157?

#79 – supervisor/user mode alignment – closed with pull #129, #157?

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#107 – heritage of features. keep researching and adding references to bibliography.

#148 – Elaborate address map possibilities. Platform should be doing the layout.

#154 – inhv clarifications

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#102 - preemptible interrupt handler code (for section 7.2)

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Tried to update pull text to clarify when interrupt is set to 0.

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#158 – add option to reuse unused clicintattr.mode bits with clicintctrl to determine level value when 3 modes are supported but only 1 or 2 modes are selected by clicctrl.nmbits?

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?