Date: 2022/07/05

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 4

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (07/19/22)

Meeting minutes

Clarified xtvec.mode note in spec. Tried to be consistent with sepc[1] behavior when toggling misa.c. where stvec.mode/utvec.mode can be written, but always behave as 000011 when mtvec.mode is 000011. created issue #248 because further clarification is probably needed.

Closed #197, #214. continuing with #247 to track missing hypervisor case.

Closed #232 based on previously merged pull.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red)**

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

#202/pull #238 –writes/reads to clic mem mapped registers. (discuss if 64b store ordering is required. Pull is different from TG discussion)

#235 – xcause.X updated on exceptions wording.

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve usage of immediate bits (0-UIE?),2,4 in xnxti imm usage since those mstatus bits are WPRI. Related to #205/211

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal.

#239 – Dret should honor inhv

#240/pull #241 – change mscratchcsw to use mstatus.mpp in pseudocode? does it matter if not visible in non-clic mode? Need to update text to clarify.

#248 – xtvec.mode clarification. current text reuses field name mode as bits 5:0 vs 1:0. better to create a new field name.

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0).

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

#191 – reopened. question about sw vectoring.

#205 – xnxti side-effect question. `csrrsi rd, mnxti, uimm[4:0].` Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interupt). Is this restriction necessary? Related to #100/#211?

#219 – Interrupt ID ordering recommendations

#222 – legacy s-mode/u-mode timer interrupt setup

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#228 – dpc treatment - can breakpoints be set in hw vector table? (related to #230). Code-reduction TG chose to not allow setting breakpoints on hw vector table. https://github.com/riscv/riscv-code-size-reduction/issues/161

#229 – clicintattr.mode WARL behavior (moot if #226 accepted)

#230 – can hwvector table loads be interrupted by higher priv interrupts? Can table load be interrupted by debug mode? so dret should check xcause.xinhv to interpret dpc correctly? Related to issue #228.

#244 – debug behavior on hw vector fetch. related to #228?

#247 – behavior when MPP is two-bits and hypervisor not implemented

#248 – CLIC hypervisor mode (related to #92).

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1