Date: 2021/08/31

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~6

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (08/31/21)

More open issue discussion?

Meeting minutes

Pull #164 - Moved clicintattr.mode to 11 to reset section.

Discuss #109 arch string: something like Smclic – S: anything that is priv, m after S: affects m-mode.

Discuss #98 – CLIC name for now. closed. reopen if have better name

Discuss pull #167. will change pull to limit nlbits to 0 and 8, other values reserved. keep rest of text the same.

Discuss #50 – in hypervisor spec, got away from dynamic load/store. allow hypervisor to do things directly. so MPRV might be fading. most linux will support hypervisor. simpler system may have new loads/stores defined. For now have to save and restore those bits. maybe should be a comment in the priv spec on how to use MPRV. Bill will review and close if he agrees.

Discuss #165 – update xnxti pseudo-code to handle side-effects correctly. may eventually be replaced by SAIL code. related to #86. both closed with spec update. #165 reopened after meeting to further discuss wording.

Github updates since last minutes:

#165 – xnxti pseudo-code

Specification updates since last minutes:

#164 – moved clicintattr.mode reset state to reset section.

#86/#165 – updated xnxti pseudo-code for write side-effects

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches.

#48 – logic/state diagram for clicintip signals (related to #149?), add more clarification about hardware clearing of IP bits. only xnxti writes can clear IP bits.

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#107 – heritage of features. keep researching and adding references to bibliography.

#148 – Elaborate address map possibilities. Platform should be doing the layout.

#154 – inhv clarifications

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#102 - preemptible interrupt handler code (for section 7.2)

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG. Tried to update pull text to clarify when interrupt is set to 0.

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#158 – add option to reuse unused clicintattr.mode bits with clicintctrl to determine level value when 3 modes are supported but only 1 or 2 modes are selected by clicctrl.nmbits?

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?