Date: 2022/08/16

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

**Next meeting agenda (08/30/22)**

Discussed #202/pull #238. try to clean up pull #238. confusion about fields/registers. try to discuss next time.

**Meeting minutes**

SAIL status – changing the way config is being done. moving to risc-v config instead of by command line switches. take risc-v config file that describes implementation to configure model. run time config instead of build time config (like the run options were). currently some csrs are hard-wired but need to be set by run-time config. clic has some configurable attributes (e.g. num interrupts).

SAIL cookbook. 5-8 people contributing. reviewers about 10-12 people. all have other jobs.

SAIL language developed (alistar armstrong). comes out of ml language toolsuite. stacey concerns – ease of use of compiling and running risc-v model. configurability of it (memory maps, reset vectors) - arch compatibility tests running (spans sail model and toochain used by arch test group).

#251 – Discussed EABI proposal. no impact to fast-interrupt seen. example code in fast-interrupt spec might change to match EABI.

#202 – don't need to be too lax with 64 bit atomic updates? with amos.

#255 – make sure text says masked on use as well as read.

Clicintattr.mode WARL – when nmbits is 0, clicintattr.mode all values are legal.

Go thru spec and change basic mode to CLINT.

Discussing #219 – check with AIA if interrupt 12 location is being used. used for supervisor guest interrupt in AIA. 13 is counter overflow. 14/15 reserved for priv arch. will move csip to 14 for now. csip used for handling interrupts on this local hart. csip – background work that can be interrupted by anything else.

**Github updates since last minutes:**

**Specification updates since last minutes:**

**Open issue status:**

**Issues that can be closed? (**Simpler **issues to discuss in red)**

**#49** – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #231? Dependent on issue #96/226 discussion?

**#160/200** - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

**#202/pull #238** –writes/reads to clic mem mapped registers. (discuss if 64b store ordering is required. Pull is different from TG discussion)

**#235** – xcause.X updated on exceptions wording.

**Need spec updates:**

**#75** – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

**#158** – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

**#191** – Should add a note. if only doing hw vectoring only need execute. If doing sw vectoring need read.

**#221** – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal.

**#228** – dpc treatment - can breakpoints be set in hw vector table? (related to #230). Code-reduction TG chose to not allow setting breakpoints on hw vector table. https://github.com/riscv/riscv-code-size-reduction/issues/161, breakpoints check pc values. so may or may not just work depending on hw. sw loads just work how loads work. so sw vectoring should just be regular. same distinction as #191. if hw based can't set.

**#239** – Dret should honor inhv

**#240/pull #241** – change mscratchcsw to use mstatus.mpp in pseudocode? does it matter if not visible in non-clic mode? Need to update text to clarify.

**Need more discussion:**

**#96** – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

**#102** - preemptible interrupt handler code (for section 7.2)

**#171** – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

**#205** – xnxti side-effect question. `csrrsi rd, mnxti, uimm[4:0].` Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interupt). Is this restriction necessary? Related to #100/#211?

**#219** – Interrupt ID ordering recommendations

**#222** – legacy s-mode/u-mode timer interrupt setup

**#226** – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

**#229** – clicintattr.mode WARL behavior (moot if #226 accepted)

**#247** – behavior when MPP is two-bits and hypervisor not implemented

**#248** – CLIC hypervisor mode (related to #92).

#**251** – discuss EABI proposal

**#255** – CLIC/CLINT wording clarification

**Issues need to be worked:**

**#91** – DTS entry – have linux group review DTS example.

**#107** - heritage of features. keep researching and adding references to bibliography.

**#185** – SAIL model implementation of CLIC (probably waiver)

**#186** – CLIC architecture tests

**#187** – QEMU CLIC implementation update

**#242** – spike required if sail is waived?

**Issues waiting on ratification (encoding/opcode consistency review needed)**

**#88** – CSR address mapping

**Issues punted for rev1, keep open for future enhancements:**

**#92**/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

**#99** – horizontal interrupt window. punted for rev1

**#101 -** xnxti to trigger on equal level. punted for rev1

**#106 –** allow level change. Punted for rev1

**#108 –** pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

**#192 –** allow mix of CLIC/CLINT at different priv modes punted for rev1