Date: 2022/02/15

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (03/1/22)

More open issue discussion? Discuss if pulls resolve discussed issues.

Discuss issue #29/pull #190 – clicinttrig

Plan to discuss #96 – option was considered where the boundary between levels was a value instead of done by fixed number of bits.

Discuss #195/pull #196 – clarification of intthresh and xstatus.xie

Discuss #197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

Discuss #160/#200/pull #201 – user mode interrupts

Discuss #202/pull #203 – generalize statement about 32-bit writes to clic mem mapped registers.

Meeting minutes

Discussed SAIL status. Arch test – yaml configure sail model. to run test, need knowledge of base addr, etc. Arch-tech yaml but risc-v config. asm1.0. plan to have both supported. probably starting with yaml.

CLIC ratification phase – not really stable yet. issue #96 proposal is a big change. Could get stable soon. shoot for 2nd quarter? only 3 weeks until end of this quarter. balance between finished and better.

Discussing #195/pull #196 – make xintthresh WARL? implemented pull for WFI clarification.

WARL leaves large option space. software and testing space is larger. mandate that it is only as big as it needs to be. arch test would like to keep WARL as restrictive as possible. so software doesn't have to do discovery. try to write it to limit it to the number of threshold bits you have. make sure enough bits are implemented to represent useful levels of threshold.

Discussed #96 – Proposal: remove attr mode bits. replace with slvl, mlvl bits that determine which levels are in which mode.

Github updates since last minutes:

Specification updates since last minutes:

WFI clarification (related to confusion in issue #195).

Open issue status:

Issues that can be closed?

#29/#155 – clarify inttrig details. Created Pull #190. debug spec added tmexttrigger.intctl to support triggers from attached interrupt controllers. Will this provide the desired tightly integrated behavior? Need to mention behavior in clic spec, e.g., breakpoint before 1st instruction of interrupt executed?

#197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

#202/pull #203 – generalize statement about 32-bit writes to clic mem mapped registers

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve immediate bits in xnxti usage

#158 – change CLICCTRLBITS to CLICMLPBITS.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #183? Dependent on issue #96 discussion.

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more.

#97 – proposed reformat of xcause CSRs (bigger discussion). Think some assumptions might be wrong. to discuss with John Hauser.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0)..

#171 – CLICCFGLBITS parameter - related to #80, #158.

#195/pull #196 – clarification of intthresh and xstatus.xie

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1