Date: 2021/10/28 (moved temporarily to Thursday for this week)

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 4

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (11/09/21)

More open issue discussion?

Meeting minutes

SAIL model Statement of Work. Solidify spec more before requesting SAIL model support.

Discussed pull #176 for issue #154 – clarify inhv. inhv is about the actions of the handler. It is only visible when the handler itself experiences a trap. The inhv is there to allow the table read to be interrupted and resumed even though the table read itself is not an "instruction". Closed #154.

Discussed pull #144 – clarification of interrupt level = 0 in WFI section.

Discussion of WFI text. have to define when it can remain sleeping. cleaned up formatting of text. closed #31/#120.

Discussion of CLIC arch string. CLIC was put in non-ISA table in TG chairs meeting. but CLIC is a priv ISA with CSR changes. Will discuss with Mark.

Discussion of pull #174. Looks correct but now has merge conflicts with inhv section. need to fix and discuss next time.

Discussion of pull #173 – all priv modes in clic or all in clint. clarify table that table only applies when both modes are supported. only when clic is supported table/text might be different. for original … say only if clic is supported in table. Make it 8 bits so it is obvious only 6 bits are 0? [XLEN-1:6] say mtvec[5:0]. Also add register figure. XTVEC has address and has mode like in current priv spec.

Aiming for RV23M profile. Try to be ratified earlier because end of year gets busy.

Github updates since last minutes:

Issue #154 closed. (inhv clarification)

Issue #31/#120 closed. (WFI clarification)

Specification updates since last minutes:

pull #176 for issue #154. issue #154 closed.

pull #144 WFI section interrupt level = 0 clarification.

Open issue status:

Issues that can be closed?

Need spec updates:

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #173 tries to close.

#48 – logic/state diagram for clicintip signals (related to #149?), add more clarification about hardware clearing of IP bits. only xnxti writes can clear IP bits. Pull #174 tries to close. need to fix pull conflicts. Pull #174 now has conflicts with inhv update.

#75 – move hw vectoring to separate section in spec - waiting until other spec updated before making this large text change.

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too? Pull #175 tries to address until platform discovery solidifies.

#96 – proposed reformat of cliccfg. bit spec change, small hw change.

#107 – heritage of features. keep researching and adding references to bibliography.

#158 – change CLICCTRLBITS to CLICMLPBITS.

#160 - can rewrite to allow for but not assume n-extension is available.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.

#97 – proposed reformat of xcause CSRs

#102 - preemptible interrupt handler code (for section 7.2)

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#29/#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

#171 – CLICCFGLBITS parameter - related to #80.

Issues related to work in other TGs:

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#99 – horizontal interrupt window

#100 – reserve immediate bits

#101 - xnxti to trigger on equal level

#106 – allow level change

#108 – pushint/popint?