Date: 2022/09/27

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 6

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (10/11/22)

Meeting minutes

Implemented pull #264 – CLIC/CLINT mtvec text clarification. Closed #264, #255.

Implemented pull #268 – clarify implementation-defined for issue #267

Implemented #273 to fix xinhv references (issue #271)

Xinhv pseudo-code is misleading with what priv the pc mem_read occurs at. created issue #274.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed? (Simpler **issues to discuss in red****)**

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270

Need spec updates:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications.   Closed by #231? Dependent on issue #96/226 discussion?

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine

Need more discussion:

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #231 to go thru change implications. Separated xcliccfg.mlvl proposal to issue #226.

#102 - preemptible interrupt handler code (for section 7.2)

#205 – xnxti side-effect question. `csrrsi rd, mnxti, uimm[4:0]`. Pseudo-code shows uimm needs to be non-zero to cause side-effects (updating mintstatus, mcause.exccode/interupt). Is this restriction necessary? Related to #100/#211?

#226 – proposal to replace clicintattr.mode with xcliccfg.xlvl

#235 – xcause.X updated on exceptions wording. help with more precise wording?

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#247 – behavior when MPP is two-bits and hypervisor not implemented

#248 – CLIC hypervisor mode (related to #92).

#274 – xinhv sail pseudo code seems misleading

#275 – spec refers to hw vector table as aload

#277 - CSIP #12 to #16

Issues need to be worked:

#91 – DTS entry –   have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC (probably waiver)

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#242 – spike required if sail is waived?

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1