Date: 2022/03/01

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: 7

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (03/15/22)

More open issue discussion? Discuss if pulls resolve discussed issues.

Discuss issue #29/pull #190 – clicinttrig

Plan to discuss #96 – option was considered where the boundary between levels was a value instead of done by fixed number of bits.

Discuss #195/pull #196 – clarification of intthresh and xstatus.xie

Discuss #197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

Discuss #160/#200/pull #201 – user mode interrupts

Discuss #202/pull #203 – generalize statement about 32-bit writes to clic mem mapped registers.

Meeting minutes

Sail github status – working on WARL/config. Looking into interfacing interrupts with SAIL.

Discussed #96 – priv based on clicintctrl level value and xcliccfg.mlvl. problem – with current design, a possible implementation of the CLIC memory map would be to alias the same physical CLIC memory-mapped registers to different address ranges. so the registers are visible to s-mode, u-mode based on clicintattr.mode setting. when mode bits are taken away, the visibility of the register in different priv views is based on clicintctrl. but lower priv can modify clicintctl which could make the visibility of the interrupt change. clicintattr.mode makes this implementation easy.

How might CLIC memory-mapped visibility work using levels determine priv – could say s-mode limited to writing clicintctl to 1 level below m-level. means if m-mode lowers mlevel dynamically,lower priv interrupts could be changed to m-mode. then either have to clear bits

(like hw-vect) or setup interrupt handlers for all previous s-mode interrupts or have default hwvect interrupts.

Will look at proposed changes to spec and try think about any security holes/sw implications this may cause for next time.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

#29/#155 – clarify inttrig details. Created Pull #190. debug spec added tmexttrigger.intctl to support triggers from attached interrupt controllers. Will this provide the desired tightly integrated behavior? Need to mention behavior in clic spec, e.g., breakpoint before 1st instruction of interrupt executed?

#197/pull #198 – clarification of executing a lower-priv xRET on intstatus and inhv.

#160/200 - can rewrite to allow for but not assume n-extension is available. probably combine #160 with #200. closed by pull #201?

#202/pull #203 – generalize statement about 32-bit writes to clic mem mapped registers

Need spec updates:

#75 – move hw vectoring to separate section in spec - waiting until other issue spec updates before making this large text change.

#100 – reserve immediate bits in xnxti usage

#158 – change CLICCTRLBITS to CLICMLPBITS.

Need more discussion:

#49 – reopened: prev spec had single control for multiple harts but current spec implies control per hart and implications. Closed by #183? Dependent on issue #96 discussion.

#96 – proposed reformat of cliccfg. bit spec change, small hw change. Tried to close with Pull #183. more discussion about xcliccfg.nmbits. change to a programmable boundary value? discuss more. created a new pull #204 to go thru change implications.

#97 – proposed reformat of xcause CSRs (bigger discussion). Think some assumptions might be wrong. to discuss with John Hauser.

#102 - preemptible interrupt handler code (for section 7.2)

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts (possibly post-1.0)..

#171 – CLICCFGLBITS parameter - related to #80, #158.

#195/pull #196 – clarification of intthresh and xstatus.xie

#205 – xnxti side-effect question

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example.

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#92/Pull #181 – hypervisor compatibility. Pull #181 with Initial hypervisor extension proposal for CLIC. Punted for rev1.

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1