Date: 2022/06/21

Task Group: Fast Interrupts
Chair: Dan Smathers
Co-Chair: Kevin Chen
Number of Attendees: 4
Meetings Disclaimers
Video : https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view
Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues
Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes
Fast Interrupt DoD (Definition of Done) Status: (new location)
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Issues discussed:

#245 Inconsistency in mtvec CLIC mode

Clarified the encoding values at the xtvec for CLIC mode. Also clarified that only 000011 is CLIC mode, and 000010 is reserved.

#197 xret and intstatus.xil in section 8.5 return from handlers

Changed the pseudo-code to SAIL-like style. However, we noticed that there is no "default" case for the scenario where there is no match at all. In particular, the selection and behavior for Hypervisor mode is missing. So we created the following issue #248 to discuss the behavior of CLIC in Hypervisor mode.

#248 Hypervisor mode should be discussed.

Extension should either be incompatible with hypervisor extension, or behavior specified when hypervisor extension present.

#215 xscratchcsw pseudo-code clarification

Need to clarify operation when MPP allows for hypervisor mode.
Also, need to clarify operation when MPP is two-bits wide, hypervisor mode is not implemented, but something has set MPP to hypervisor mode. SAIL code is

incomplete with a missing case, and will cause SAIL run-time error if this occurs.

#213 Does CLICMTVECALIGN requirements align with AIA IMSIC and code size extension jump table?

Fixed CLIC parameter value ranges with pull request #216.

#220 Access to reserved address space

For reserved memory regions, we do not specify any specific trap behavior. Depending on system bus architecture, the system can ignore the access (e.g., read zero/write ignored) or cause a bus error (usually imprecise interrupt), or some other platform-specific behavior. The "reserved" annotation here implies that future standards might place additional standard registers in that space, and so using the space for non-standard features is inadvisable.