NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/07/18

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 7

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (08/1/23)

Issue #333/pull #341 – xcause.xinhv - should x be faulting priv or handling priv.

Issue #314/pull #342 – shv==0 requirement for xnxti. more discussion needed.

Issue #308/pull #325/pull #343– xnxti service loop – more discussion needed.

Issue #307/pull #331 – Parameter cleanup (compare with pull #297?)

Meeting minutes:

Krste couldn't join. Discussed ACT/SAIL.

Asked about status of PLIC sail progress. Allen said someone is working on tests for PLIC. Saravana created a first attempt at PLIC sail model. trying to compile but get syntax issues. Bills experience, very strong type checking pops up in unexpected places.

SAIL work. board of directors asked for info on ACT and SAIL work to be done. bill making list of extensions planning that are ratified or may be ratified. Remedial work to be done (something ratified but not done – hw performance monitors). when people with vested interest (e.g. vector crypto) then implementing and have pull requests. vector – sub-divided into 8 sub pull requests. 1,2, then vector crypto could make forward progress.

SAIL has a ci step that runs existing tests. working on solution to try regressions. for ci want to get both spike and sail cross-checking. runs against directed self-checking tests.

PLIC sail development lessons learned. changed 3 sections – c code, sail, ocaml as well. ocaml support might go away? no one seems to be using ocaml? sail – have to write an ocaml function to spit out data structures. when run a model, what inst does it support. hard to get today. go into sail, risc-v model. load/store implementation. for assembly language mapping. do we have a built-in functions that checks which bits are set, not set? saravana had to do bit-manipulation functions. would be nice to have binary manipulations. have shift-left/right. if have mismatch on type trying to add get compile error. So how to convert from 1 type to another. can't cast. intentionally can't do casting. if want to convert to other types, have to go thru the work of taking a bit-vector and expanding it into another bit vector. so makes code explicit.

Ocaml was helpful for original bring-up of sail. ocaml version may not be supported for much longer. on summit – hope there will be a talk on asciidoc taking in sail. presentation on vector sail? trials and tribulations on getting vector extension done. Working on pull request for 6 months.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

#307/pull #331 – NUM_INTERRUPT listed in two sections (text cleanup)

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

#308/pull #325 – xnxti service loop behavior

#314 – shv==0 requirement for xnxti

#333 – xcause.xinhv - should x be faulting priv or handling priv.

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – SPIKE model implementation of CLIC

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#**329 -** support for hw register save.