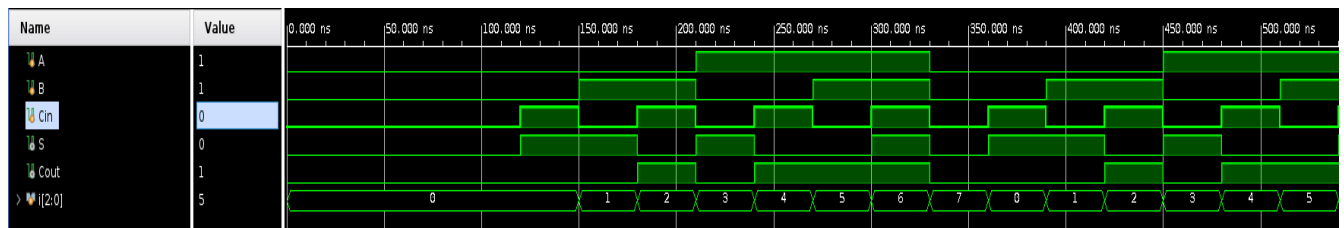


Lab 2 report  
ALU  
Hao Nguyen  
Arnaud Harmange

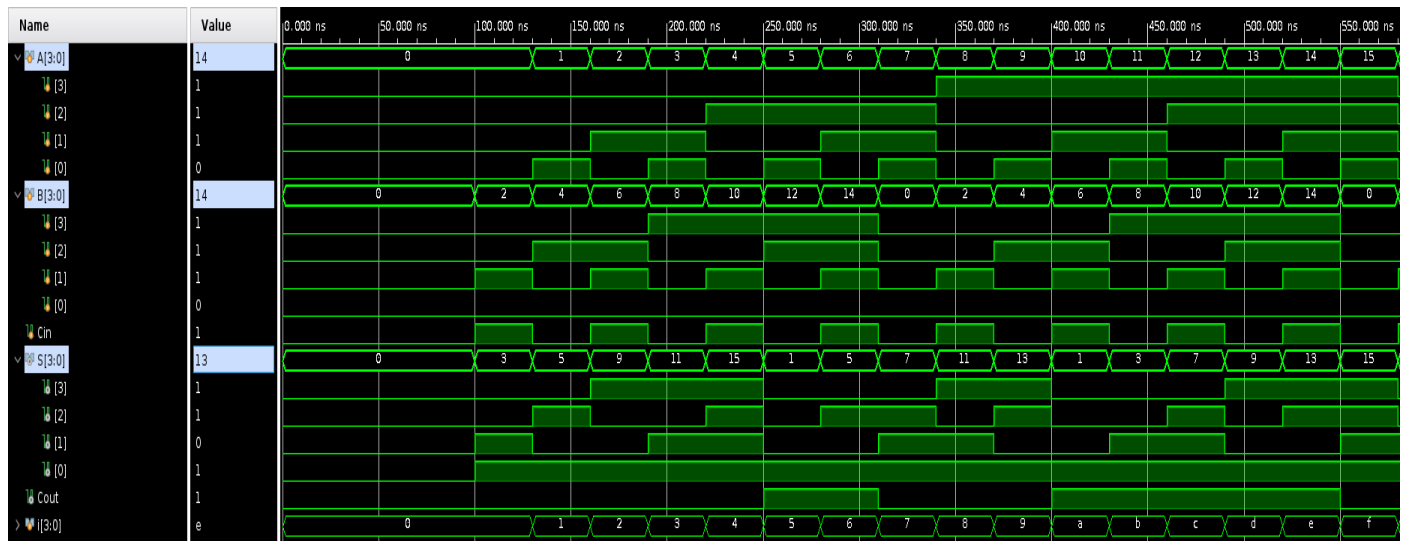
### Task 1: Full adder

Full adder using structural Verilog and basic gates to construct a 1 bit full adder. It has a 1 bit carry in and 2 1 bit inputs. Output S is 1 bit and a 1 bit carry-out.



### Task 2: Ripple carry adder

A ripple carry adder is simply 4 full adders connected together by the Carry out of the previous adder. The ripple carry adder has 2 4-bit inputs, 1-bit carry in and a 4-bit output and 1-0bit carry-out.



### Task 3: Carry-Select adder

Carry select adder consists of 3 4-bit ripple carry adder and 1 2-1 MUX. The first ripple carry adder calculates the addition of the least significant 4 bits and the carry out. The other 2 ripple carry adders calculate the sum of the most significant 4 bits. The mux pick which of the result

from the last 2 ripple carry adders to choose based on the carry-out from the first ripple carry adder



#### Task 4: ALU

The ALU consists of 12 switches and 3 buttons. The reset button resets all internal data and makes the seven segment display to display a 0. If button 0 and button 1 is pressed, the data from the switches is imputed and fed into the sub-ALU model.

ALU submodule:

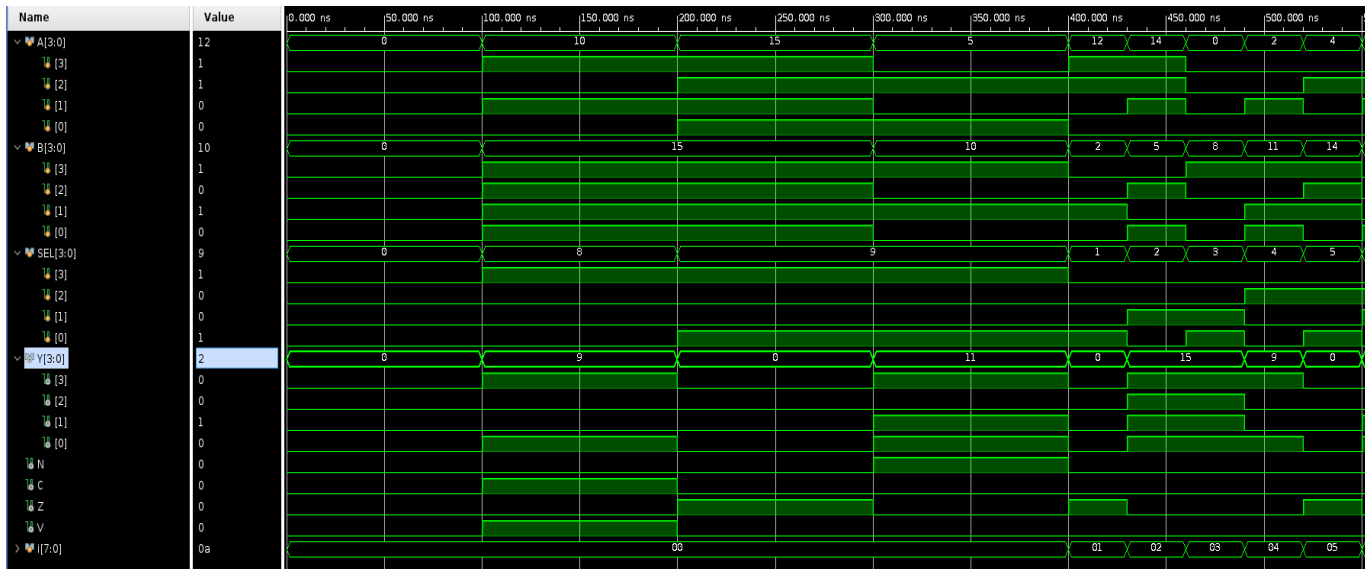
The ALU model is a 9-1 mux which will select the output based on the opcode. It also utilizes an internal 5 bit register *sum* to check for overflow and carry-out. Since A and B are both positive 4-bit numbers, an overflow and carry-out will cause the most significant bit of *sum* to be 1. Similar logic applied to subtraction. A leading bit of 1 in *sum* indicates a negative. The N flag will only be raised during subtraction operation and the C and V flag will only be raised during the addition operation.

The ALU will output the N,C,V,Z flag to the corresponding LEDs flag and the Y output will be fed to the seven segment display.

Seven segment display:

The resulting 4-bit binary will be converted into a hexadecimal display on the seven segment display. A decoder will convert the 4 bit input into corresponding hexadecimal cathode on the seven segment display.

ALU submodule simulation:



Top Module simulation:

