Agilent HCTL-2032, HCTL-2032-SC, HCTL-2022 Quadrature Decoder/Counter Interface ICs

Data Sheet

Description

The HCTL-20XX-XX is CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX-XX is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-20XX-XX consists of a quadrature decoder logic, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-20XX-XX contains 32-bit counter and provides LSTLL compatible tri-state output buffers. Operation is specified for a temperature range from –40 to +100°C at clock frequencies up to 33MHz.

The HCTL-2032 and HCTL-2032-SC have dual-axis capability and index channel support. Both devices can be programmed as 4x/2x/1x count mode. The HCTL-2032 and HCTL2032-SC also provides quadrature decoder output signals and cascade signals for use with many standard computer ICs.

The HCTL-2022 has most of the HCTL-2032 features, but it can only supports single axis and fixed at 4x count mode. The HCTL-2022 doesn't provide decoder output and cascade signals.

Features

- **Interfaces Encoder to Microprocessor**
- **33 MHz Clock Operation**
- **Programmable Count Modes (1x, 2x or 4x)**
- **Single or Dual Axis Support**
- **Index Channel Support**
- **High Noise Immunity:**
- **Schmitt Trigger Inputs and Digital Noise Filter**
- **32-Bit Binary Up/Down Counter**
- **Latched Outputs**
- **8-Bit Tristate Interface**
- **8, 16, 24, or 32-Bit Operating Modes**
- **Quadrature Decoder Output Signals, Up/Down and Count**
- **Cascade Output Signals, Up/Down and Count**
- **Substantially Reduced System Software**
- **5V Operation ($V_{DD} - V_{SS}$)**
- **TTL/CMOS Compatible I/O**
- **Operating Temperature: -40°C to 100°C**
- **32-Pin PDIP, 32-Pin SOIC, 20-Pin PDIP**

Applications

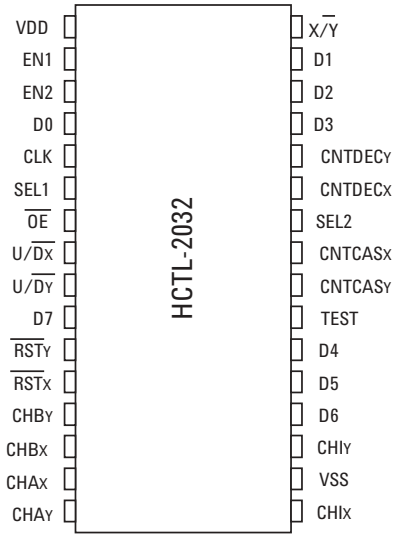
- **Interface Quadrature Incremental Encoders to Microprocessors**
- **Interface Digital Potentiometers to Digital Data Input Buses**

ESD WARNING: *Standard CMOS handling precautions should be observed with the HCTL-2032 family ICs.*

Devices

Part Number	Description	Package Drawing
HCTL-2032	32-bit counter, dual axis, decoder and cascade outputs, index channel support, programmable count modes, and 33 Mhz clock operation.	A
HCTL-2032-SC	All features of HCTL-2032.	B
HCTL-2022	Most of the HCTL-2032 features. The device supports single axis, and no decoder output and cascade signals. The programmable count mode is set to 4x internally.	C

PINOUT A



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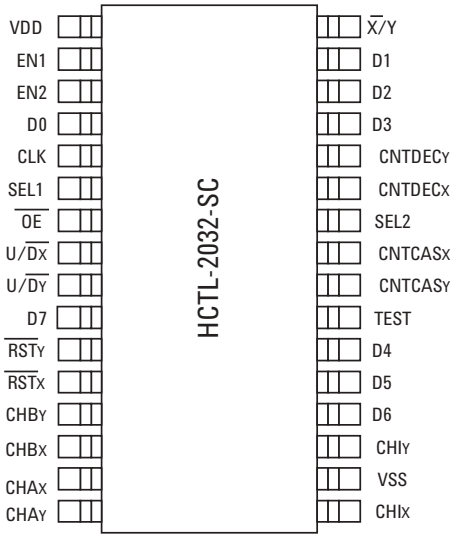

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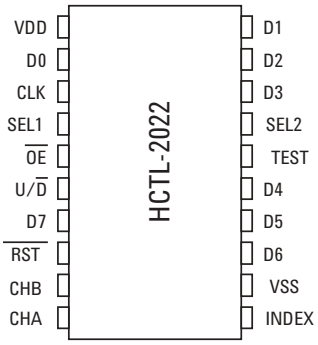
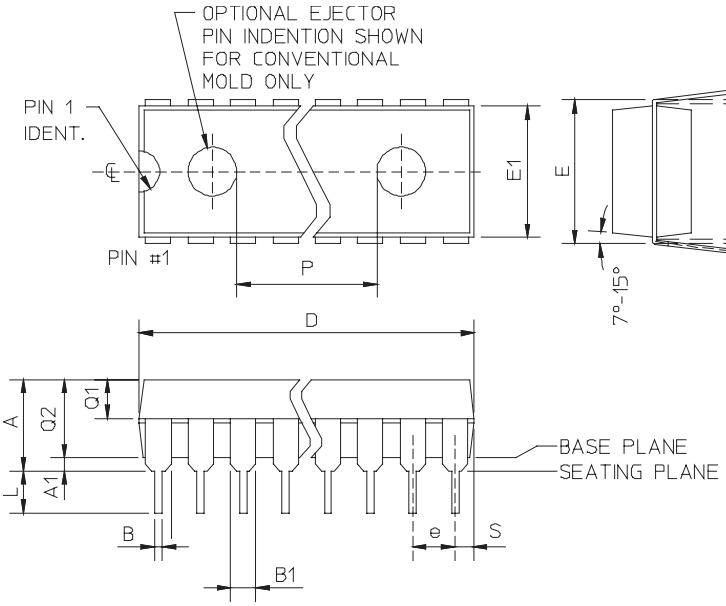


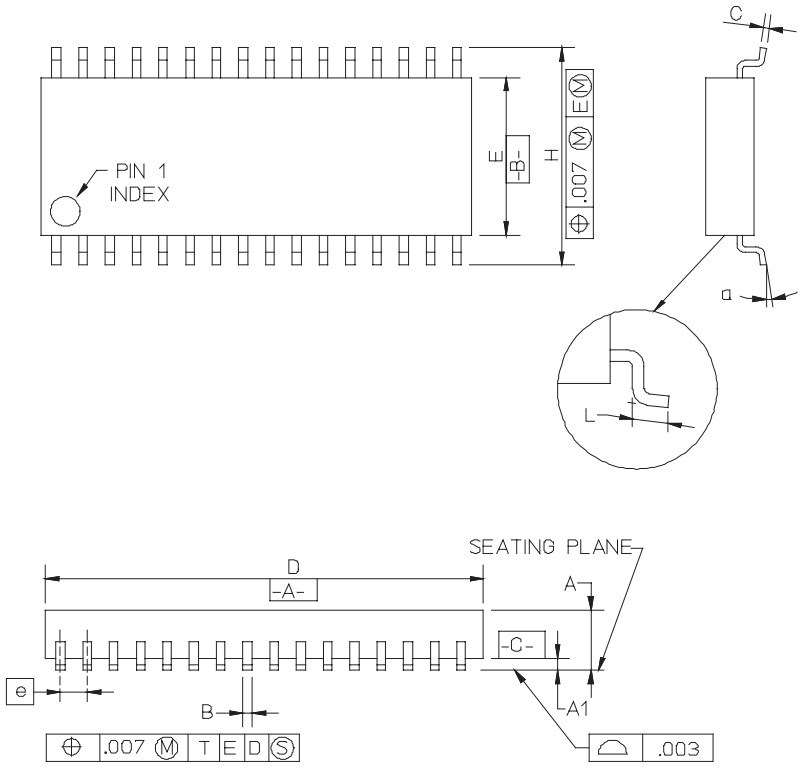
Package Dimensions (dimension in inches)

1) HCTL-2032



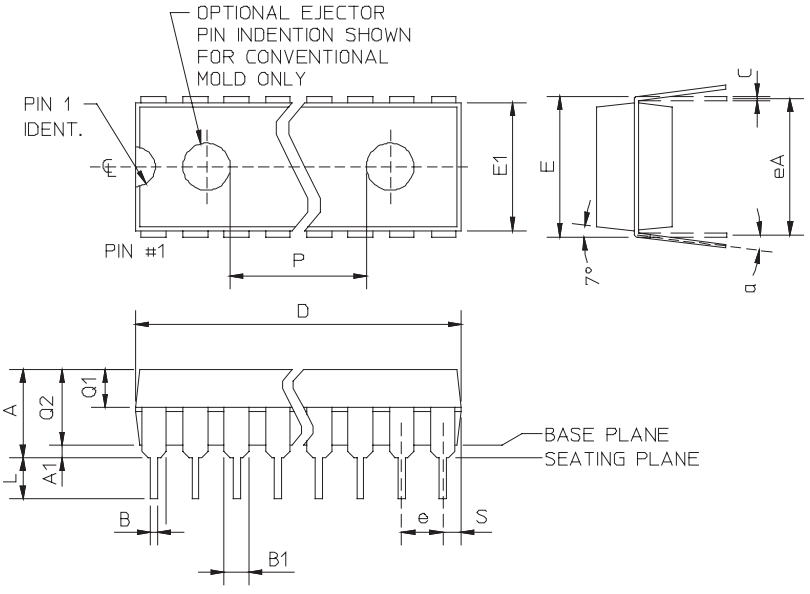
SYMBOL	MIN.	NOM.	MAX.
A	–	–	–
A1	–	–	–
B	.016	.018	.020
B1	.045	.050	.055
C	–	.010	–
D	1.640	1.650	1.660
E	.590	.610	.630
E1	.546	.550	.554
e	.100 TYP		
eA	–		
L	.100	–	–
α	–	–	–
Q1	.066	.070	.074
Q2	–	–	–
S	–	–	–

ii) HCTL-2032-SC



SYMBOL	MIN.	NOM.	MAX.
A	.090	.095	.100
A1	.004	.007	.010
B	.014	.016	.020
C	.006	.008	.0125
e	.050 BSC.		
D	.810	.818	.822
E	.292	.296	.299
L	.024	.032	.040
H	.405	.412	.419
α	0°	4°	8°

3) HCTL-2022



SYMBOL	MIN.	NOM.	MAX.
A	–	–	.170
A1	.015	–	–
B	.015	.018	.022
B1	.055	.060	.065
C	.008	.010	.012
D	1.015	1.020	1.025
E	.300	–	.325
E1	.250	.260	.270
e	.100 BSC.		
eA	.300 BSC.		
L	.125	–	.135
α	0°	–	15°
P	.710	–	–
Q1	.060	.065	.070
Q2	–	.130	–
S	.055	.060	.065

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_{IN}	-0.3 to (V_{DD} +0.3)	V
Storage Temperature	T_S	-55 to +150	°C
Operating Temperature [1]	T_A	-40 to +100	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	4.5 to 5.5	V
Ambient Temperature [1]	T_A	-40 to +100	°C

Table 3. DC Characteristics V_{DD} = 5V ± 5%; T_A = -40 to 100°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL} [2]	Low-Level Input Voltage				1.5	V
V_{IH} [2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN}=V_{SS} or V_{DD}	-10	1	+10	µA
V_{OH} [2]	High-Level Output Voltage	I_{OH} = -3.75 mA	2.4	4.5		V
V_{OL} [2]	Low-Level Output Voltage	I_{OL} = +3.75mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O=V_{SS} or V_{DD}	-10	1	+10	µA
I_{DD}	Quiescent Supply Current	V_{IN}=Vss or V_{DD}		1	10	µA
C_{IN} [3]	Input Capacitance	Any Input		5		pF
C_{OUT} [3]	Output Capacitance	Any Output		5		pF

Notes

1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5V to +5.5V), V_{IL} = 0.3V_{DD} and V_{IH} = 0.7V_{DD}; typical values are V_{OH} = V_{DD} − 0.5V and V_{OL} = V_{SS} + 0.2V
3. Including package capacitance

Functional Pin Description

Table 4. Functional Pin Descriptions.

Symbol	Pin		Description
	HCTL 2032/ 2032-SC	HCTL 2022	
V_{DD}	1	1	Power Supply
V_{SS}	18	12	Ground
CLK	5	3	CLK is a Schmitt-trigger input for the external clock signal.
CHA_X CHA_Y CHB_X CHB_Y	15 16 14 13	10 NC 9 NC	CHA_X, CHA_Y, CHB_X, and CHB_Y are Schmitt-trigger inputs that accept the outputs from a quadrature-encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required. CHA_X and CHB_X are the 1st axis and CHA_Y and CHB_Y are the 2nd axis.
CHI_X CHI_Y	17 19	11 NC	CHI_X and CHI_Y are Schmitt-trigger inputs that accept the outputs of Index channel from an incremental optical shaft encoder.
RSTNX RSTNY	12 11	8 NC	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. RST_X/ and RST_Y/ are asynchronous with respect to any other input signals. RST_X/ is to reset the 1st axis counter and RST_Y/ is to reset the 2nd axis counter.
OEN	7	5	This CMOS active low input enables the tri-state output buffers. The OE/, SEL1, and SEL2 inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL1 SEL2	6 26	4 17	These CMOS inputs directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in OE/ above, SEL_1 and SEL_2 also control the internal inhibit logic.

		BYTE SELECTED			
SEL1	SEL2	MSB	2ND	3RD	LSB
0	1	D4			
1	1		D3		
0	0			D2	
1	0				D1

EN1	EN2	Count Modes		
		4x	2x	1x
0	0	Illegal Mode		
1	0	On		
0	1		On	
1	1			On

EN1 EN2	2 3	NC NC	These CMOS control pins are set to high or low to activate the selected count mode before the decoding begins.
X/Y	32	NC	Select the 1st or 2nd axis data to be read. Low bit enables the 1st axis data, while high bit enables the 2nd axis data.
$CNTDEC_X$ $CNTDEC_Y$	27 28	NC NC	A pulse is presented on this LSTTL-compatible output when the quadrature decoder (4x/2x/1x) has detected a state transition. $CNTDEC_X$ is for 1st axis and $CNTDEC_Y$ is for 2nd axis.
U/Dx U/Dy	8 9	6 NC	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNTDEC and CNTCAS outputs. The proper signal U (high level) or D/ (low level) will be present before the rising edge of the CNTDEC and CNTCAS outputs.

$CNTCAS_X$ $CNTCAS_Y$	25 24	NC NC	A pulse is presented on this LSTTL-compatible output when the HCTL-2032 / 2032-SC internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
TEST	23	16	This pin is used for internal testing. Tied it to ground or leave it floating for normal operation.
D0	4	2	These LSTTL-compatible tri-state outputs form an 8-bit output ports through which the contents of the 32-bit position latch may be read in 4 sequential bytes. The MSB is read first followed by the rest of the bytes with the LSB is read last.
D1	31	20	
D2	30	19	
D3	29	18	
D4	22	15	
D5	21	14	
D6	20	13	
D7	10	7	

Switching Characteristics

Table 5. Switching Characteristics

Max/Min specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to +100 ^{0}C, C_L = 40 pf

Symbol	Description		Min.	Max.	Units
1	t_{CLK}	Clock Period		33	MHz
2	t_{CHH}	Pulse width, clock high	1/f		ns
3	t_{CD}	Delay time, rising edge of clock to valid, updated count information on D0-7		31	ns
4	t_{ODE}	Delay time, OEN fall to valid data		29	ns
5	t_{ODZ}	Delay time, OEN rise to Hi-Z state on D0-7		29	ns
6	t_{SDV}	Delay time, SEL0~SEL1 valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		29	ns
7	t_{XNYDV}	Delay time, XNY valid to stable, selected data byte.		29	ns
8	t_{CLH}	Pulse width, clock low	15		ns
9	t_{SS}	Setup time, SEL1~SEL2 before clock fall	12		ns
10	t_{OS}	Setup time, OEN before clock fall	12		ns
11	t_{XNYS}	Setup time, XNY before clock fall	12		ns
12	t_{SH}	Hold time, SEL1~SEL2 after clock fall	0		ns
13	t_{OH}	Hold time, OEN after clock fall	0		ns
14	t_{XNYH}	Hold time, XNY after clock fall	0		ns
15	t_{RST}	Pulse width, RSTNX~RSTNY low	10		ns
16	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	2		ns
17	t_{DSD}	Hold time, last data byte stable after next SEL state change	2		ns
18	t_{DOD}	Hold time, data byte stable after OEN rise	2		ns
19	t_{DXNYD}	Hold time, data byte stable after XNY change	2		ns
20	t_{UDDX}	Delay time, U/DNX valid after clock rise	4	29	ns
21	t_{UDDY}	Delay time, U/DNY valid after clock rise	4	29	ns
22	t_{CHXD}	Delay time, CNTDECX or CNTCASX high after clock rise	4	31	ns
23	t_{CHYD}	Delay time, CNTDECY or CNTCASY high after clock rise	4	31	ns
24	t_{CLXD}	Delay time, CNTDECX or CNTCASX low after clock fall	4	31	ns
25	t_{CLYD}	Delay time, CNTDECY or CNTCASY low after clock fall	4	31	ns
26	t_{UDXH}	Hold time, U/DNX stable after clock rise	2		ns
27	t_{UDYH}	Hold time, U/DNY stable after clock rise	2		ns
28	t_{UDCXS}	Setup time, U/DNX valid before CNTDECX or CNTCASX rise	Note 1		ns
29	t_{UDCYS}	Setup time, U/DNY valid before CNTDECY or CNTCASY rise	Note 1		ns
30	t_{UDCXH}	Hold time, U/DNX stable after CNTDECX or CNTCASX rise	Note 2		ns
31	t_{UDCYH}	Hold time, U/DNY stable after CNTDECY or CNTCASY: rise	Note 2		ns

Notes

1. tclk – max delay (item 20/21) + min delay (item 22/23)
2. tclk – max delay (item 22/23) + min delay (item 20/21)

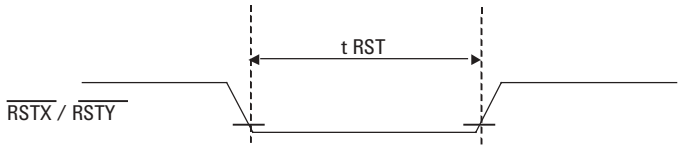


Figure 1. Reset Waveform

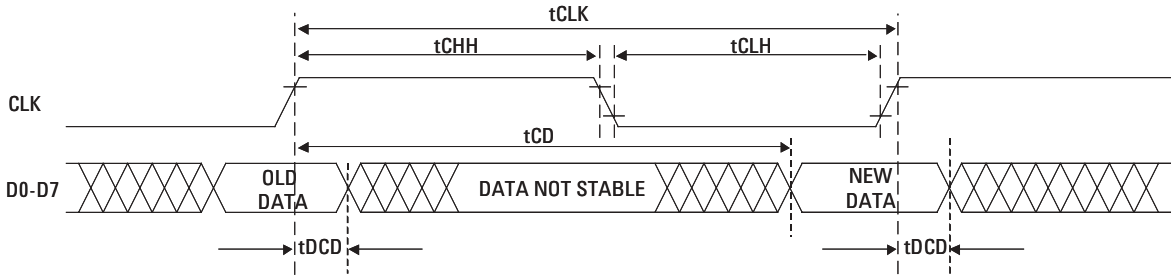


Figure 2: Waveforms for Positive Clock Edge Related Delays

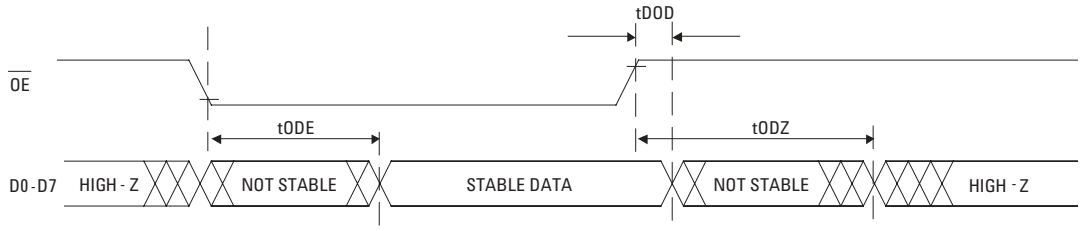


Figure 3: Tri-State Output Timing

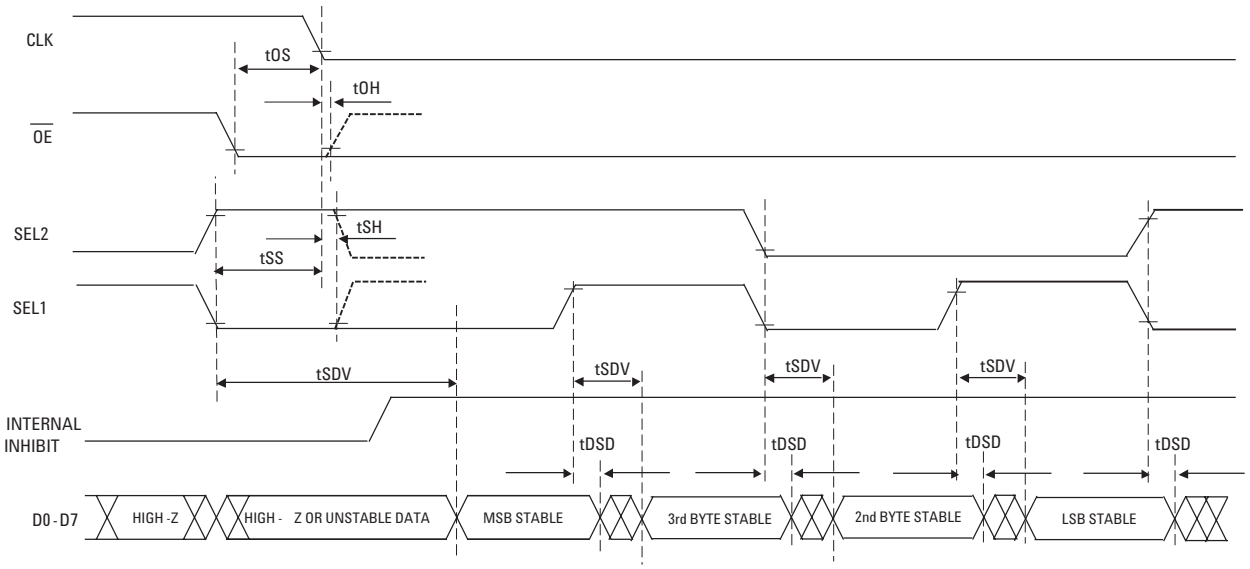


Figure 4: Bus Control Timing

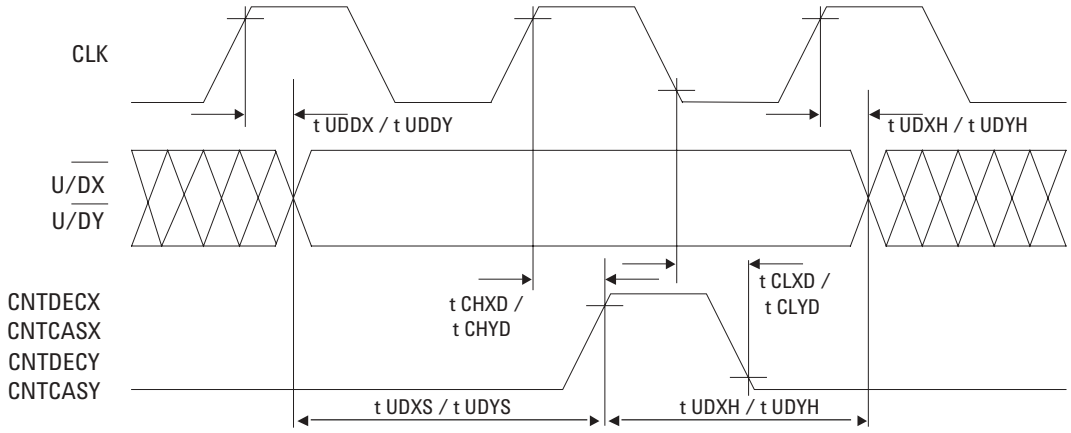


Figure 5: Decoder, Cascade Output Timing

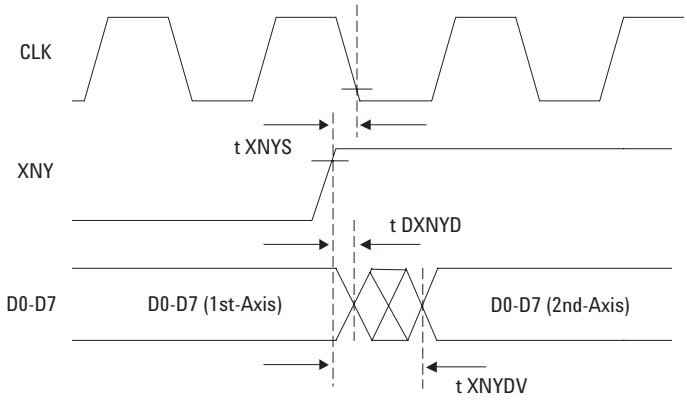


Figure 6: Output Data from 1st-axis and 2nd-axis

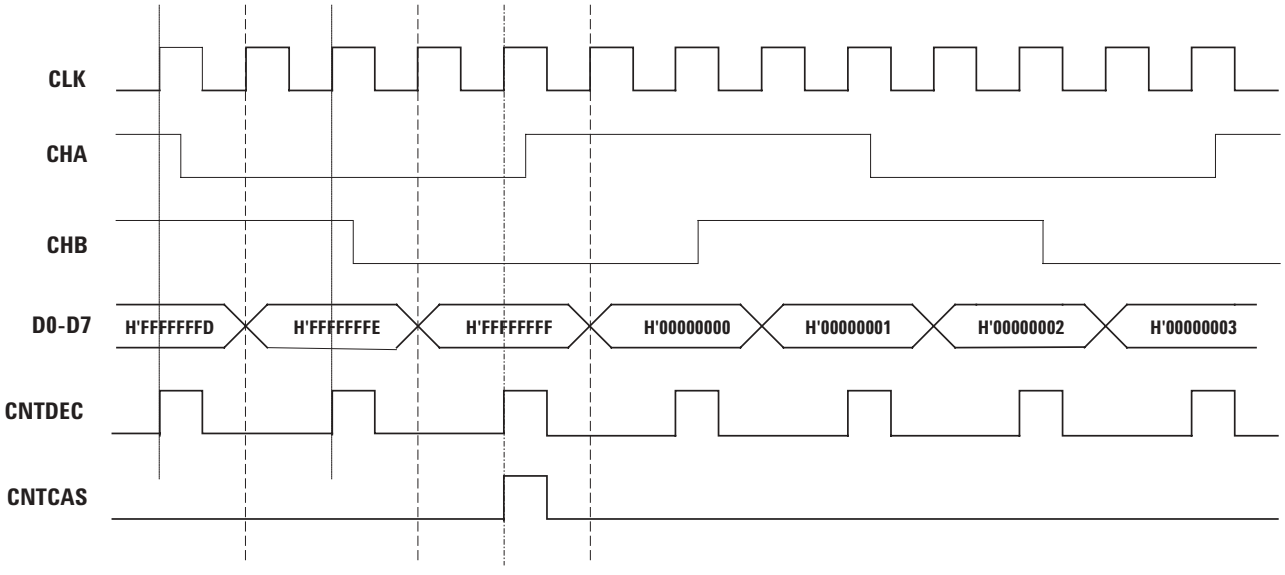


Figure 7: Quadrature decoder for 1st-axis / 2nd-axis (4x count mode)

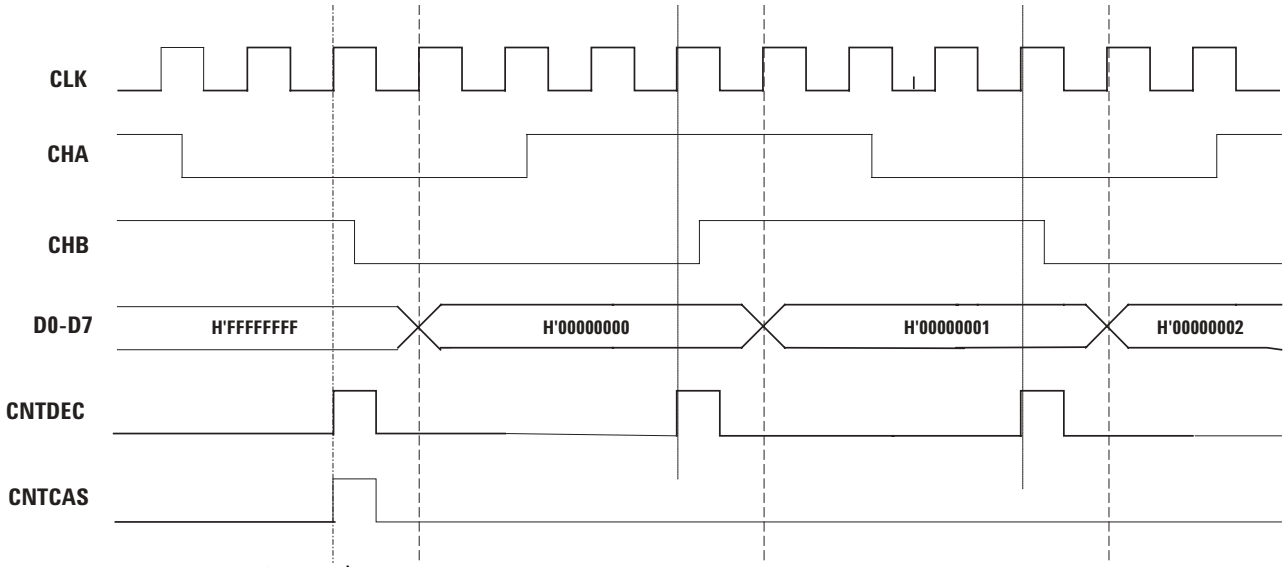


Figure 8: Quadrature decoder for 1st-axis / 2nd-axis (2x count mode)

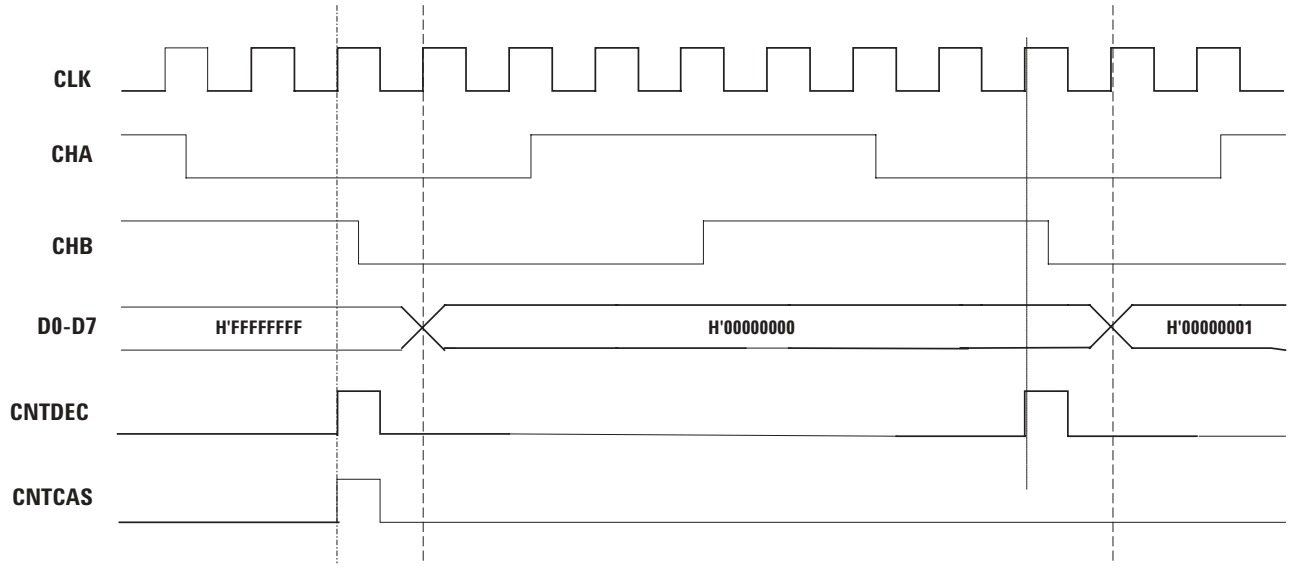


Figure 9: Quadrature decoder for 1st-axis / 2nd-axis (1x count mode)

Operation

A block diagram of the HCTL-20XX-XX family is shown in Figure 10. The operation of each major function is described in the following sections.

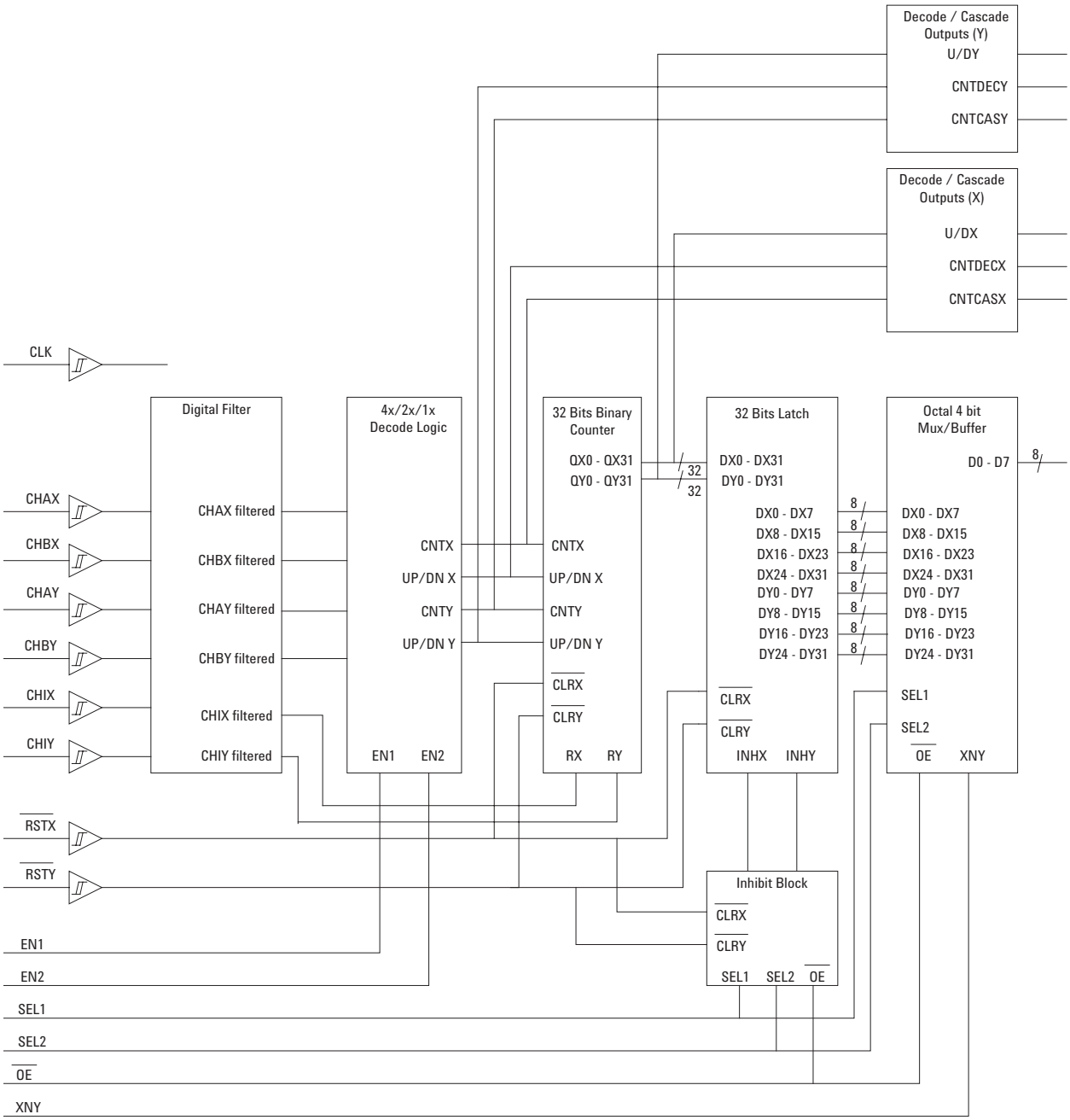


Figure 10. Simplified Logic Diagram

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 11 shows the simplified schematic of the input section. The signals are first passed through a Schmitt-trigger buffer to address the problem of input signals with slow rise times and low-level noise (approximately < 1V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges.

Refer to Figure 12, which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

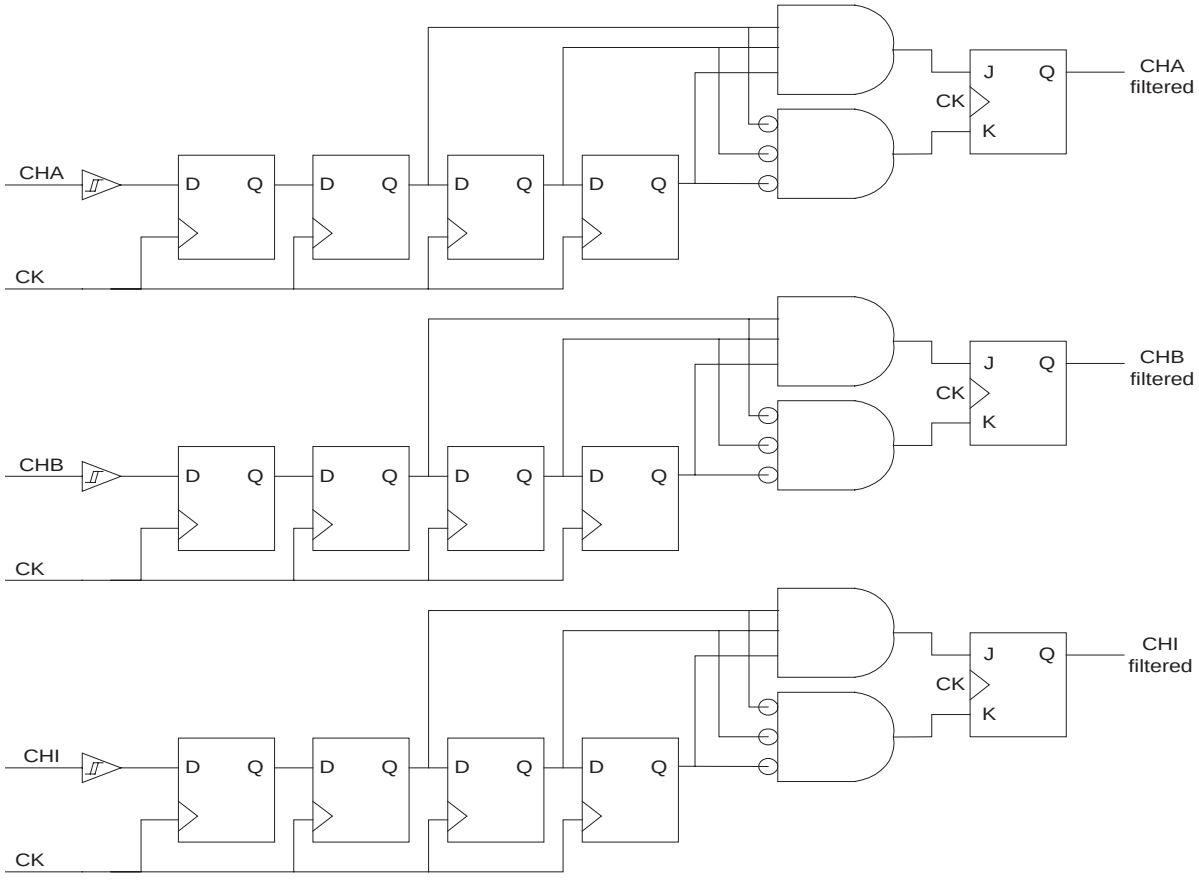


Figure 11. Simplified Digital Noise Filter Logic

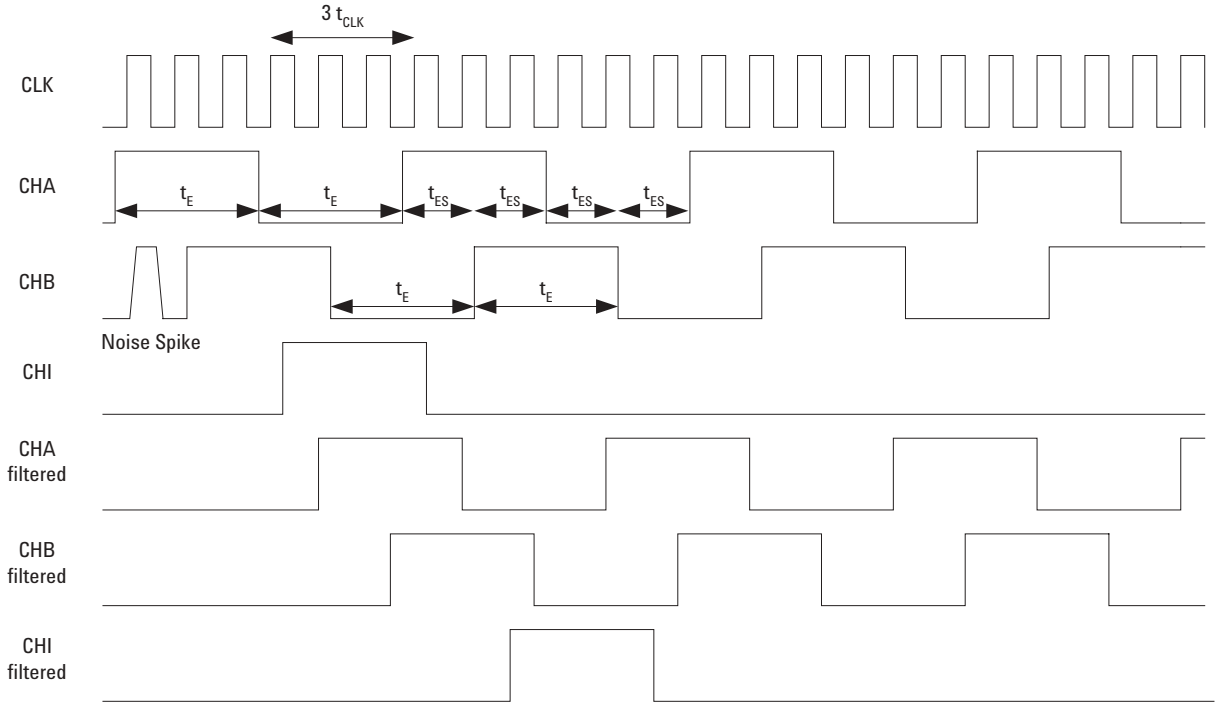


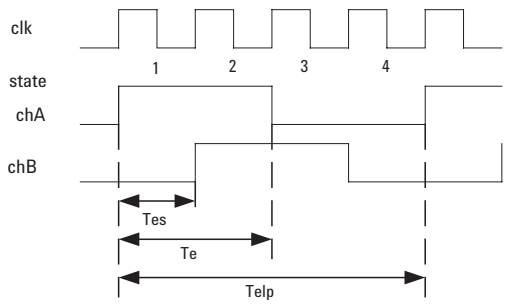
Figure 12. Signal Propagation through Digital Noise Filter

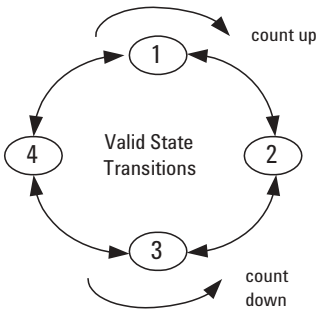
Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of one, two or four (1X, 2X, 4X decoding) depending on the resolution mode. When using an encoder for motion sensing, the user benefits from the selectable resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the integral position counter.

Figure 13 shows the quadrature states of Channel A and Channel B signals. The 4x decoder mode will output a count signal for every state transition (count up and count down). Figure 14 shows the valid state transitions for 2x and 1x decoder modes. The 2x/1x decoder will output a count signal at respective state transition, depending on the counting direction. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.





CHA	CHB	STATE	4X Decoder (Count Up & Count Down)
1	0	1	Pulse
1	1	2	Pulse
0	1	3	Pulse
0	0	4	Pulse

Figure 13. 4x Decoder Mode

CHA	CHB	STATE	2x Count Up	2x Count Down	1x Count Up	1x Count Down
1	0	1	Pulse	-	Pulse	-
1	1	2	-	Pulse	-	Pulse
0	1	3	Pulse	-	-	-
0	0	4	-	Pulse	-	-

Figure 14. 2x and 1x Decoder Modes

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 12 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high) has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take into account finite rise time of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much greater than $3t_{CLK}$ to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 13, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that t_{ES} > t_{CLK}.

Position Counter

This section consists of a 32-bit (HCTL-20XX-XX) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 32 bits of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is 32 bits, so the count represents "absolute" position.

B. The system is cyclic with 32 bits of count per cycle. RST/ is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is >8, 16, 24, or 32 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability. Two's-complement arithmetic is normally used to compute position from these periodic position updates.

D. The system count is >32 bits so the HCTL-2032 / 2032-SC can be cascaded with other standard counter ICs to give absolute position.

Position Data Latch

The position data latch is a 32-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during four-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically re-enabled at the end of these reads. The latch is cleared to 0 asynchronously by the RST signal.

Inhibit Logic

The Inhibit Logic Section samples the OE, SEL1 and SEL2 signals on the falling edge of the clock and, in response to certain conditions (see Figure 15), inhibits the position data latch. The RST signal asynchronously clears the inhibit logic, enabling the latch.

Bus Interface

The bus interface section consists of a 32 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL1, SEL2 and OE signals determine which byte is output and whether or not the output bus is in the high-Z state. In the HCTL-20XX-XX, the data latch is 32 bit wide.

Quadrature Decoder Output (HCTL-2032 / 2032-SC only)

The quadrature decoder output section consists of count and up/down outputs derived from the 4x/2x/1x decoder mode of the HCTL-2032 / 2032-SC. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic.

Cascade Output (HCTL-2032 / 2032-SC only)

The cascade output also consists of count and up/down outputs. When the HCTL-2032 / 2032-SC internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic.

Step	SEL1	SEL2	OE	CLK	Inhibit Signal	Action
1	L	H	L		1	Set inhibit; Read MSB
2	H	H	L		1	Read 2nd Byte
3	L	L	L		1	Read 3rd Byte
4	H	L	L		1	Read LSB
5	X	X	H		0	Completes inhibit logic reset

Figure 15. Four Bytes Read Sequence

Cascade Considerations (HCTL-2032 / 2032-SC only)

The HCTL-2032 / 2032-SC 's cascading system allows for position reads of more than four bytes. These reads can be accomplished by latching all the bytes and then reading the bytes sequentially over the 8-bit bus. It is assumed here that, externally, a counter followed by a latch is used to count any count that exceeds 32 bits. This configuration is compatible with the HCTL-2032 / 2032-SC internal counter/latch combination.

Consider the sequence of events for a read cycle that starts as the HCTL-2032 / 2032-SC 's internal counter rolls over. On the rising clock edge, count data is updated in the internal counter, rolling it over. A count-cascade pulse (CNT_{CAS}) will be generated with some delay after the rising clock edge (t_{CHD}). There will be additional propagation delays through the external counters and registers. Meanwhile, with SEL and OE low to start the read, the internal latches are inhibited at the falling edge and do not update again till the inhibit is reset.

If the CNT_{CAS} pulse now toggles the external counter and this count gets latched a major count error will occur. The count error is because the external latches get updated when the internal latch is inhibited.

Valid data can be ensured by latching the external counter data when the high byte read is started (SEL and OE low). This latched external byte corresponds to the count in the inhibited internal latch. The cascade pulse that occurs during the clock cycle when the read begins gets counted by the external counter and is not lost.

For example, suppose the HCTL-2032 / 2032-SC count is at FFFFFFFFh and an external counter is at F0h, with the count going up. A count occurring in the HCTL-2032 / 2032-SC will cause the counter to roll over and a cascade pulse will be generated. A read starting on this clock cycle will show FFFFFFFFh from the HCTL-2032 / 2032-SC. The external latch should read F0h, but if the host latches the count after the cascade signal propagates through, the external latch will read F1h.

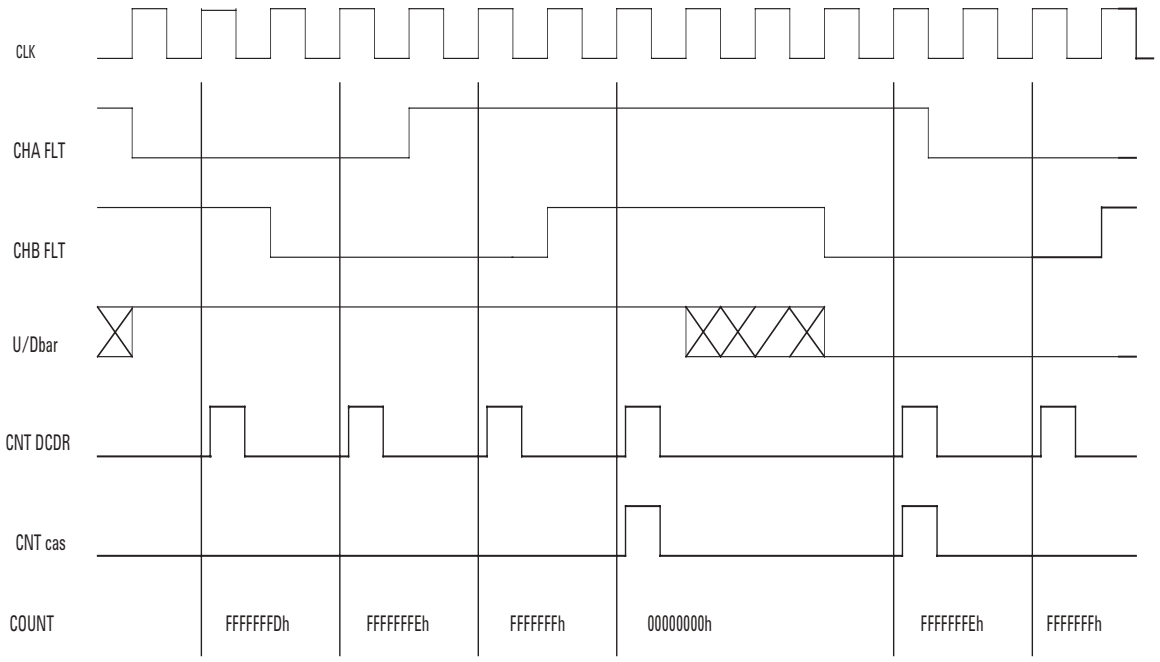


Figure 16. Decode and Cascade Output Diagram (4x)

Interfacing the HCTL-2032 to an Atmel AVR 90S8535

The circuit shown in Figure 17 shows the connections between an HCTL-2032 and an Atmel AVR controller. Data lines D0-D7 are connected to the Atmel AVR bus port. The 8 MHz oscillators clock the Atmel AVR, whereas the external 33 MHz oscillators clock the HCTL-2032. Figure 18 illustrates the program that interfaces with an Atmel AVR 90S8535.

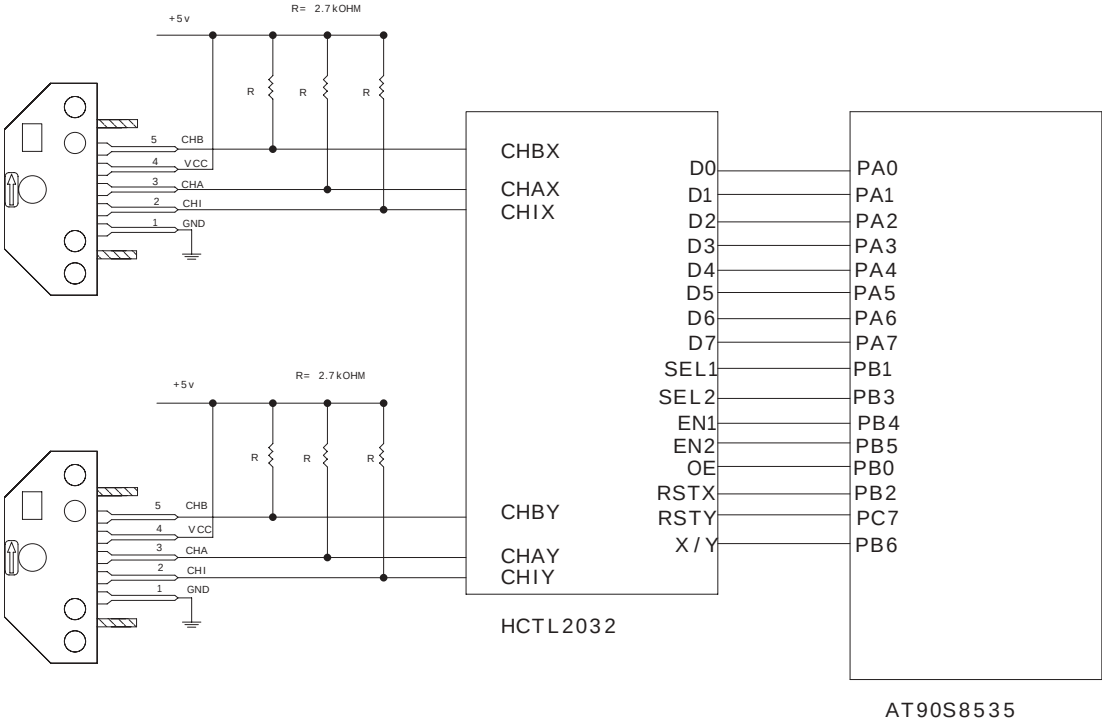


Figure 17. An HCTL-2032-to-Atmel AVR Interface

```
Set Portb.4                         'EN1=1
Reset Portb.5                        'EN2=0
Reset Portb.6                          'Select X-axis

Result_new = 0
Result_old_x = 0
Result_old_y = 0

Do

  Set Portb.0                       'Disable OE
  Waitms 25

  Reset Portb.1                      'SEL1=0 (MSB)
  Set Portb.3                       'SEL2=1 (MSB)
  Reset Portb.0                      'Enable OE

  Gosub Get_hi                      'Get MSB

  Set Portb.1                       'SEL1=1 (2nd Byte)
  Set Portb.3                       'SEL2=1 (2nd Byte)

  Gosub Get_2nd                      'Get 2nd Byte

  Reset Portb.1                      'SEL1=0 (3rd Byte)
  Reset Portb.3                      'SEL2=0 (3rd Byte)

  Gosub Get_3rd                      'Get 3rd Byte

  Set Portb.1                       'SEL1=1 (LSB)
  Reset Portb.3                      'SEL2=0 (LSB)

  Gosub Get_lo                      'Get LSB

  Set Portb.0                       'Disable OE
  Waitms 25

  Mult = 1
  Temp = Result_lo * Mult                 'Assign LSB
  Result = Temp
  Mult = Mult * 256
  Temp = Result_3rd * Mult                 'Assign 3rd Byte
  Result = Result + Temp
  Mult = Mult * 256
  Temp = Result_2nd * Mult                 'Assign 2nd Byte
  Result = Result + Temp
  Mult = Mult * 256
  Temp = Result_hi * Mult                 'Assign MSB
  Result = Result + Temp
'
'Result = 32-bits Count Data
'
                              .
                              .
Loop

Get_hi:
  Hi_old = Pina                     'Get Current Data
  Hi_new = Pina                     'Get 2nd Data
  If Hi_new = Hi_old Then
                Result_hi = Hi_new              'Get Stable Data
                Return
  Else
                Goto Get_hi
  End If
```

Figure 18. Typical Program for Reading HCTL-2032 with Atmel AVR

```
Get_2nd:
  2nd_old = Pina                        'Get current data
  2nd_new = Pina                        'Get 2nd Data
  If 2nd_new = 2nd_old Then
                Result_2nd = 2nd_new            'Get stable data
                Return
  Else
                Goto Get_2nd
  End If

Get_3rd:
  3rd_old = Pina                        'Get current data
  3rd_new = Pina                        'Get 2nd Data
  If 3rd_new = 3rd_old Then
                Result_3rd = 3rd_new            'Get stable data
                Return
  Else
                Goto Get_3rd
  End If

Get_lo:
  Lo_old = Pina                         'Get current data
  Lo_new = Pina                         'Get 2nd Data
  If Lo_new = Lo_old Then
                Result_lo = Lo_new              'Get stable data
                Return
  Else
                Goto Get_lo
  End If
```

Figure 18 Cont. Typical Program for Reading HCTL-2032 with Atmel AVR

ACTIONS

1. At first, Port B4, B5, and B6 are setup for 4X encoding and X/Y axis selection.
2. The HCTL-2032 detects that OE/ are low on the next falling edge of the CLK and asserts the internal inhibit signal. Data can be read without regard for the phase of the CLK.
3. SEL1 and SEL2 are setup to select the appropriate bytes. The "Get_hi" subroutine is called and the data is read into the AVR.
4. Step 3 is repeated by changing the SEL1 and SEL2 combinations and specific subroutine is called to read in the appropriate data.
5. The HCTL-2032 detects OE/ high on the next falling edge of the CLK. The program set OE/ high by writing the correct value to the respective Port. This causes the data lines to be tristated. On the next rising CLK edge new data is transferred from the counter to the position data latch.
6. For displaying purposes, the data is arranged in 32-bit data by shifting the MSB to the left through multiplication.

Ordering Information

HCTL - 20 XX - XX

32	Blank	32-PDIP Package
32	SC	32-SOIC Package
22	Blank	20-PDIP Package

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Data subject to change.

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