**Laboratory 5-6:**
**Sequential Circuits**
***EE 203 Digital Systems Design***

**Date Performed:** December 6-December 13, 2023

**Teaching Assistant:** Ayşenaz Ezgi Ergin

**names Teaching Assistant:** Bora Kayaoglu

**Instructor:** Dr.Mustafa Tanış

**Institution:** MEF University

**Filiz Köse** 042301071

**Kerim Ercan** 042401167

# 1.Introduction:

The skills required to develop reliable and efficient digital systems.

In the fifth session of the EE203 Digital Systems Design Laboratory, the basic concepts of sequential logic circuits are explored, with a focus on their design, implementation, and analysis. Sequential circuits, which store and process information over time, are crucial to digital systems because they include memory and feedback mechanisms. This curriculum aimed to improve understanding of these circuits through practical exercises such as developing T-flip-flops with D-latches, constructing parity generators, and putting state machines into practice. The lab tasks included building and testing circuits to make sure they operated as the theory expected. Among the techniques used to examine how flip-flops and sequential circuits operated were truth tables, Karnaugh maps, and state diagrams. Understanding the differences between Moore and Mealy state machines and reducing circuit components for optimal performance were given a lot of attention. Students gained hands-on experience in creating and troubleshooting digital systems by applying classroom concepts to actual scenarios.The introduction of technology like breadboards, LEDs, and Logisim software allowed for precise observations and validation of circuit performance. This lab activity not only reinforced theoretical knowledge but also fostered the critical thinking and problem-solving skills required to build reliable and efficient digital systems.

## 2.Theory:

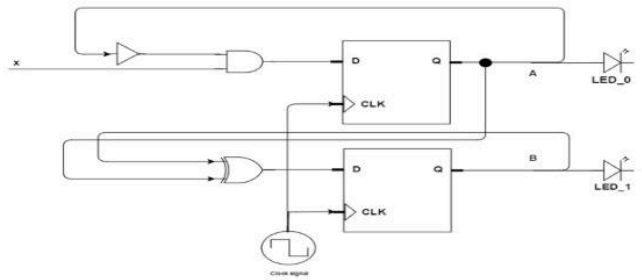
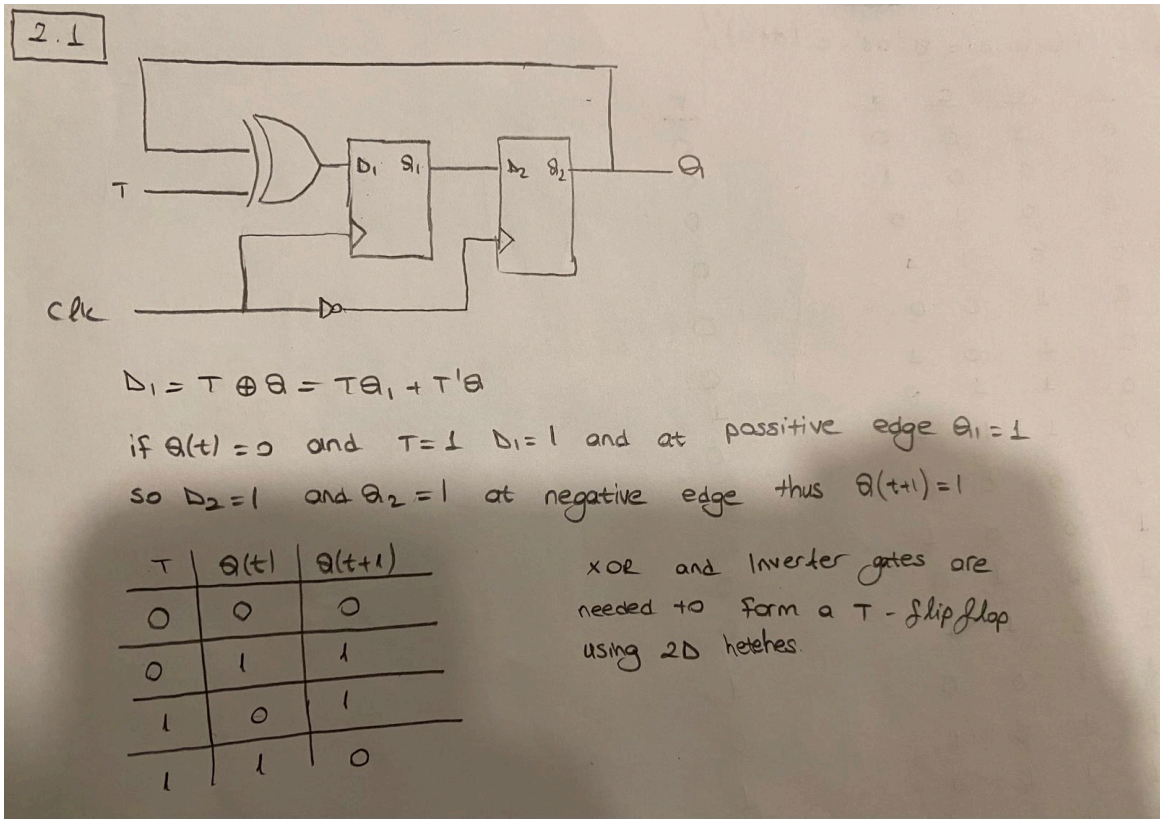


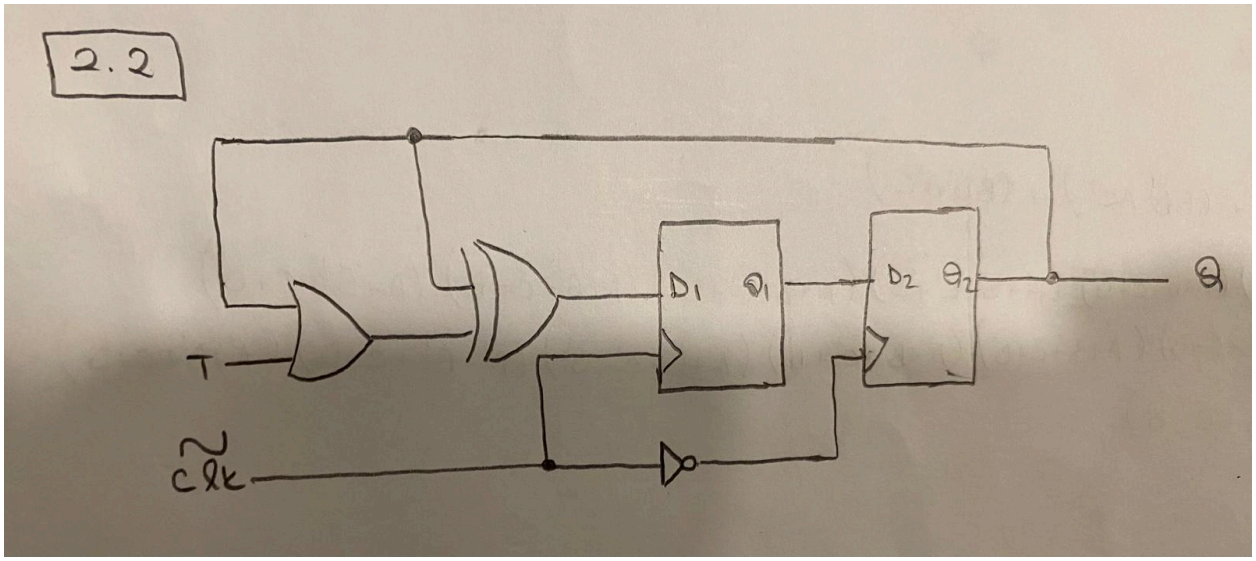

Figure 1: A sequential logic circuit diagram.

phase of the experiment consists of constructing the given sequential circuit using two JK-flipflops. The rest of the questions explore the second phase of the experiment.

## 2.1:

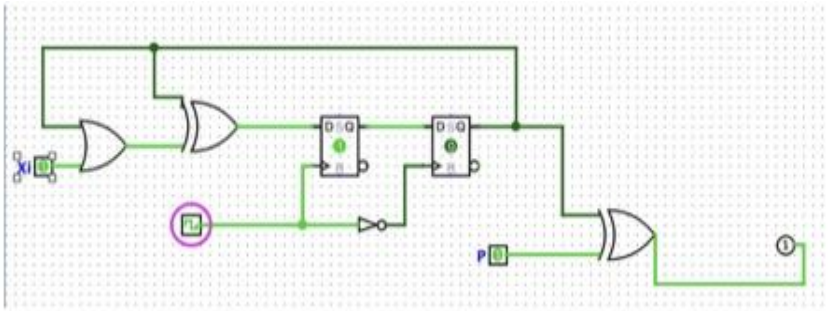


## 2.2:




## 2.3:

A parity generator can be adapted to function as a parity checker with slight adjustments. The concept involves comparing the generated parity (calculated parity) with the given parity (expected parity bit). Any discrepancy between the two signals a parity error.

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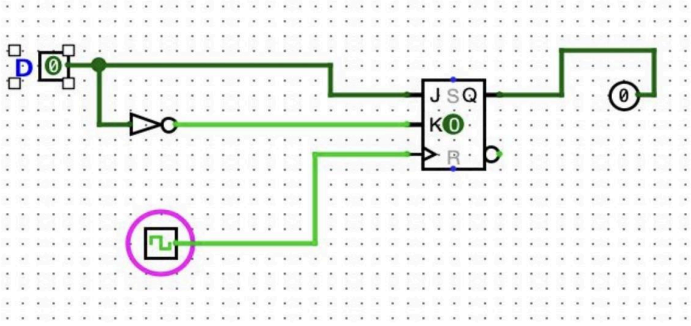


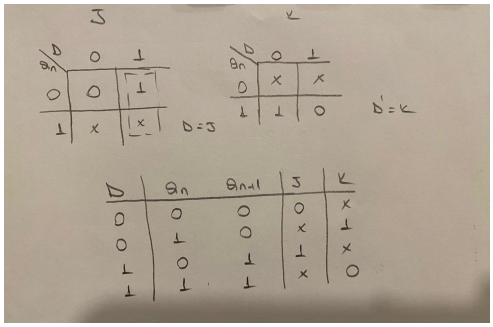

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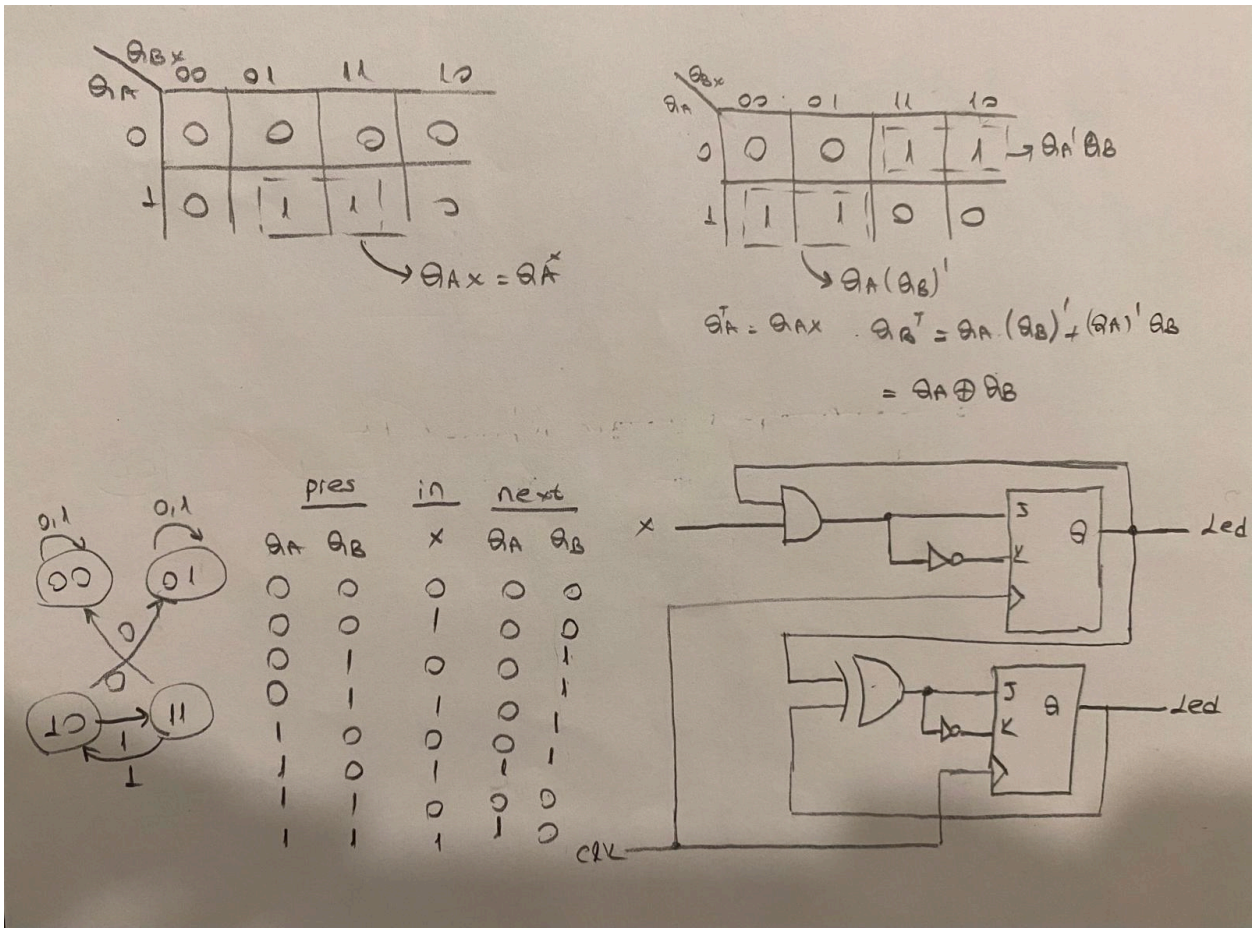
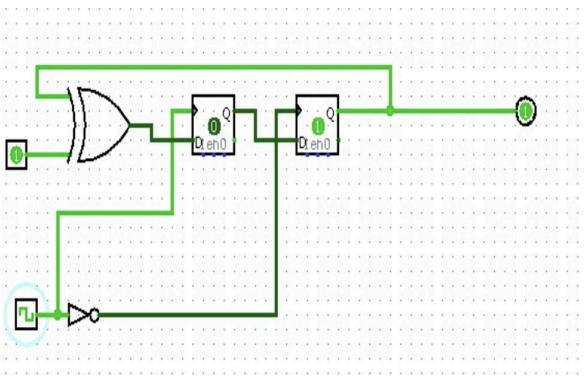


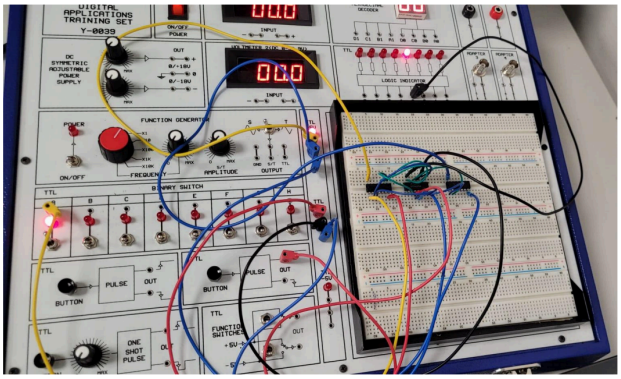

## 2.6:

The circuit shown is a Moore machine because its outputs are determined solely by the current state.

# 3.Experimental Results:

## 3.1:





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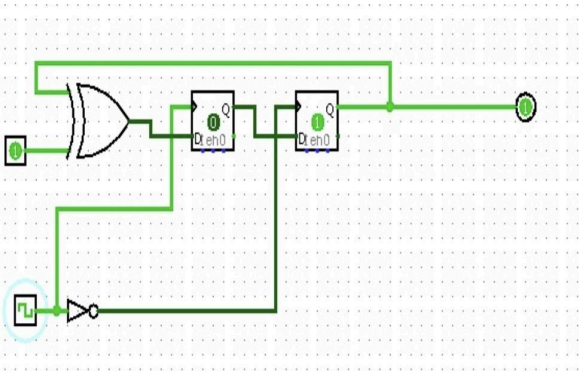

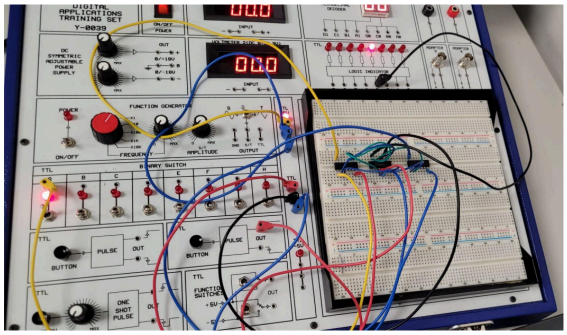

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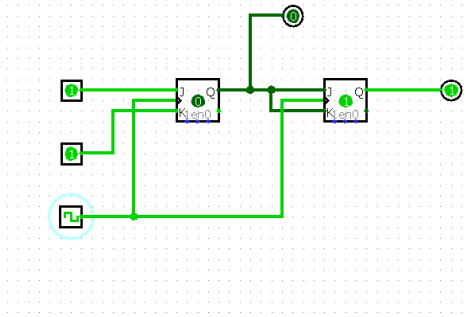

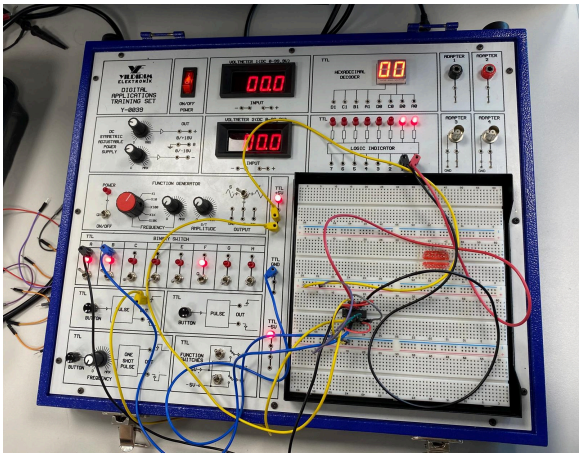

# 4. Discussion:

## 4.1 (5pts) Please discuss the results of the experiments. Generate three questions and responses. What kind of difficulties you faced during the laboratory? Explain them and talk about the methods to resolve.

**Question 1:** Why isn't the clock sign of the second T turn flop always used?
Answer: Setting up a master-slave arrangement is the aim. Master-slave is necessary for the circuit to operate in synchrony with the clock and prevent system flaws. The grasp degree statistics it at the growing area while the slave stage outputs the enter on the falling aspect

**Question 2:** How does the sequential XOR circuit help to end the parity era?
Answer: To determine ıts output country the T turn-flop sequentially executes an XOR operation based mainly on enter bıts. This behavior accumulates the parity bit over a 4-bit collection, producing "0" for even parity and "1" for unusual parity.

**Question 3:** Which packages correspond to the completed circuit depicted in Figure 1?
Answer: If the outputs of the turn-flops are treated as binary bits, this circuit can function as a 2-bit binary counter.

**4.2 (5pts) Discuss the similarities and differences (as well as advantages and disadvantages) between the serial parity generator of this laboratory and the parallel version that we have seen in class (implemented with many XOR gates). Think about the number of bits, the complexity of implementation, delay, performance, etc.**
While both parallel and serial parity mills use parity bits to detect errors, their overall complexity and performance differ. Serial generates parity bit by bit, sequentially, and with little hardware, which makes them easy to use and inexpensive but slower All bit are handled simultaneously by parallel turbines which are much faster but require more hardware and complexity

While parallel circuits are preferred when high performance and on-the-spot effects are crucial serial circuits are better suited for sequential low-strength data packages. The particular application requirements determine the desire.

Serial generator: Slowe simpler and requires significantly less hardware.
Parallel generator: More complicated and requires more hardware but faster.

**4.2 (5pts)** A bill of materials (sometimes bill of material, BOM or associated list) is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, extra parts and the quantities of each needed to manufacture/implement a certain functionality or a product. Generate and discuss the BOM for this laboratory.

- **Breadboard**: 1 unit, 40 TL
- **7486 XOR Gate**: 1 unit, 10 TL
- **7432 OR Gate**: 1 unit, 8.47 TL
- **7404 NOT Gate**: 1 unit, 8.47 TL
- **7475 D Flip-flop**: 1 unit, 86 TL
- **7473 JK Flip-flop**: 1 unit, 12 TL
- **Jumper Cable**: 20.50 TL

**Total**: 174.94 TL

## 5 Labor Authentication:

| TASK | GROUP MEMBERS |
|---|---|
| **Prelab, Breadboard, write report** | **Filiz Köse** |
| **Prelab, Logism, write report** | **Kerim Ercan** |

**Filiz Köse** **Kerim Ercan**