

Laboratory 1-2:

EE203 Digital Systems Design

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Section: 1.1

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1.Introduction

We used them to construct circuits with MUX and simplify Boolean equations prior to the lab. After installing it on Logisim, we filled up a truth table to display the table's numbers on a seven-segment display.

In the lab, we used logic gates to implement a 2:1 MUX and 2:1 MUX components to construct the circuit for the expression we had simplified in the prelab. Finally, we used the Boolean expression of the seven-segment display to generate one of its segments.

Learning to simplify expressions and then testing them out on a breadboard to see how they work was the primary objective of this project.

2.Theory

We first simplified the given statement to ascertain which of the SOP and POS forms had the best V, G, and GN values for prelab work 2.1. The calculations clearly show that the SOP form is the most effective.

2.1

$$F = b(ad' + c(d + a')) = b(ad' + c(a'd')) = b(a \cdot d' + a'cd') \\ = abd' + a'bcd'$$

AB \ CD	00	01	11	10
00				
01				1
11	1			1
10				

$$bcd' + abd' - bd'(a + c) = F$$

$$\sum m(6, 12, 14) \rightarrow \text{SOP is easier}$$

$$\pi m(0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 13, 15)$$

In prelab job 2.2, we noticed that the cost of the equation $ab'(c + d)$ is identical to the cost of the optimal form of expression on prelab 2.1. The expression's G, N, and GN values match those of the first expression's optimal form, proving that their costs are the same.

2.2

$$G = ab'(c + d) = ab'c + ab'd$$

AB \ CD	00	01	11	10
00				
01				
11				
10		1	1	1

$$\text{SOP} = ab'd + ab'c = ab'(c + d) = G$$

$$\text{POS} = (a + b' + d)(a + b' + c)$$

$$\sum m(9, 10, 11)$$

$$\pi m(0, 1, 2, 3, 4, 5, 6, 7, 8, 12, 13, 14, 15)$$

* F and G aren't the same functions, but their implementations will be the same because $F = abd' + bcd' - bd'(a + c)$ and $G = ab'(c + d)$. Both of them can get implemented by using 1 inverter and 3 multiplexers or by using two AND and OR logic gates with 1 inverter.

We first completed the truth table and truth values for each segment on prelab work 2.4 in order to make the design execution process easier. After completing it, we made Karnaugh Maps for each section. This helped us as we were building the circuit by making it simpler for us to extract the Boolean expressions for each part.

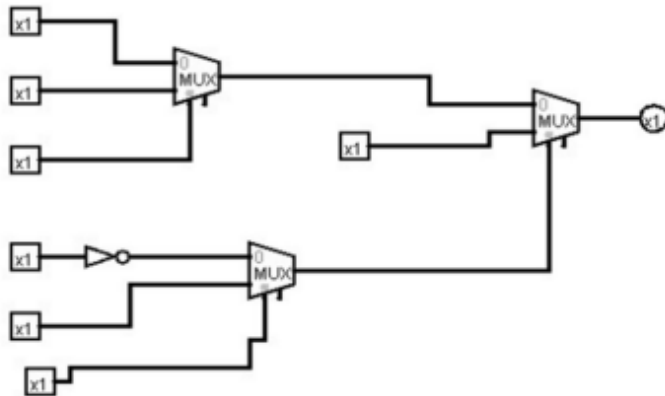


Figure 7: Implementation of work 2.3.

We started by filling up the truth table and truth values for each section on prelab work 2.4 in order to make the design execution process easier. After completing it, we produced Karnaugh Maps for each sector. This facilitated our ability to extract the Boolean expressions for every segment, which came in handy when we were working on the circuit.

ABCD	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	1	1	1
1010	1	1	1	1	0	1	1
1011	0	0	1	0	1	1	1
1100	1	0	0	1	1	1	1
1101	0	1	1	1	1	1	0
1110	1	0	0	1	1	0	1
1111	1	0	0	0	1	1	1

	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	x	x	x	x
10	1	1	x	x

$$\overline{B}\overline{D} + C + BD + A$$

	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	x	x

$$\overline{B} + \overline{C}\overline{D} + CD$$

	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

$$\overline{C} + D + B$$

	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	x	x	x	x
10	1	1	x	x

$$\overline{B}\overline{D} + \overline{B}C + C\overline{D} + B\overline{C}D + A$$

	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	x	x

$$\overline{B}\overline{D} + C\overline{D}$$

	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

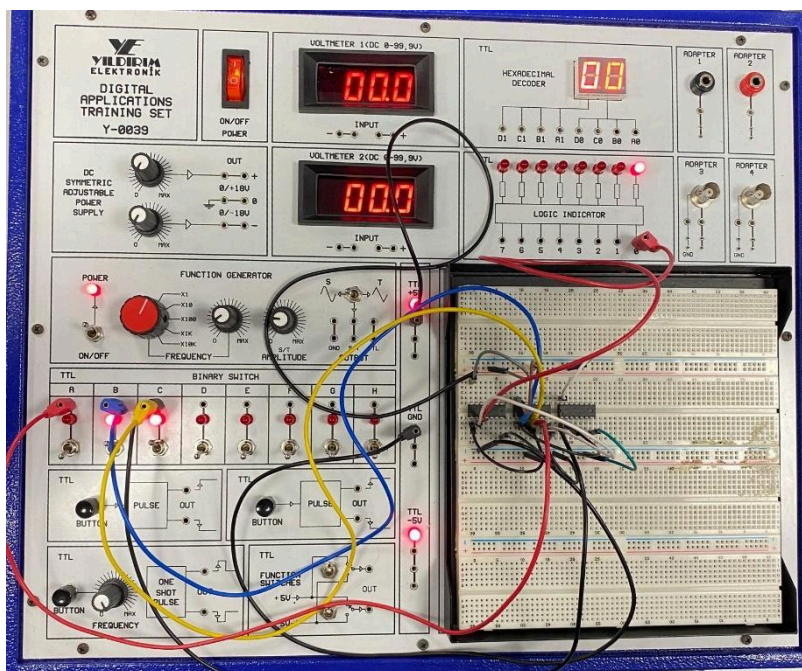
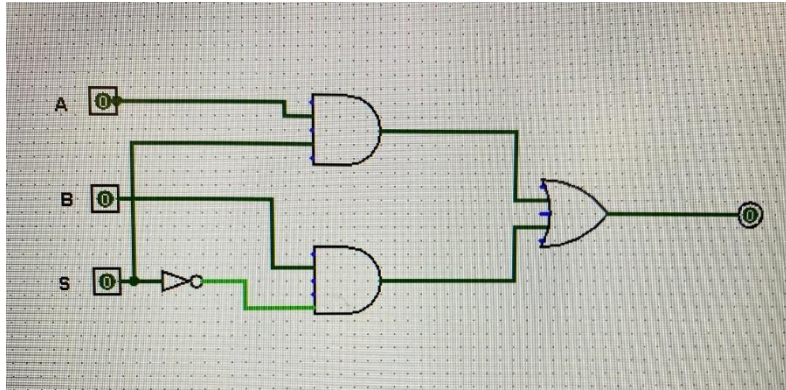
$$\overline{C}\overline{D} + B\overline{C} + B\overline{D} + A$$

	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

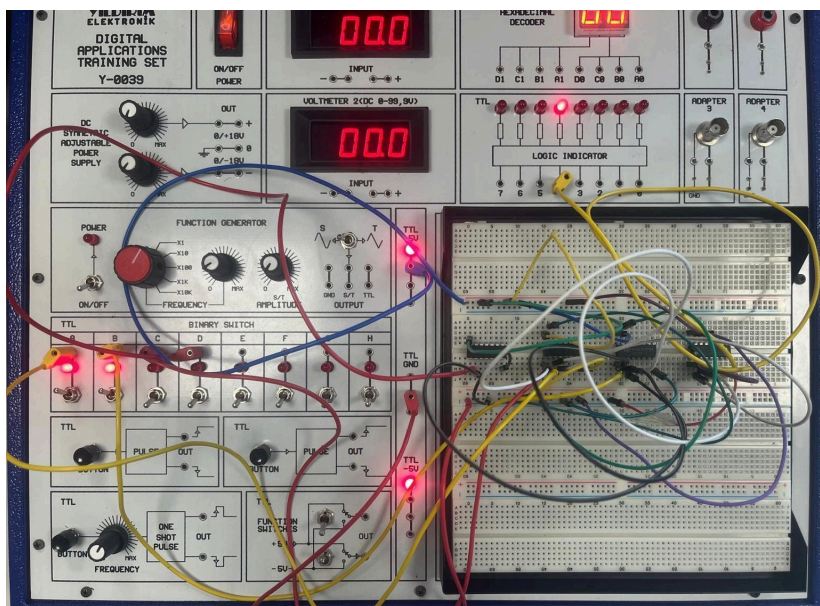
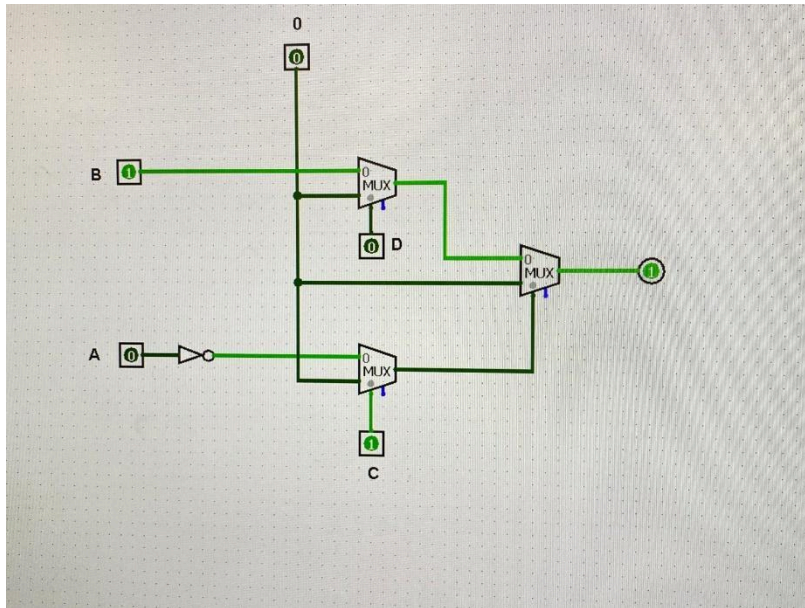
$$\overline{B}C + B\overline{C} + B\overline{D} + A$$

3. Experimental Results

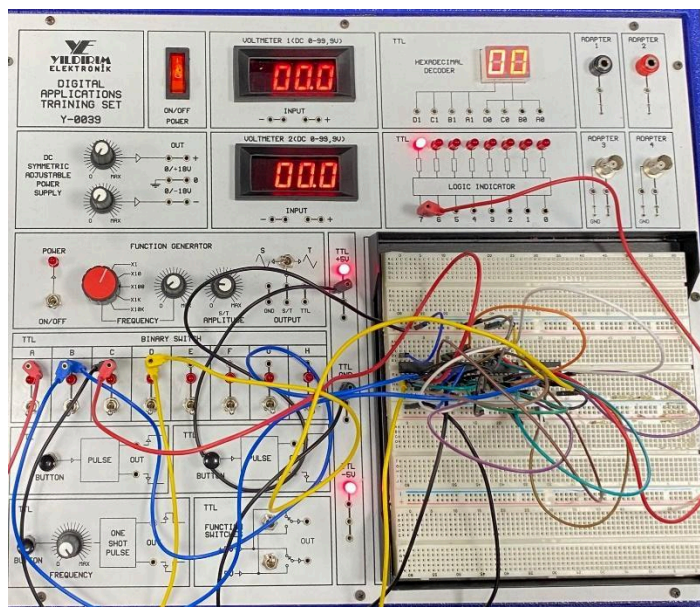
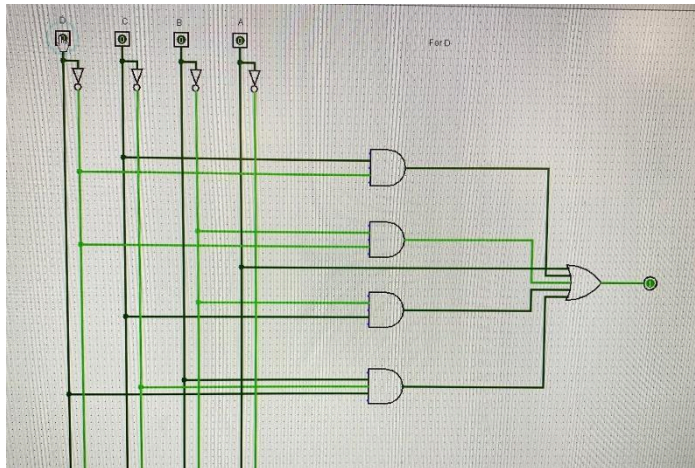
Using NOT, AND, and OR gates, we constructed a 2:1 MUX in compliance with the guidelines in Experiment 3.1. S represents the SELECT pin, whereas A and B represent the inputs. On the breadboard, the letters A and B stand for S and A and B, respectively.



We built the circuit in 2.3 using three quad MUX components on 3.2.



Experiment 3.3 required us to use the segment D circuit on the seven-segment display. The circuit was constructed using the expression derived from the Karnaugh Map.



4. Discussion

4.1 (10pts) Please discuss the results of the experiments. Comment on the external factors that occur during the experiment. Give examples of the real-life use of the models you implemented in the experiment.

During the experiments, outside factors like ambient temperature or electric interference might have an effect on the components used. For example, the multiple-enter MUX circuit may be used as a channel selector in televisions, wherein it manages input alerts and selects a specific channel.

4.2 (8pts) A bill of materials (sometimes bill of material, BOM or associated list) is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, extra parts and the quantities of each needed to manufacture/implement a certain functionality or a product. Generate and discuss the BOM for this laboratory. Calculate the total cost for each experiment. You can use the prices you find on the internet for this.

The bill of material (BOM) contains a list of all the components used in the circuit. This lab uses a MUX 2:1 circuit, some logic gates, and seven segment display. You can find component prices online, and find the total cost of each implementation. For example, the cost of a MUX IC, basic logic gate, resistor, and LED display can be calculated as follows:

2:1 Multiplexer ICs (2 units): \$0.35 each, \$0.70 total.

Basic logic gates (not and, or, or): Each IC costs approximately \$0.10, with an estimated total cost of \$0.30 for each.

Resistors and LEDs (10 units): \$0.06 each, \$0.60 total.

This brings the estimated total cost to \$1.60.

1 Labor Authentic

The following table details the labor distribution among group members:

Task	Group Member Responsible
derive a truth table, create a K-map, set up a logic circuit, prepare a prelab, simplify functions	Filiz Köse
derive a truth table, create a K-map, set up a logic circuit, prepare a prelab, draw a circuit using Logisim	Kerim Ercan

Each group member attests to the accuracy and completion of the job claimed by signing the following:

Filiz Köse

Kerim Ercan