Laboratory 5-6:
Sequential Circuits
EE 203 Digital Systems Design

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1 Objective

Objective of this laboratory session is to design, test and demonstrate how se quential logic circuits work using flip-flops combined with combinational circuits. More specifically, we would like to explore the ways storage devices and logic gates can be used together to create a sequential circuit. It uses a combination of feedback (the current state of a storage device) together with combinational logic to create a device implementing a predefined and useful function.
Your designs should be as least gate-consuming design as possible. Make sure also that you use minimum wiring for circuit efficiency and save yourself from complicating your job. Each question has its points written down next to it. Although point-wise percentage of the Prelab. work is relatively low, it is quite essential to the overall lab experience, particularly to be able to get the experi ments done correctly.
Teaching assistants are free to give extra bonus points (up to 10) depending on your performance in the lab., how neat you work with electronic components, actively engage in or collaborate with your group member/s.

2 Prelab work

There are two parts to this experiment. In the first phase, we will implement a T-flipflop from two latches and find a use case where it is quite useful i.e., parity generation. The first three questions explore the first phase of the experiment. In the second phase, we shall explore the analysis of a given sequential circuit logic diagram. The logic diagram is drawn using D-flipflops, in order to use JK-flipflops, necessary transformation should be performed. Eventually, this

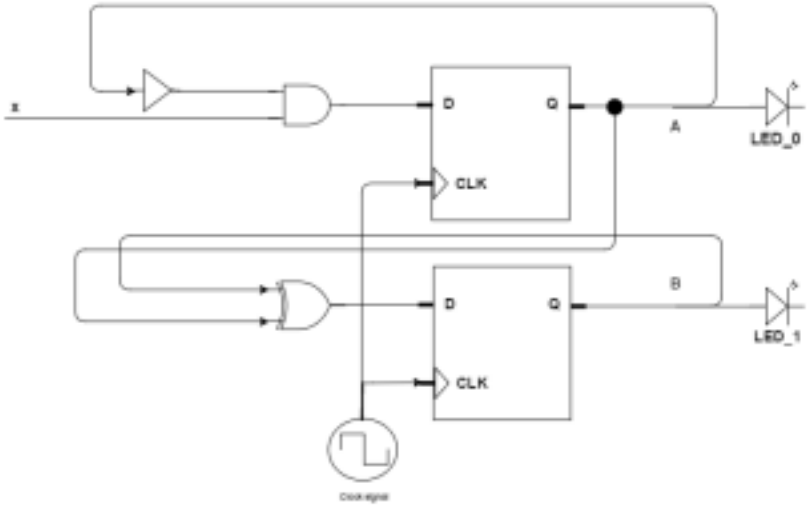
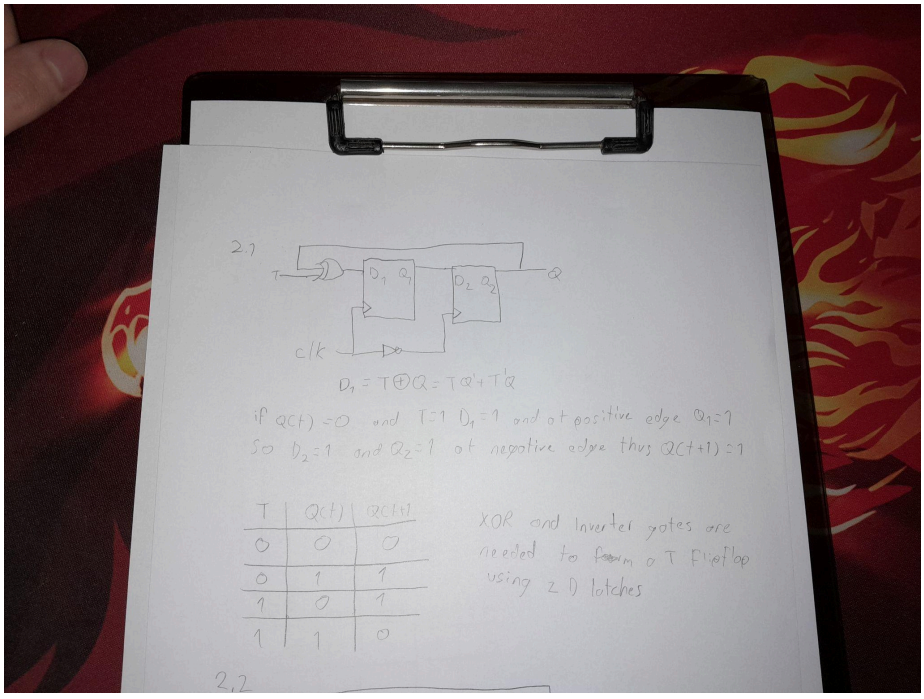


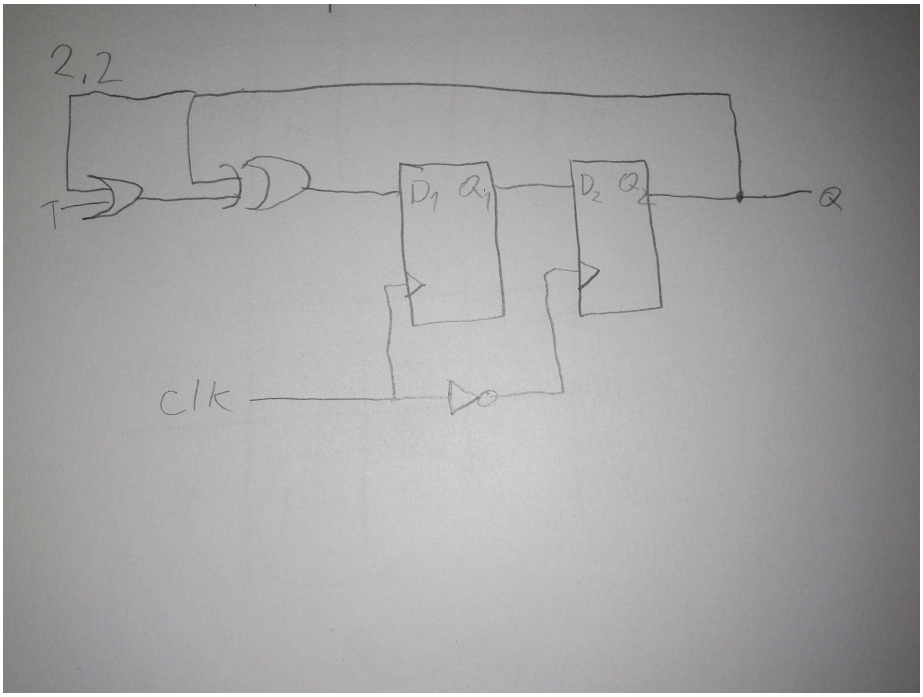
Figure 1: A sequential logic circuit diagram.

phase of the experiment consists of constructing the given sequential circuit using two JK-flipflops. The rest of the questions explore the second phase of the experiment.

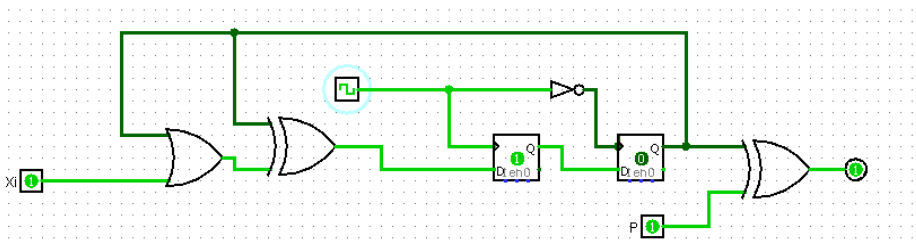
2.1 (7pts) We would like to design a T-flipflop using two D-latches. Design this circuit using a Master-Slave approach and draw the corresponding truth and state tables. Please provide a short description of how your circuit works. How many extra logic gates you need? What are those gates?



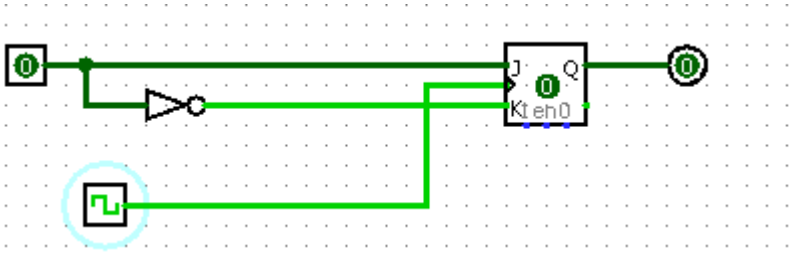
2.2 (7pts) Use your T-flipflop to sequentially perform XOR operation for four bits. So the output of the circuit for an input of 1011 should give you logical “1”. Note that this is also the even parity bit of the 4-bit word in question. Therefore, your circuit is a sequential(serial) parity generator!.

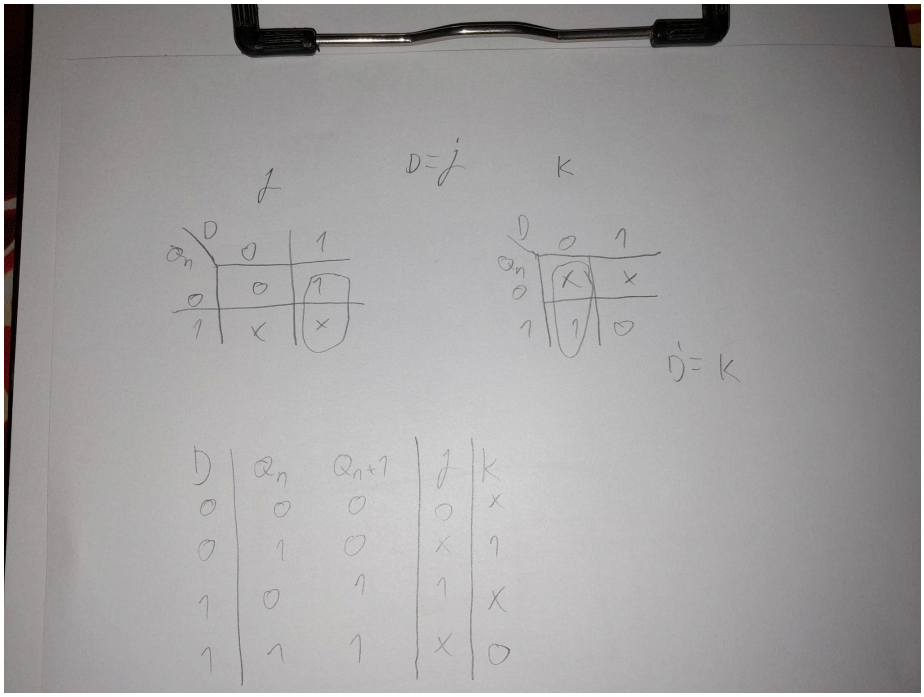


2.3 (7pts) Discuss whether you can use your parity generator as a parity checker? In otherwords, can you use the same circuit to detect a single bit error? Draw your logic diagram in Logisim with a single output being 1 if the parity does not check and 0 if the parity checks.

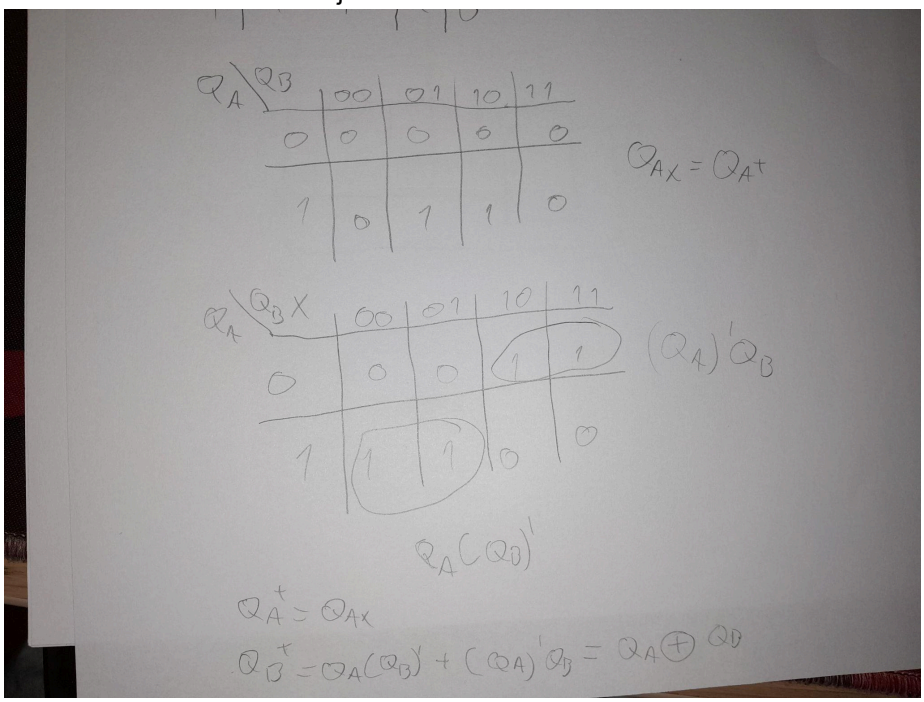


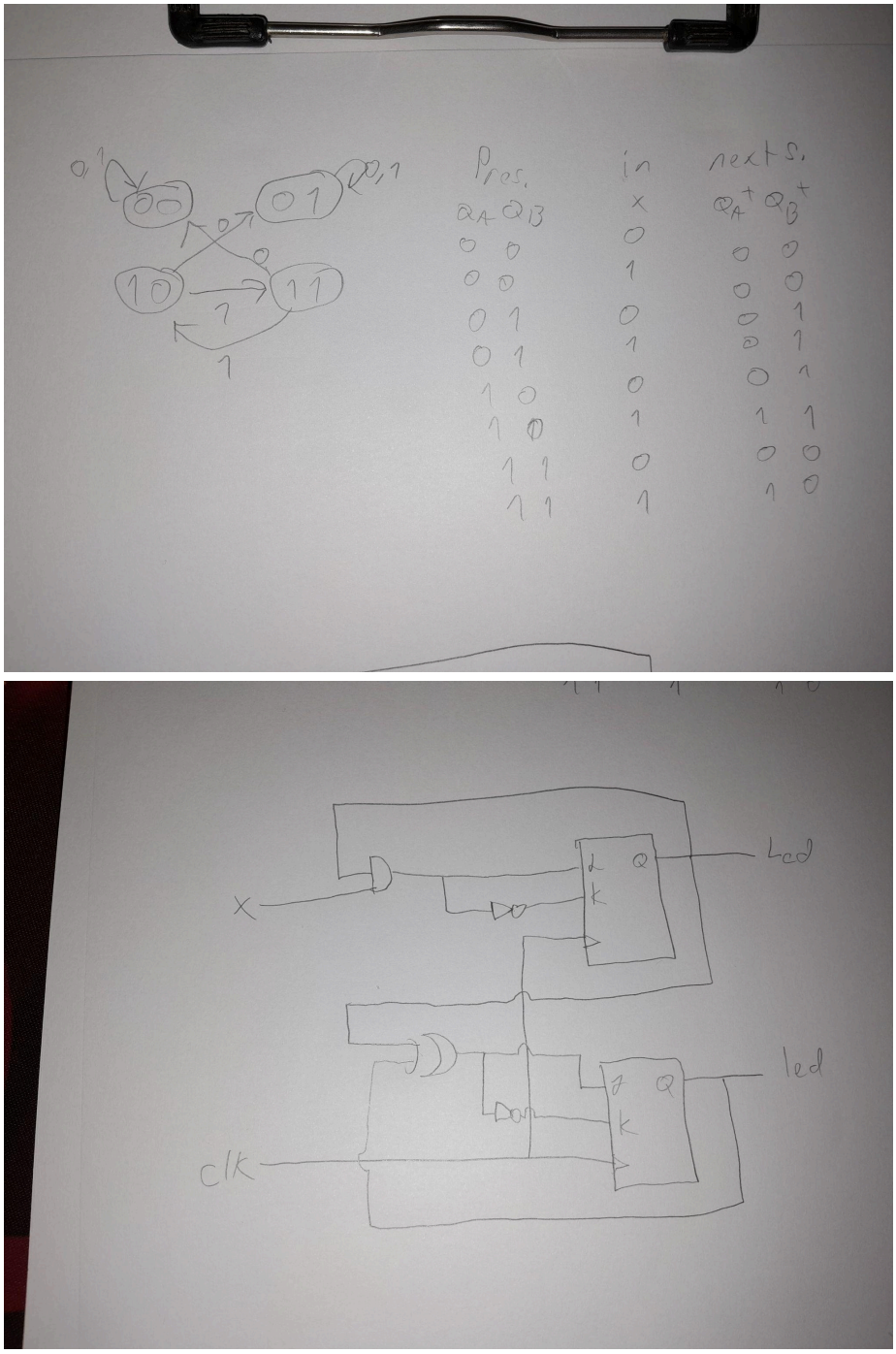
2.4 (6pts) In this question, we also would like to design a D-flipflop using a JK flipflop. Draw the logic diagram of your transformation in Logisim and verify the truth and state tables of the D-flipflop.





2.5 (5pts) Using two D-flipflops (two JK flipflops and some logic gates in your case), let us connect the circuit shown in Fig. 1. Can you minimize the combinational circuit component of the sequential circuit?. Use Karnough maps to explore this. Drive the state equations and draw the state diagram of the circuit. Make a conjecture about the behaviour of the circuit.





2.6 (3pts) Is the circuit in Fig. 1 a Mealy or Moore machine? Provide your reasoning along with your answer.

Because the outputs of the circuit above rely on both the inputs and the current state, it is a Mealy machine. When it comes to modeling systems with outputs that are dependent on changes in inputs, Mealy machines are renowned for their adaptability.

3 Experimental work

3.1 (15pts) Design a T-flipflop using two D-latches as asked in 2.1. Construct your circuit and verify your truth and state tables on the breadboard. 3.2 (15pts) Using your T-flipflop, construct your parity generator circuit. Use available LEDs on your breadboard for logic verification.
3.2 (20pts) Implement the circuit of Fig. 1 using minimum number of ICs. •

Use LEDs to monitor the Q outputs of the two flip-flops.

- Please pick the LED for A1 to be on the left of the LED you choose for A0.
- Use clear (reset) terminals of the flipflops to clear the content of the flipflops (Q = 0).
- Repeatedly apply clock pulses to the circuit and observe the two Q outputs until you discover the pattern and tell what this sequential circuit is doing.
- Report your observations using a characteristic table.
- Based on your observations, what useful circuit have you constructed?

4 Discussion of Experiment Results

4.1 (5pts) Please discuss the results of the experiments. Generate three ques tions and responses. What kind of difficulties you faced during the laboratory? Explain them and talk about the methods to resolve.
4.2 (5pts) Discuss the similarities and differences (as well as advantages and disadvantages) between the serial parity generator of this laboratory and the parallel version that we have seen in class (implemented with many XOR gates). Think about the number of bits, the complexity of implementation, delay, per formance, etc.
4.2 (5pts) A bill of materials (sometimes bill of material, BOM or associ ated list) is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, extra parts and the quantities of each needed to manufac ture/implement a certain functionality or a product. Generate and discuss the BOM for this laboratory.