# EEAIC 2022 PLL - Final report

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## I. Introduction

**This paper presents the implementation of a Phase-Locked Loop (PLL) in the TSMC 65-nm CMOS process based off the Class-D oscillator introduced by Fanori and Andreani in [1]. Class-D oscillators produce less phase noise compared to the class-B/C architectures for the same power consumption, at the expense of higher power supply than their counterparts. This work looked at implementing a Class-D VCO in a realistic PLL design where non-idealities were also taken into account. Current consumption, phase noise and figure-of-merits were derived and compared with the reference paper. The PLL runs at a supply voltage of 1.2V with a total power consumption of 3.837mW, with the VCO consuming 1.947mW which is substantially lower than the 4mW reported in the reference paper. The VCO exhibits a phase noise of -141.312 dBc/Hz at 10MHz, with a tuning range of 4%.**

## II. Design specifications

In order to design a realistic design, some metrics needed to be chosen.

| Parameter | Value | Unit |
|---|---|---|
| $f_{vco}$ | 4 | GHz |
| $f_{ref}$ | 31.25 | MHz |
| $P_{tot}$ | <4 | mW |
| $FoM_{VCO}$ | <-191 | dBc/Hz |
| $\phi_{n,vco}$ @ 10MHz | <-143.5 | dBc/Hz |

TABLE I: Initial design criteria for the PLL

## III. PLL Design and Components.

We aimed for a Type-II PLL using a fully analog control circuitry. In the following subsections, we will go through the choice of the components used for the realisation of the design.

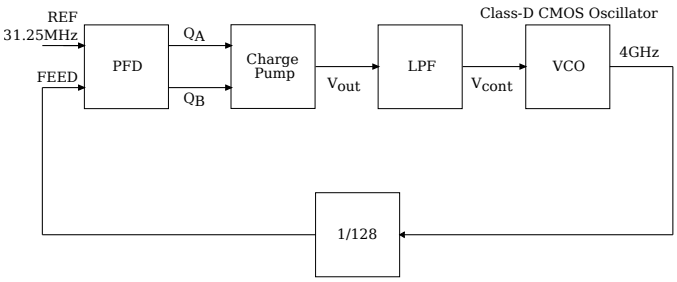


Fig. 1: Block diagram for the PLL design.

### A. Phase Frequency Detector (PFD)

The PFD, inspired from [2], has a role of generating switch signals $Q_a$ and $Q_b$ for the charge pump depending on which

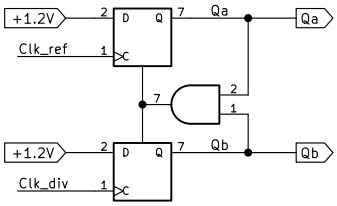


Fig. 2: PFD Schematic

clock is lagging or leading. Those states are generated on rising edges of $Clk_{ref}$ and $Clk_{div}$ respectively. If $Clk_{ref}$ is leading, we first generate a pulse $Q_a$ that is pushing current into the low pass filter to raise the VCO control voltage $V_{cont}$. If $Clk_{div}$ is rising first, $Q_b$ is turned on first and the charge pump will pull current to ground, decreasing $V_{cont}$. The pulses are reset when the other clock has a rising edge.

### B. Charge Pump (CP)

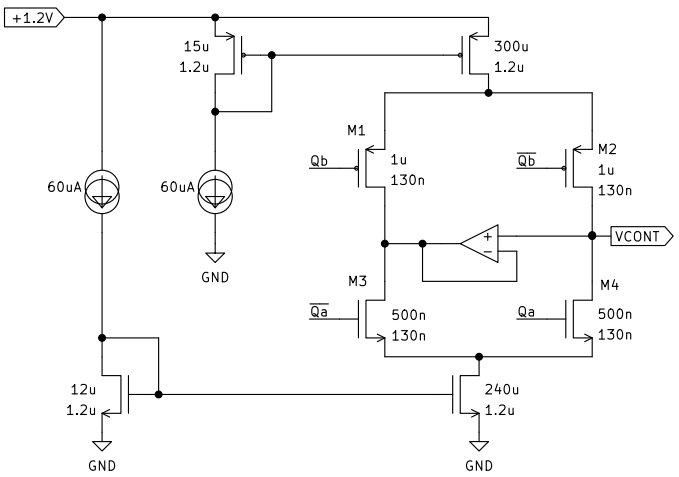


Fig. 3: Charge Pump Schematic

As we can see in Fig. 3, a simple current steering concept was used in order to keep a constant current flow at all times for better output control. Upon $Q_a$ being high, the transistor M1 turns off and M3 is turned on, injecting current to the loop-filter. Upon $Q_b$ being high, it would have the opposite to $Q_a$, turning off M3 and turning M4 on, depleting current from the loop-filter as it would be connected to ground. If $Q_a$ and $Q_b$ are both off, the left branch is still drawing current. This keeps the $V_{ds}$ node voltages of the PMOS and NMOS current sources transistor constant. This is necessary in order to keep the parasitic capacitance $C_{ds}$ of all transistor fully charged at all times, instead of depleting them due to the charge sharing nature of the capacitance in the loop-filter. In order to do so, the operational amplifier between the two

branches keeps $V_{cont}$ constant on both sides of the branches and keeps the parasitic capacitances charged. Therefore the charge pump and the loop-filter charge sharing is minimised which improves dynamic current matching. CP phase noise is primarily given by the channel thermal noise component of the current source $\bar{i_d^2} = 4KT\gamma g_m$.

### C. Loop Filter (LF)

In order to ensure stability of the PLL loop dynamics described in section V, a higher order filter needs to be used. In this project, a simple 2nd order filter was designed using two capacitors and a resistor.

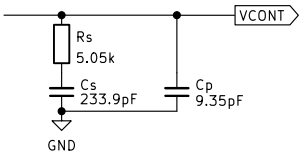


Fig. 4: 2nd order loop filter schematic

### D. Frequency Divider (FD)

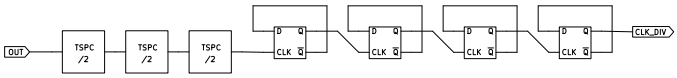


Fig. 5: Frequency divider block diagram

The frequency divider is using 3 daisy chained TSPCs with a division factor of 2, along with 4 daisy chained flip-flops with a division factor of 2. This gives in total a division factor of $2^7 = 128$. The full schematic and operation is available in Appendix VIII-B.

The TSPC blocks are responsible for frequency division of high frequency clock signals, whereas the flip-flops are more suitable for slower signals, since the TSPC topology fails at slower clock frequencies due to high leakage currents. Finally, the output of the last divider stage goes into the PFD block, which completes the PLL Loop.

## IV. Class-D VCO

The main building block of every PLL is the VCO. This project was aimed at integrating the Class-D oscillator as envisioned by [1] and benchmark its performances in a Type-II PLL.

In Fig. 6 is the schematic of the implemented VCO for the PLL. It shows discrepancies from the ideal VCO as we needed to account for parasitics in order to simulate a realistic environment.

*1) Inductor Model:* In order to simulate a realistic inductor in the VCO, a simplified model needed to be realised. By choosing an inductance of 500pH, and a Q-factor of 15 (which is realistic for a moderately designed inductor), other parasitic elements can be calculated as follows. The quality factor for an ideal inductor is:

$$Q = \frac{\omega L}{R} \tag{1}$$

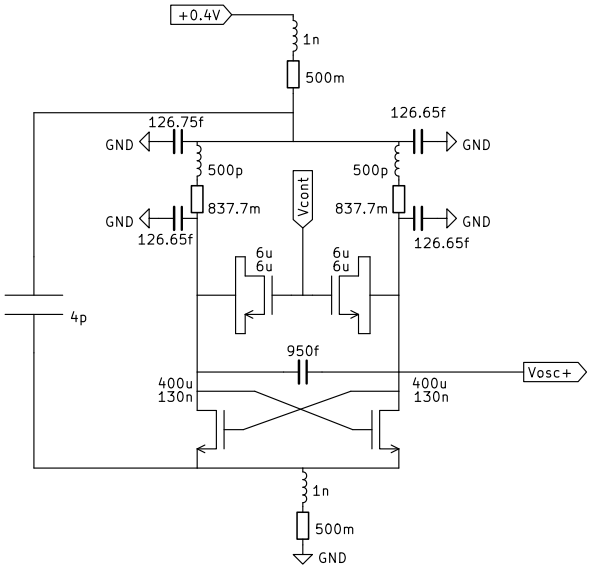


Fig. 6: Class-D VCO Schematic

and by simplifying for R, we can calculate the parasitic resistance:

$$R = \frac{\omega L}{Q} = 837.7m\Omega \tag{2}$$

where $\omega = 2 \cdot \pi \cdot f_{osc}$, where $f_{osc} = 4$GHz. Now we state that we have a oscillating harmonic at 5 times the oscillation frequency, and using:

$$\omega_H = 5 \cdot \omega = \frac{1}{\sqrt{LC}} \tag{3}$$

and solving for C, we get:

$$C = \frac{1}{\omega_H^2 L} = 126.65f\text{F} \tag{4}$$

*2) Wire Bonding:* Because of the severe supply pushing of the Class-D oscillator, it is of extreme importance to simulate the off-chip wire bonding instead of using a clean power supply in order to see the supply pushing effect on the output of the oscillator. In order to simulate a realistic wire bonding, an inductor of 1nH and a resistor of 500mΩ were attached on both ground and $V_{dd}$. Along with the off-chip parasitics, a capacitor of 4pF was added between the rails in order to suppress the harmonics introduced by the parasitics.

### A. Tuning Range

In order to control the oscillation frequency of the oscillator, a way to change either the inductance or the capacitance of the LC tank has to be developed. In a real design, it is extremely hard to change the inductance as the inductor has a fixed size (area of metal on a substrate), so the easiest and most-common choice is to vary the capacitance of the LC-tank using a so-called varactor. Different configurations can be used in order to adjust the capacitance of the LC-tank. In this report, two transistors were chosen in a back-to-back configuration, by using their parasitic capacitance when operated in the triode region. The control voltage from the charge pump ($V_{cont}$) was connected to the gates of both transistors, and their bulk (drain,

source and body) were connected to the differential output ports of the VCO. By doing so, an acceptable tuning range could be chosen.

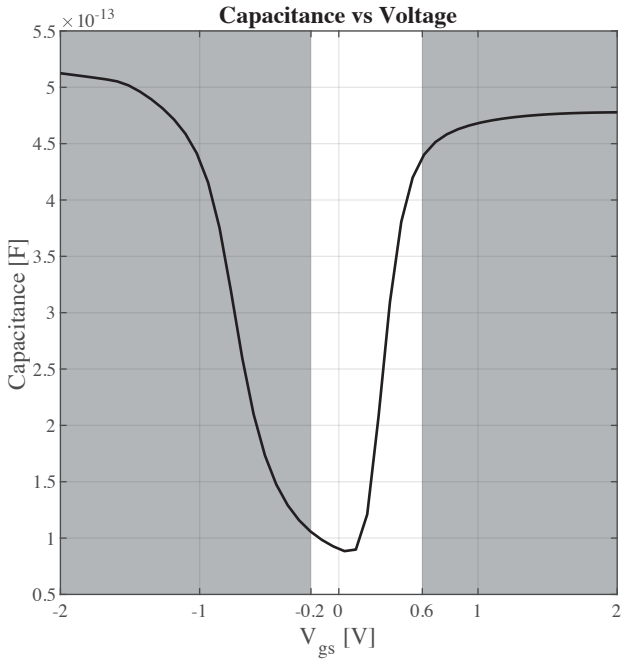


Fig. 7: Capacitance of tuning varactors plotted over applied voltage

As we can see from Fig. 7, the white area of the capacitance curve is the available working range of capacitance with the given oscillation amplitude and the given control voltage amplitude. Due to the asymmetrical nature of the Class-D oscillations, the simple formula $\omega_{osc} = \frac{1}{\sqrt{LC}}$ cannot be used in order to determine the running frequency of the oscillator. A more elaborated analysis needs to be carried out [1], but a simple simulation can also suffice by simply sweeping the control voltage and simultaneously plotting the oscillation frequency $f_{osc}$.

As we can see in Fig. 8 the range varies from [3.9-4.05] GHz, with the target frequency achieved when $V_{cont} \approx 630m$V, resulting in a gain factor of $K_{vco} = 220$MHz/V. Special care needs to be taken when defining the range of $V_{cont}$, since it can sacrifice the closed loop stability of the PLL if too low.

### *B. Phase Noise and FoM*

Phase noise can be described as random phase fluctuations at the output of the VCO. These fluctuations are caused by time-domain instabilities usually referred to as phase jitter. The phase noise is relative to the carrier frequency ($f_{osc} = 4$GHz).

As we can see in Fig. 9, we see the two main noise contributors to the phase noise, namely the upscaled flicker noise and the upscaled thermal noise. The corner where the thermal noise starts dominating over the flicker noise has been meticulously chosen at 180kHz. This will depend on the overall noise of the PLL's performance which will be discussed better in section VI-A.

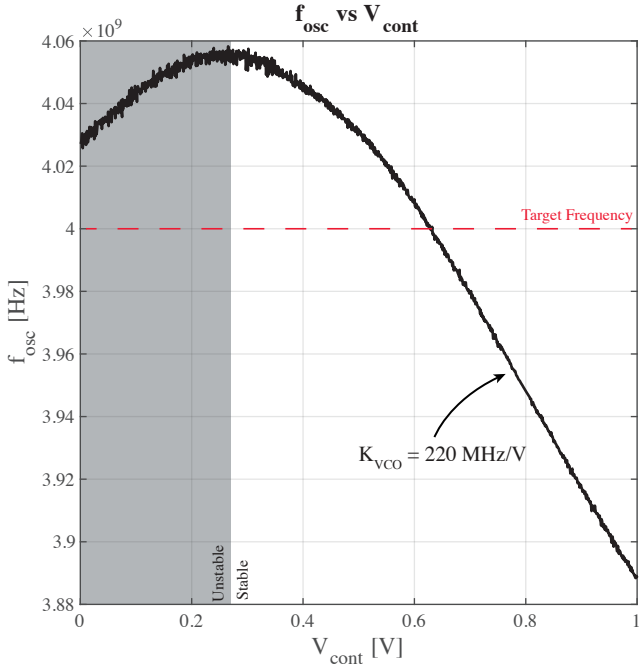


Fig. 8: Oscillation frequency plotted over control voltage.

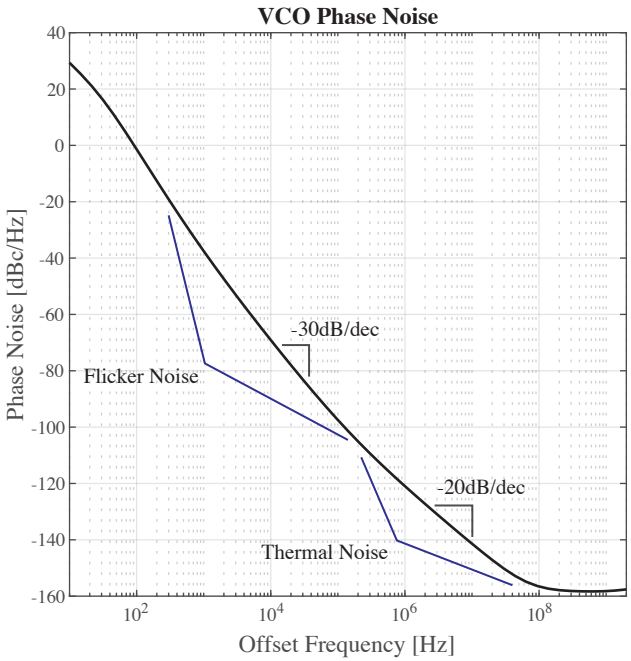


Fig. 9: Phase noise of the Class-D VCO

In order to compare the VCO design with other designs on the market, the best benchmark is the Figure-of-Merit (FoM). Which compares the phase noise with the power needed to achieve that noise level. The FoM yields:

$$FoM_{vco} = L(\Delta f) - 20log\left(\frac{f_{osc}}{\Delta f}\right) + 10log\left(\frac{P_{vco}}{1\text{mW}}\right) \quad (5)$$

$$= -190.4\text{dBc/Hz} \quad (6)$$

where $L(\Delta f) = -141.312$dBc/Hz, $\Delta f = 10$MHz, $f_{osc} =$

4GHz and $P_{vco} = 1.947$mW.

### C. PVT Variations

Due to PVT (Process-Voltage-Temperature) variations the PLL behaves differently than under ideal conditions. For the operation of the PLL, the biggest concern is the frequency tuning range of the VCO (see Fig. 10). In order to keep things simple, the only PVT variations of interest were the ones that had the most impact on the tuning range of the VCO. After running a bulk of initial simulations, three corners were chosen which displayed the highest range of tuning range.

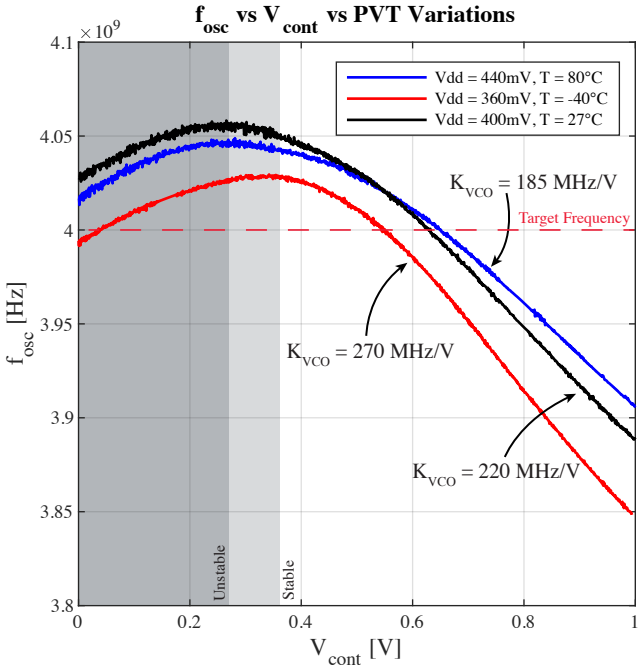


Fig. 10: Frequency tuning range in terms of PVT variations.

As we can observe on Fig. 10, which shows the best and worst case scenarios for the PVT variations, the frequency gain of the VCO $K_{VCO}$ is heavily affected. This $K_{VCO}$ difference will impact the PLL noise characteristics and the loop bandwidth would ideally have to be adjusted again to match the new crossover frequency between the VCO and CP noise curves. However, it is possible to change $I_{CP}$ accordingly to conserve the same noise figure. Under PVT variations the frequency tuning crosses our target frequency of 4GHz, which indicates that the PLL will be able to lock under any conditions. It might however experience longer locking times at lower $K_{VCO}$. We also see that in order for the PLL's closed loop to be stable, the voltage control range must be limited between [0.35V-1V] when the VCO reaches higher $K_{VCO}$ while having a wider range of [0.25V-1V] for smaller $K_{VCO}$.

As we can see from Fig. 11, the main change in phase noise because of PVT variations happens in the flicker noise region. That proves to be non-crucial since the transfer function for the noise of the VCO attenuates the flicker noise sufficiently.

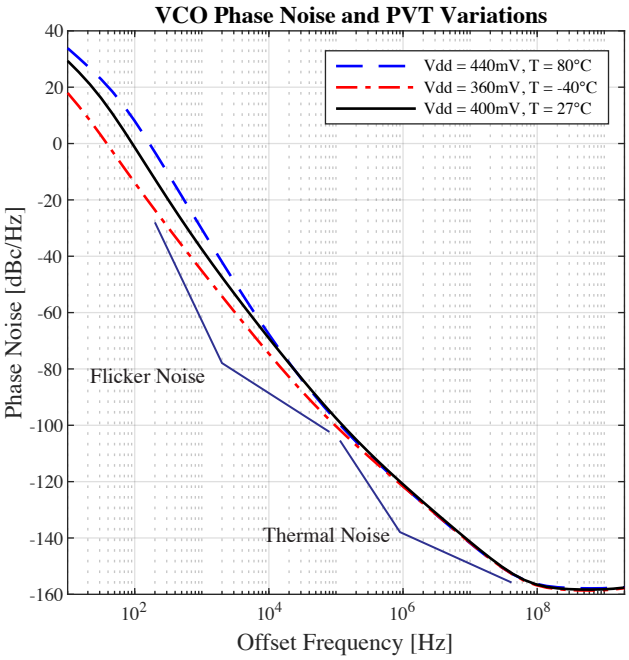


Fig. 11: Phase noise dependent on PVT variations

| $K_{VCO}$ | Voltage | Temperature | Library |
|---|---|---|---|
| Nominal | 400mV | 27°C | tt_lib |
| High | 360mV | -40°C | sf_lib |
| Low | 440mV | 80°C | sf_lib |

TABLE II: Chosen PVT corners for all simulations

## V. PLL Loop Dynamics

The PLL closed-loop dynamics (type-II system) is unstable as such, due to the non-existent phase margin as constant phase is -180°. This is usually compensated by the addition of a resistor $R$ in between the CP and the VCO, which adds a zero for the loop stability. Additionally, we add another capacitor $C_2$ in parallel to $RC_1$ which is used to minimize the ripple on the control voltage.

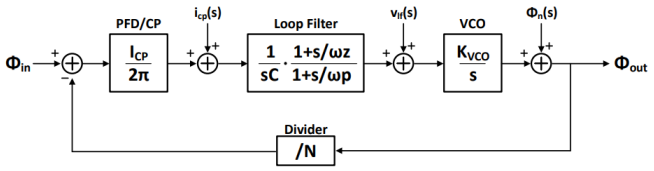


Fig. 12: PLL block diagram of transfer function

Ignoring the charge sharing capacitor, the closed-loop transfer function in the Laplace domain is given by:

$$H_{CL}(s) = \frac{\frac{I_{cp}K_{VCO}}{2\pi C_1}(sRC_1+1)}{s^2 + \frac{I_{cp}}{2\pi}\frac{K_{VCO}}{N}Rs + \frac{I_{cp}}{2\pi C_1}\frac{K_{VCO}}{N}} \tag{7}$$

We identify it to a second order system which is in the general case expressed as:

$$H(s) = \frac{{\omega_n}^2}{s^2 + \zeta\omega_n s + {\omega_n}^2} \tag{8}$$

We define $\omega_n$ and $\zeta$ in eq. 8 as such[1]:

$$\omega_n = \sqrt{\frac{I_{CP}}{2\pi C_1}\frac{K_{VCO}}{N}} \quad \zeta = \frac{R}{2}\sqrt{\frac{I_{CP}C_1}{2\pi}\frac{K_{VCO}}{N}} \tag{9}$$

The PLL loop bandwidth of 281 kHz was optimized to match the crossover frequency of the charge pump and VCO phase noise curves and with a trade off between integrated jitter and lock time. The detailed optimisation process is explained in section VI.

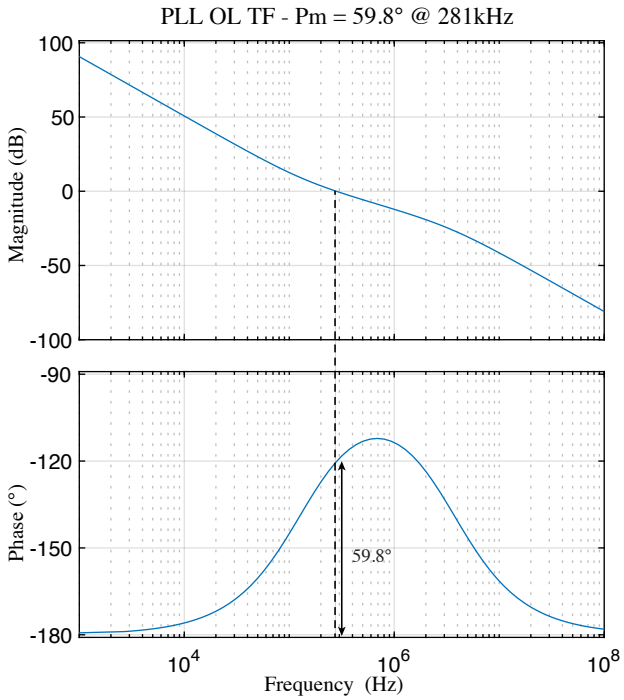


Fig. 13: PLL Open Loop Dynamics

As we can see from Fig. 13, the open loop gain of the PLL dynamics has a phase margin of 59.8°at 281kHz.

## VI. Results

We ran a transient simulation of the whole PLL using Cadence Spectre. The resulting graphs are shown below.

As seen in Fig. 14, our PLL locks with success on the target frequency with a lock time of 5.05$\mu$s. In the further subsections, we will introduce the noise figures, the overall Figure-of-Merit for the entire PLL as well as the design resilience against PVT variations.

### A. Noise

The biggest concern of a PLL is it's noise contribution. Every block of the PLL introduces it's own noise transfer functions, which in return contributes to the overall noise level of the PLL. In this work, the noise contribution of the reference clock is considered out of scope.

[1] $K_{VCO}$ = 220MHz/V, $I_{CP}$ = 1.2mA, $N$ = 128, $C_1$ = 233.9pF, $R = 5.05K\Omega$

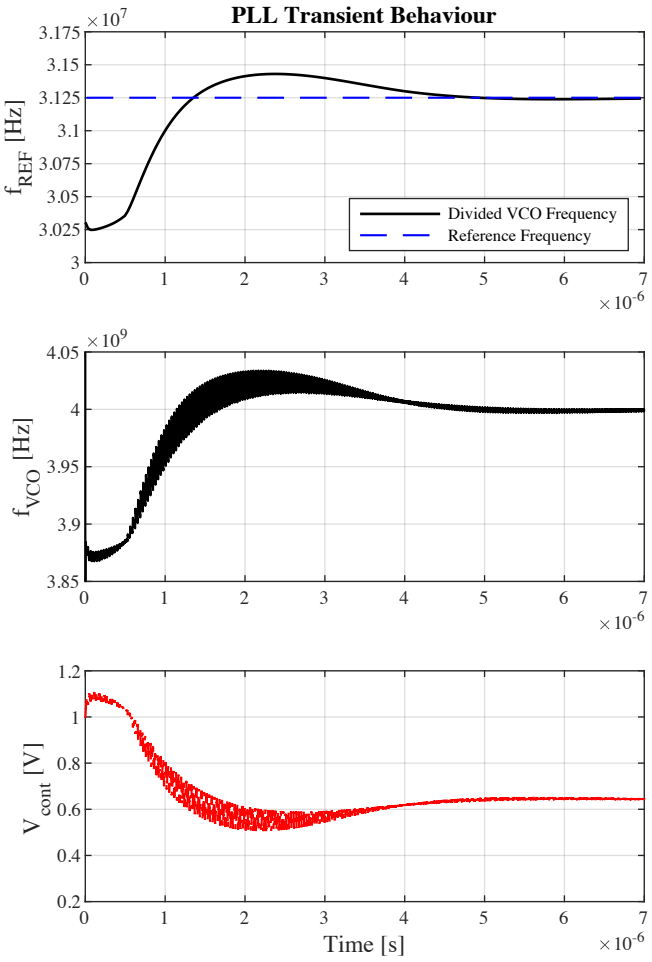


Fig. 14: (a): $\frac{f_{VCO}}{N}$ against $f_{REF}$ plotted over time.
(b): $f_{VCO}$ plotted over time.
(c): $V_{cont}$ plotted over time.

As we can see from Fig. 15, the the noise from the charge pump and and the VCO are nicely optimised in order to minimise the overall noise. Because of that, the overall noise is solely dominated by the loop-filter noise. Since the loop filter only consists of passive elements, it introduces a fixed noise floor that provides a hard limit to what can be achieved when it comes to noise optimisation.

### B. Figure-of-Merit

By integrating the total noise from Fig. 15, the absolute RMS-jitter can be computed. The absolute RMS-jitter is defined as:

$$\sigma^2_{t,PLL} = \frac{1}{2\pi^2 f_0^2}\int_0^\infty L(f)\,df \tag{10}$$

and the FoM of the PLL is defined as:

$$FoM_{PLL} = 10\log\left[\left(\frac{\sigma_{t,PLL}}{1s}\right)^2\frac{P_{PLL}}{1mW}\right] \tag{11}$$

With $\sigma_{t,PLL}$ = 79.2fs and $P_{PLL}$ = 2.8974mW we get an FoM value of:

$$FoM_{PLL} = -257.4\text{dBc/Hz} \tag{12}$$

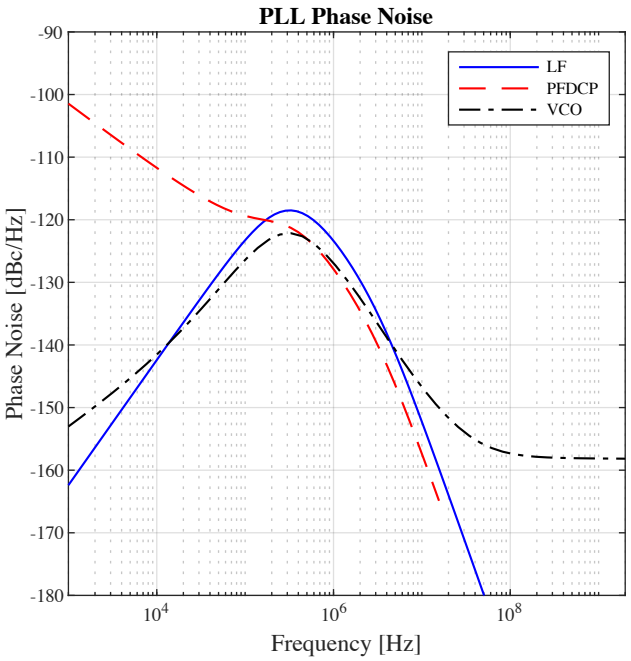


Fig. 15: All noise contributions in the PLL.

### C. PVT Variations

One of the biggest design criteria of every PLL design, is its robustness to PVT variations. By choosing the three important corners mentioned in Tab. II, we can predict the overall noise performance of the PLL.

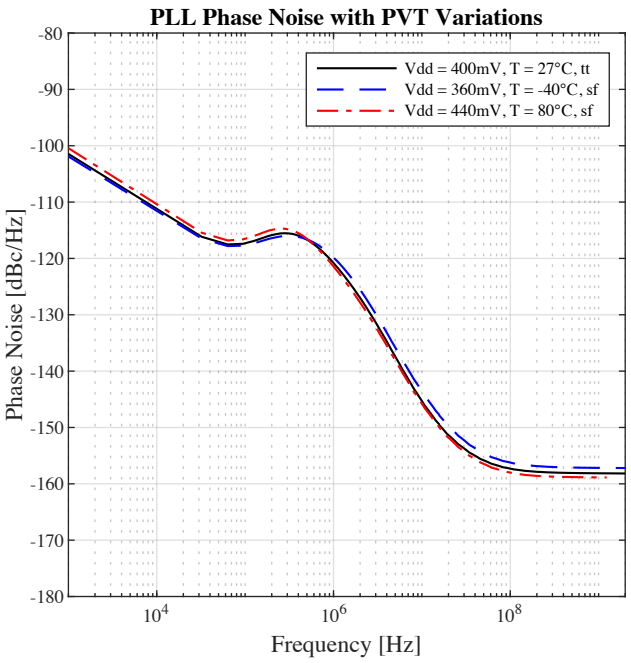


Fig. 16: Total noise at different PVT corners

As we can see in Fig. 16, there is quite some noise deviation between the different corners.

| $K_{VCO}$ Corner | Total Jitter | $FoM_{PLL}$ |
|---|---|---|
| Nominal | 79.2 fs | -257.40 dBc/Hz |
| High | 81.3 fs | -258.65 dBc/Hz |
| Low | 81.21 fs | -256.44 dBc/Hz |

TABLE III: Total Noise of PLL w.r.t. to PVT variations

## VII. Conclusion

This paper has presented a simple Type-II PLL design with a Class-D VCO [1]. The simulations have shown reasonable performance under all corner cases of interest and a decent FoM. Further improvements include increasing the tuning range of the VCO for a broader, which could entail adding coarse tuning, along with looking into more varactor topologies in order to tailor the tuning range even further than this present work does.

## VIII. Appendix

### A. Inverted Varactors

Instead of connecting $V_{cont}$ to the gates of the two transistors, the transistors can be "turned around", and by connecting $V_{cont}$ to their bulk (drain, source and body) and connecting the gate to the differential outputs (see Fig. 17) achieving a different frequency operating range.

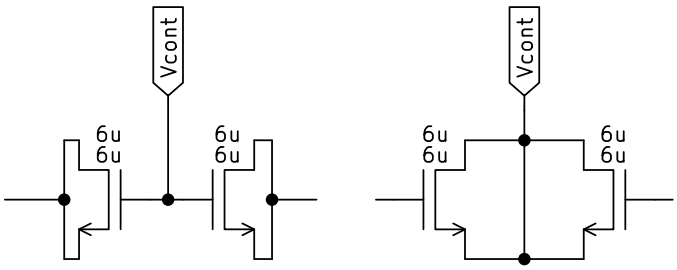


Fig. 17: Two different varactor topologies.
Left: MOSFETs with $V_{cont}$ wired to the common gates.
Right: MOSFETs with $V_{cont}$ wired to the common bulks.

Now by examining the tuning range of the VCO in Fig. 18, we can see substantial differences between the two varactor placements.

As we can see in Fig. 18, the voltage range of the control voltage is severely reduced compared to the varactor structure used in the current design. We can also see that in order to ensure closed loop stability of the PLL, the control range of $V_{cont}$ must be meticulously chosen in order not to introduce a negative $K_{VCO}$ in the control loop.

### B. TSPC

The True Single-Phase Clocking (TSPC) divide by 2 based circuit is shown in figure 19. It is a positive-edge triggered D-flip-flop with TSPC logic [3] which inverted output is tied to the D input.

We perform an analysis of the circuit to understand its functionality. We will initially assume that Q and CLK are 0. Node A and B will both be 1 and Q output will not change. On a rising edge of CLK, A will be floating. Node B will be

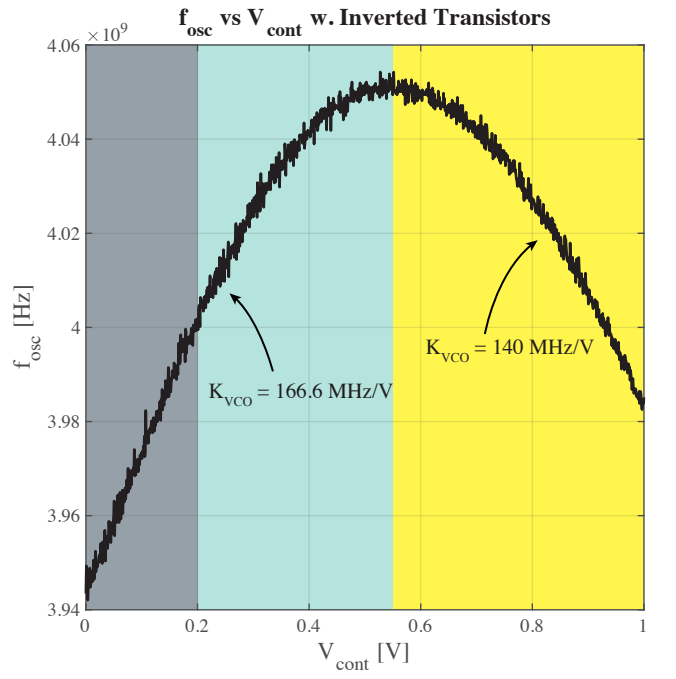


Fig. 18: Frequency behaviour of inverted varactors in the current VCO design.

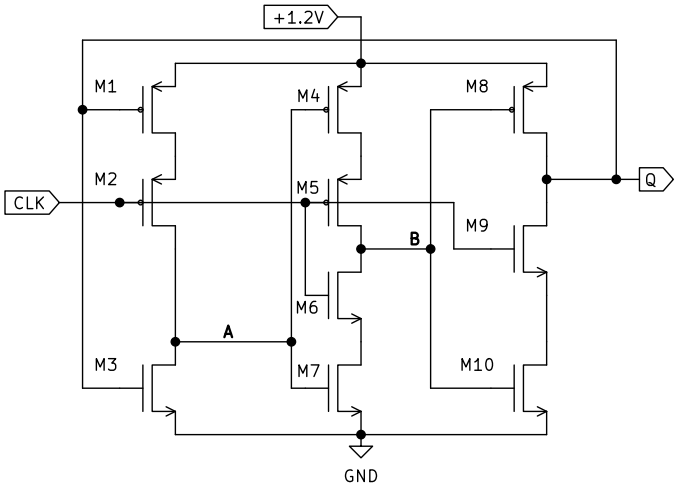


Fig. 19: True Single-Phase Clocking (TSPC) used as a frequency divider

pulled to 0 which raises Q to 1. This change of output has no retroactive effect on the current state.

Now that Q is high, when CLK goes low the node A will have the logic value 0 and B will be floating, keeping the charge from last state, so the output stays constant. Finally, on a rising edge of CLK, node A will still be 0 and B still has the last state of 0. This pulls the Q output to 0, which effectively halves the clock period. This topology achieves relatively high speeds with low power dissipation.

## References

[1] Luca Fanori and Pietro Andreani. "Class-D CMOS Oscillators". In: *IEEE Journal of Solid-State Circuits* 48.12 (Dec. 2013). Conference Name: IEEE Journal of Solid-State Circuits, pp. 3105–3119. ISSN: 1558-173X. DOI: 10.1109/JSSC.2013.2271531.

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