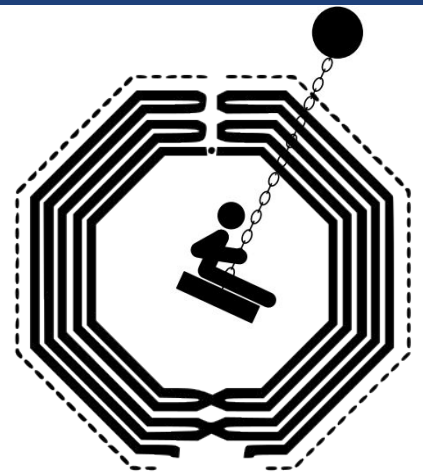
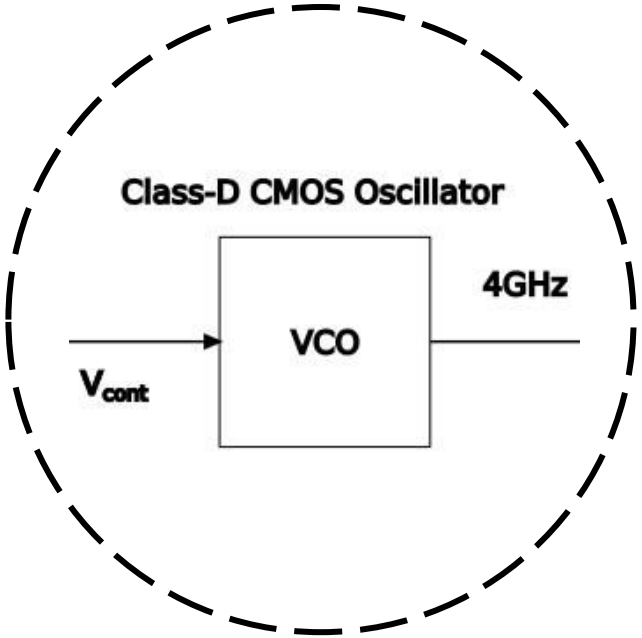


PLL based on a Class-D CMOS Oscillator

Xi Chen, Kyuik Cho, Garðar Eðvaldsson, Marwan Abdelaziz Ibrahim, Guillaume Thivolet

The paper introduced a novel Class-D CMOS Oscillator



Class-D CMOS Oscillators

Luca Fanori and Pietro Andreani

***Abstract*—This paper presents class-D CMOS oscillators capable of an excellent phase noise performance from a very low power supply voltage. Starting from the recognition of the time-variant nature of the class-D *LC* tank, accurate expressions of the oscillation frequency, oscillation amplitude, current consumption, phase noise, and figure-of-merit (FoM) have been derived. Compared with the commonly used class-B/C architectures, the optimal class-D oscillator produces less phase noise for the same power consumption, at the expense of a higher power supply pushing. A prototype of a class-D voltage-controlled oscillator (VCO) targeted for mobile applications, implemented in a standard 65-nm CMOS process, covers a 46% tuning range between 3.0 and 4.8 GHz; drawing 10 mA from 0.4 V, the phase noise at 10-MHz offset from 4.8 GHz is –143.5 dBc/Hz, for an FoM of 191 dBc/Hz with less than 1-dB variation across the tuning range. A version of the same VCO with a resonant tail filter displays a lower $1/f^3$ phase-noise corner and improves the FoM by 1 dB.**

***Index Terms*—Class-D, CMOS, high efficiency, low phase noise, low-voltage, voltage-controlled oscillator (VCO).**

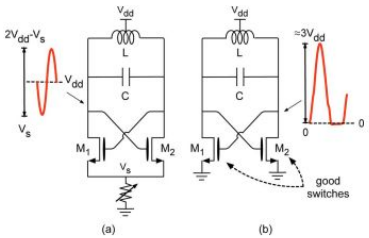


Fig. 1. (a) Class-B oscillator with tail resistor. (b) class-D oscillator.

I. Introduction

IT is a widely acknowledged truth of radio IC design that voltage-controlled oscillators (VCOs) in modern multistandard transceivers are major power consumers and, as such, targets of tireless research efforts tending to increase their efficiency without compromising their multifaceted performance.

The steadily dropping maximum tolerable voltage of standard MOS devices in nanometer digital CMOS technologies certainly helps power saving, but exacerbates to an even higher degree the difficulty of obtaining the desired phase-noise performance (especially when this is demanded together with a wide tuning range), since a low phase noise is largely dependent on a high oscillation amplitude, which is naturally limited by the available supply voltage V_{dd}.

The traditional class-B VCO shown in Fig. 1(a) exhibits a maximum voltage swing limited by the voltage drop V_s across a tail resistor (or, equivalently, across a tail nMOS current source), which is typically required to limit the current drawn from the power supply. The resulting maximum oscillation amplitude (peak, single-ended) is equal to $V_{dd} - V_s$, which, for a low supply voltage, may prove insufficient to guarantee the desired phase noise level demanded by mobile communications standards, at least when reasonable values for the inductance and capacitance in the VCO core are assumed.

Following the demand for a low V_{dd}, Okada *et al.* [1] combine class-C operation [2] with an extremely low V_{dd}, accepting a phase-noise performance that is unsuitable for mobile communications. More recently, Li *et al.* have proposed a remarkable VCO [3] (refining the transformer-based design by Bevilacqua *et al.* [4], [5]) requiring only 0.6 V of V_{dd} and covering an extremely wide tuning range with an excellent phase noise performance and figure-of-merit (FoM).

The oscillator to be here described resorts to the class-D topology [6], shown in Fig. 1(b), which makes it possible to combine low phase noise, low supply voltage and high efficiency simply by increasing the size of the cross-coupled MOS switches of the traditional class-B VCO, removing at the same time the current control circuitry. This maximizes the oscillation amplitude, which reaches a peak of approximately $3V_{dd}$, and improves the power efficiency to beyond 90%, since the product of drain voltage and channel current in the MOS switches is very close to zero across the whole oscillation period, with the result that all power dissipation occurs in the LC tank of the VCO.[1] The relatively very high oscillation amplitude benefits the phase noise and makes the class-D topology suitable for very low-voltage applications. Moreover, the class-D architecture offers the great advantage of an unsurpassed design simplicity: apart from the obvious *LC* tank, it requires only two excellent switches (M_1/M_2), whose performance enjoys all of the advantages attending device scaling in current and future CMOS technologies and disposes of any current-bias circuitry, typically needed in class-B/C VCOs, which affects the dynamic range and contributes to noise as well. The downside of the class-D VCO, on the other

Manuscript received April 05, 2013; revised May 23, 2013; accepted June 24, 2013. Date of publication July 22, 2013; date of current version November 20, 2013. This paper was approved by Guest Editor Hooman Darabi. This work was supported in part by the European Union 7th Framework Programme (FP7/2007-2013) under Grant 248277 and the Swedish Foundation for Strategic Research (SSF) under the DARE Project.

The authors are with the Department of Electrical and Information Technology, Lund University, SE-221 00 Lund, Sweden (e-mail: luca.fanori@eit.lth.se; piero@eit.lth.se, pietro.andreani@eit.lth.se).

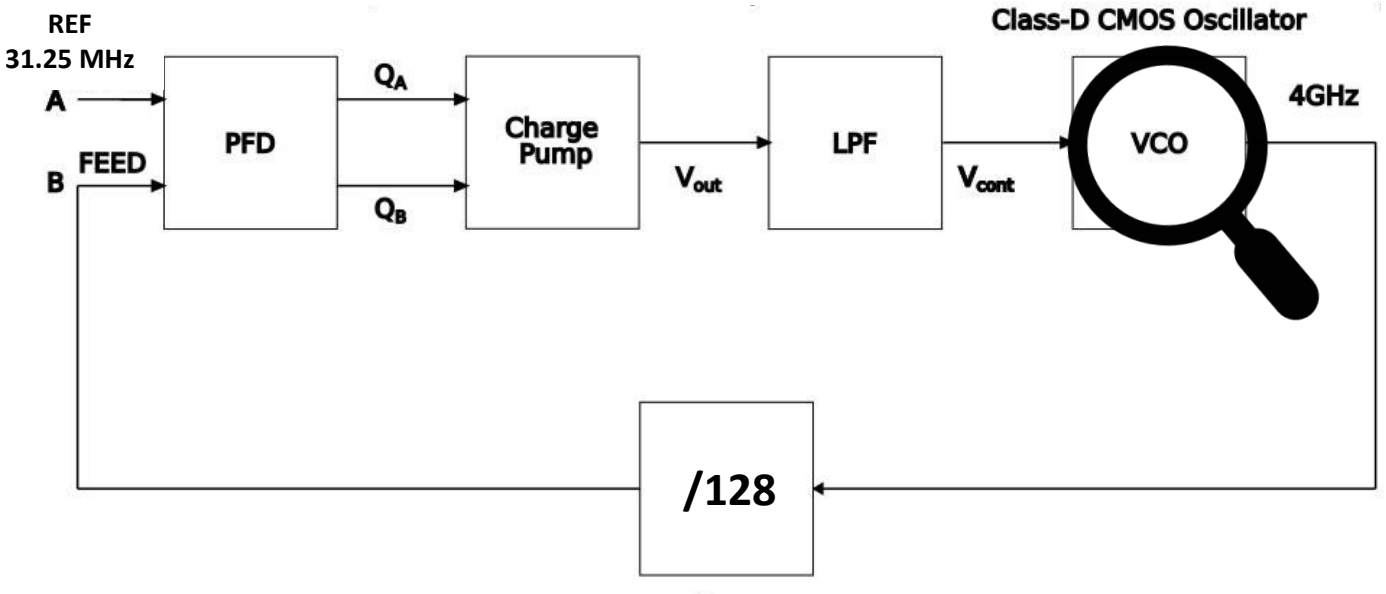
Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2013.2271531

[1]It should be noted, however, that the *LC* tank in the class-D oscillator behaves quite differently from the same in a class-B/C oscillator. This issue is dealt with in detail in the following sections.

Luca Fanori and Pietro Andreani, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 12, DECEMBER 2013

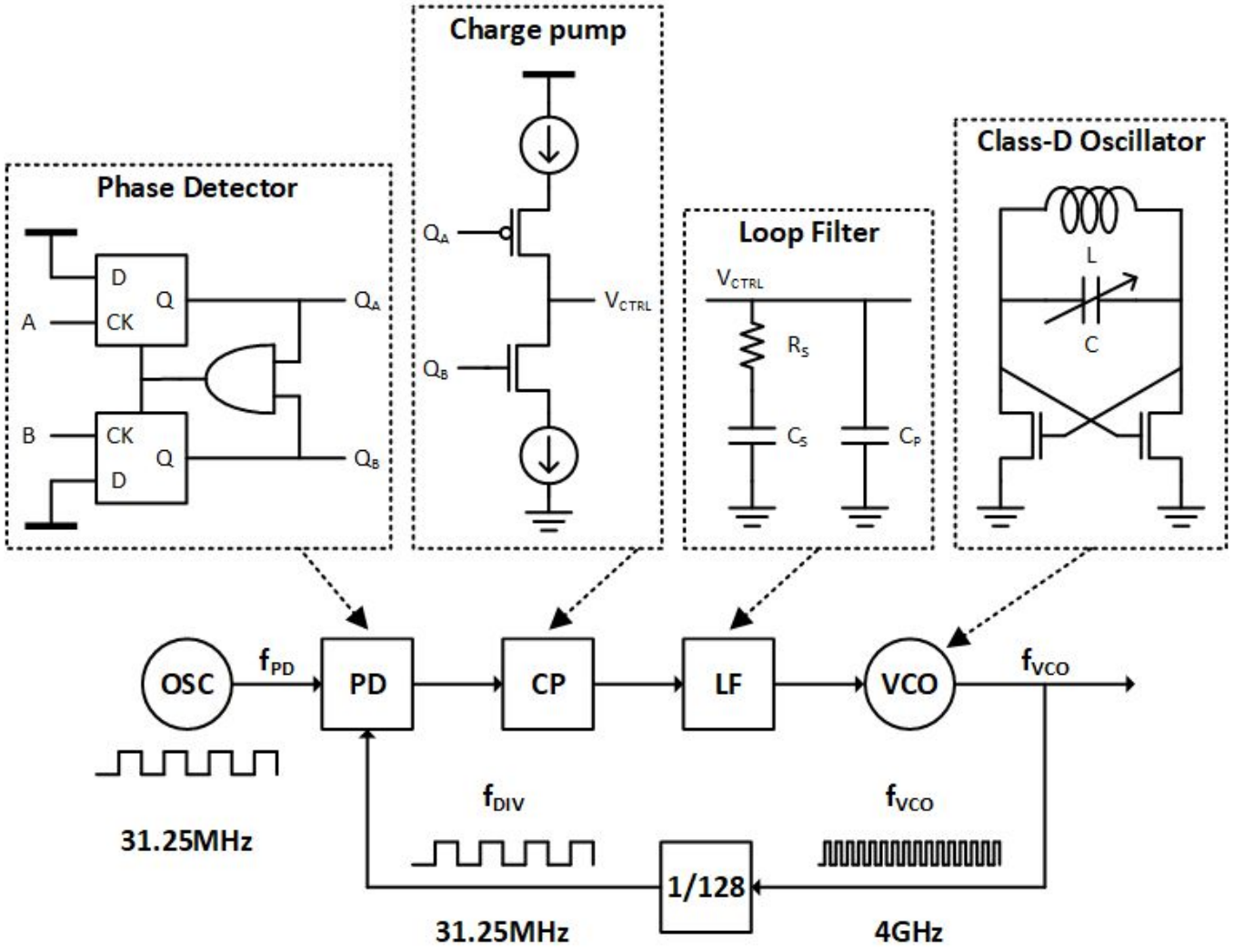
Our goal was to implement the VCO as part of a whole PLL



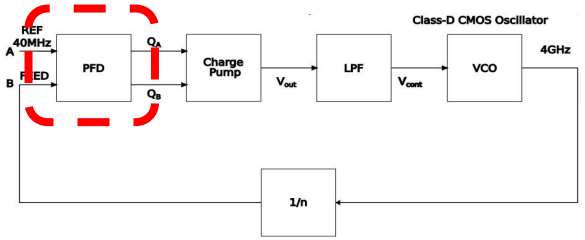
Specifications

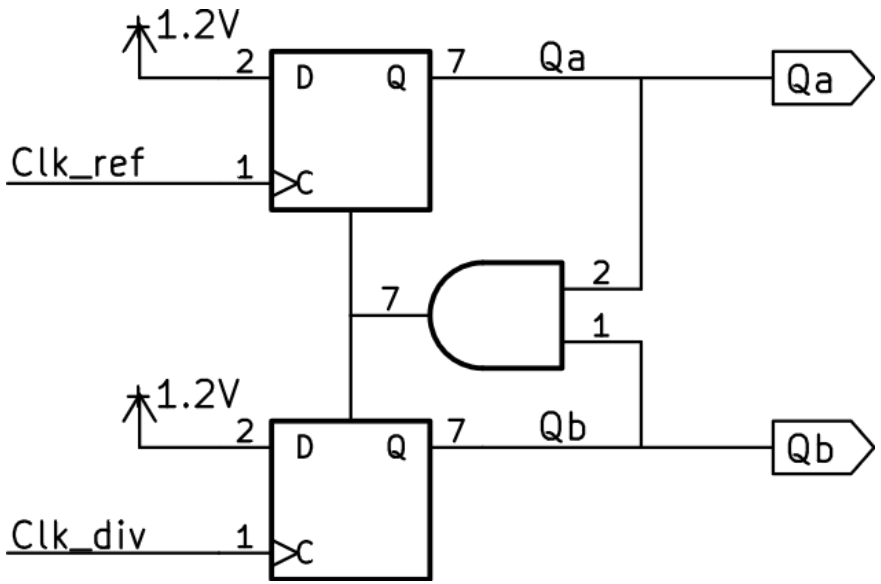
Parameter	Target	Unit
Ref clock	31.25	MHz
Output freq.	4	GHz
Power consumption	< 4	mW
VCO Phase Noise @ 10MHz	< -190	dBc/Hz

PLL – Overview



PLL – PFD Block

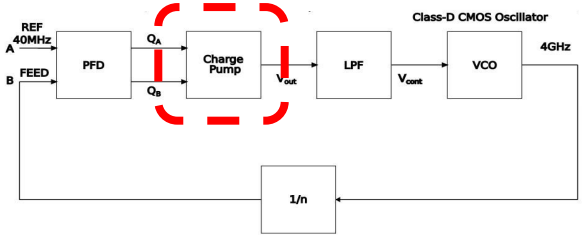


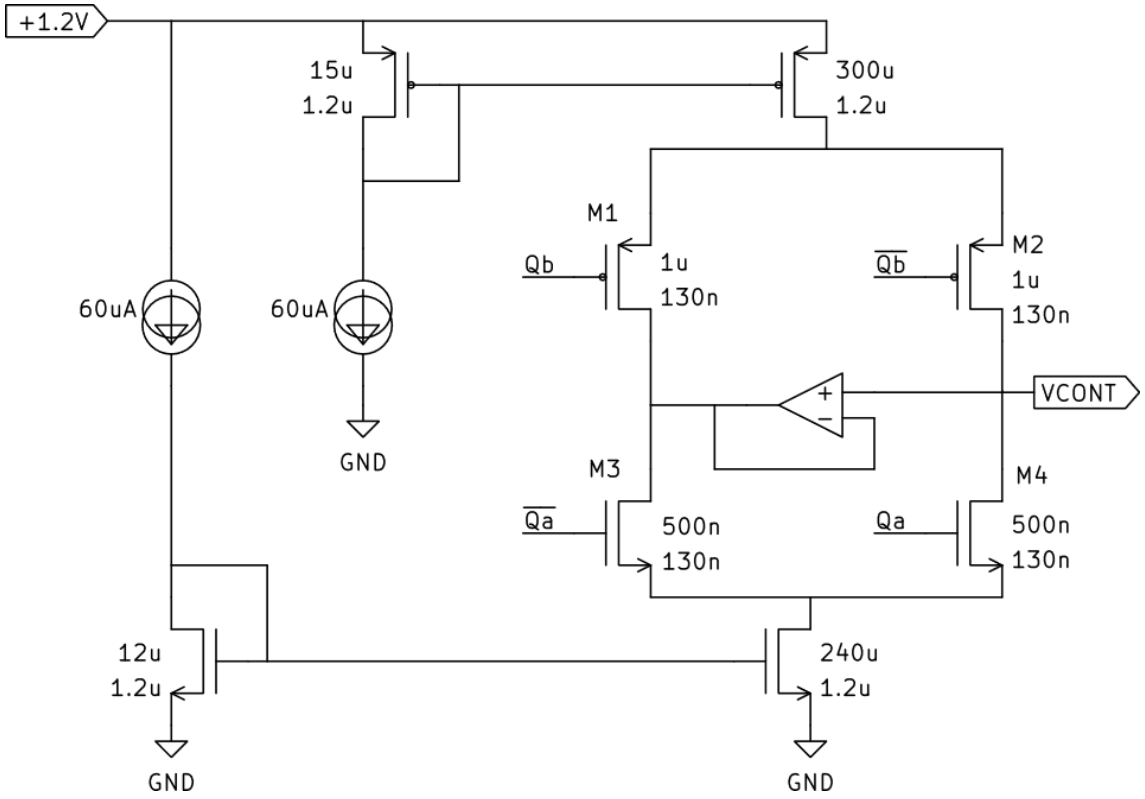


Phase Frequency Detector

- Generate control signals for the charge pump
- Two DFFs with their D input tied to +VDD, one clocked by the stable reference clock CLK_ref (31.25MHz) and the other by CLK_div (feedback from the VCO)

PLL – Charge Pump Block





Current Steering Topology

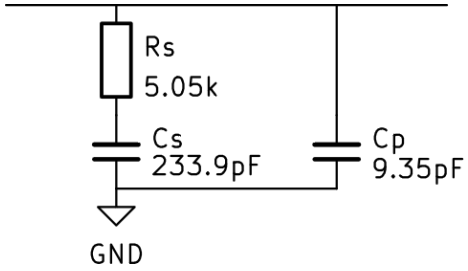
- I_{cp} = 1.2mA
- P_{cp} = 1.9mW

- Role: increasing and decreasing Vcont for the VCO

Challenges

- Current matching for Qa and Qb, and minimize switching charge sharing with the dummy branch

PLL – 2nd order LPF



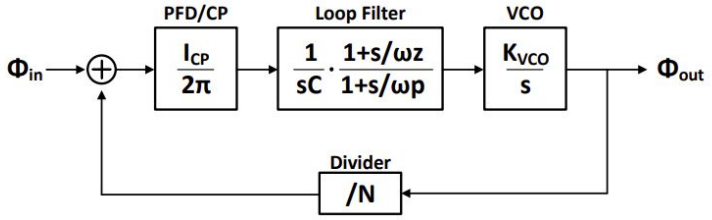
- Role of Rs is to provide loop stability
- Cp for charge sharing

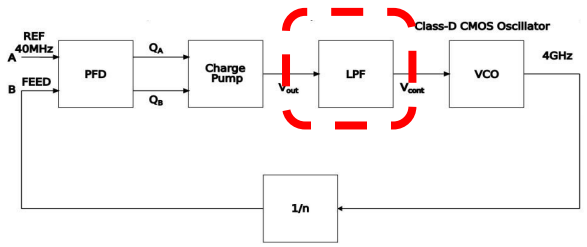
$$\omega_n = \sqrt{\frac{I_{cp}C_s}{2\pi}\frac{K_{VCO}}{N}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{cp}}{2\pi C_s}\frac{K_{VCO}}{N}}$$

$$H(s) = \frac{\frac{I_{cp}K_{VCO}}{2\pi C_s}(sRC_s + 1)}{s^2 + \frac{I_{cp}K_{VCO}}{2\pi N}R \cdot s + \frac{I_{CP}K_{VCO}}{2\pi C_s N}}$$

Closed loop transfer function





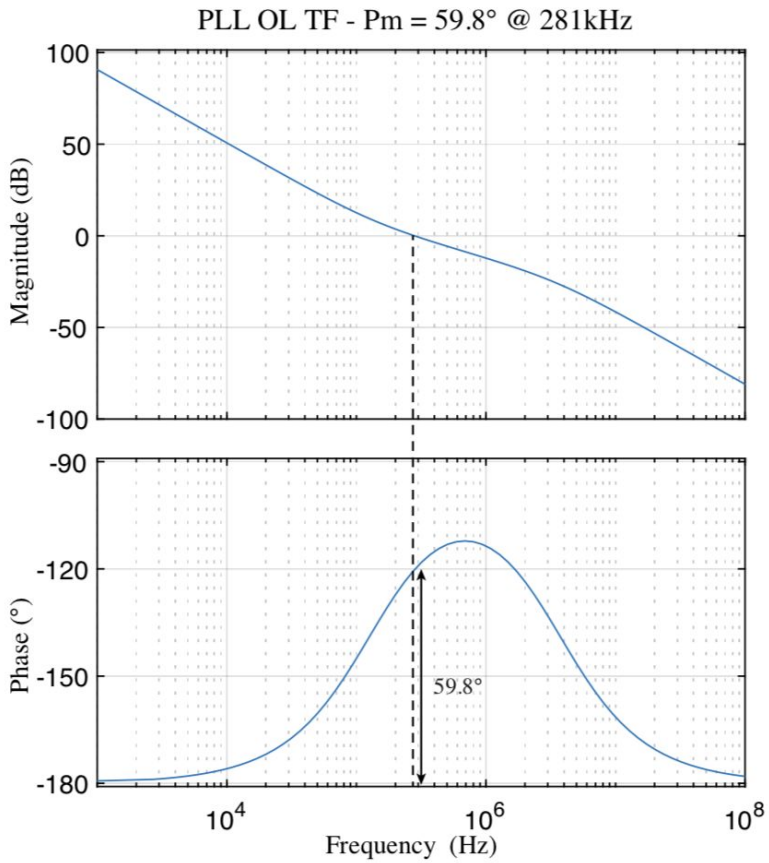
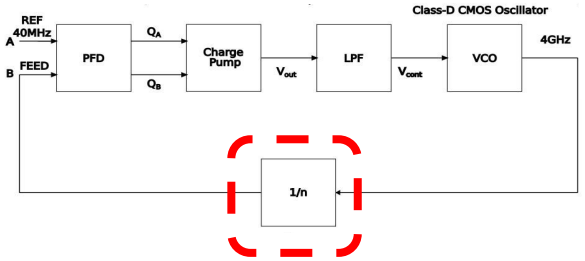
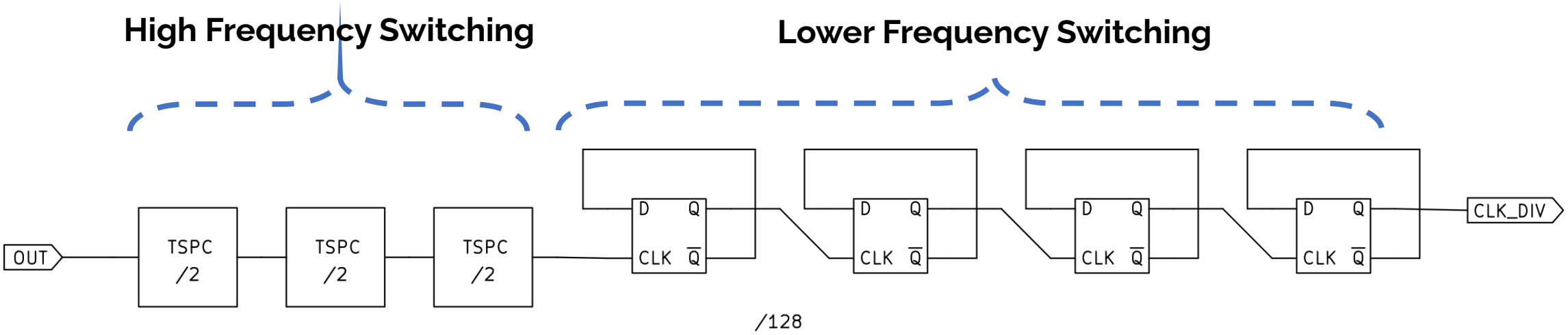


Fig. Open loop transfer function | Amplitude and Phase plots

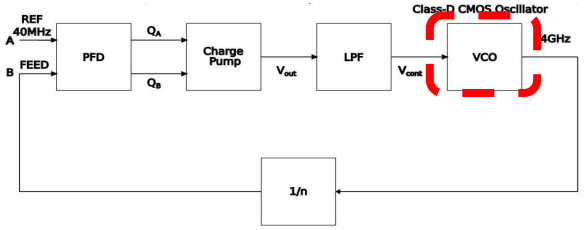
PLL – Frequency Divider





* TSPC available in appendix

Ideal Class-D VCO



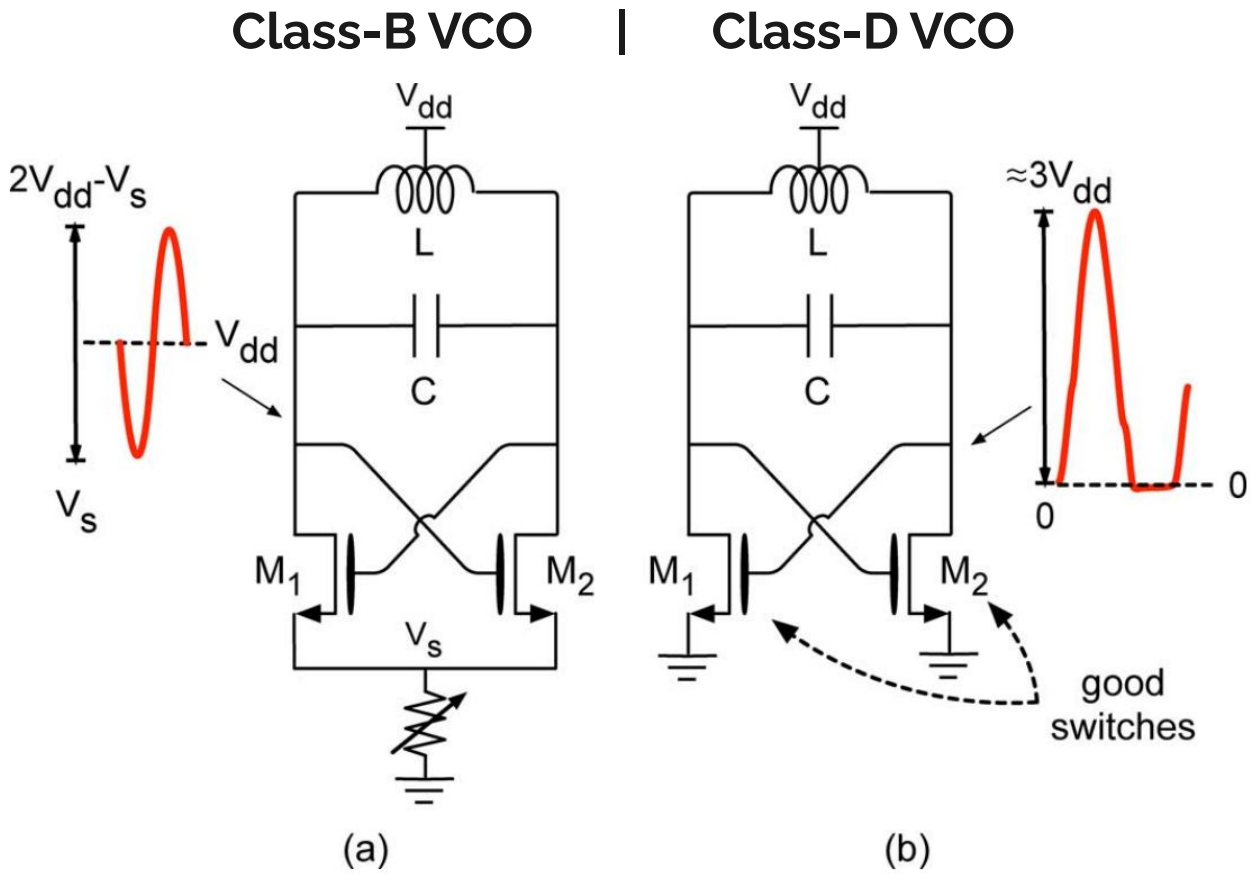


Fig. Class-B (left) and Class-D (right) Oscillator with LC-tank [1]

[1] L. Fanori and P. Andreani, "Class-D CMOS Oscillators," IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3105–3119, Dec. 2013

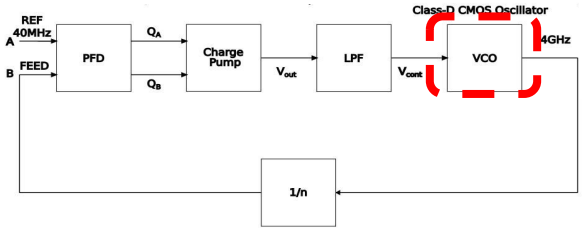
Ideal Class-D VCO

Advantages

- Lower phase noise
- Improved power efficiency
- Design simplicity (no control circuitry for the tail transistor)

Drawbacks

- Asymmetrical oscillation period
- Supply pushing
- Class-D Oscillator design is challenging because of parasitics



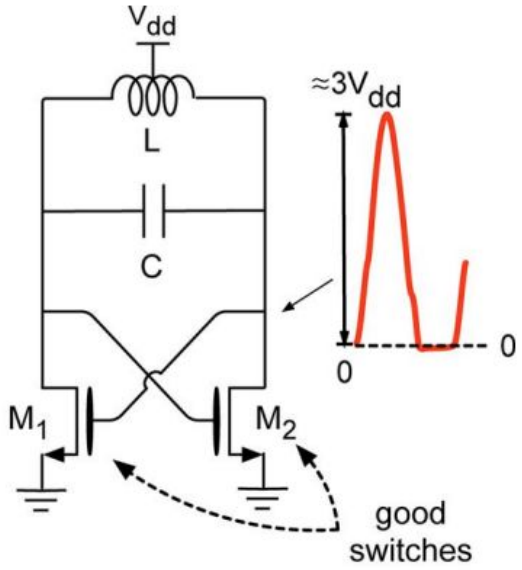
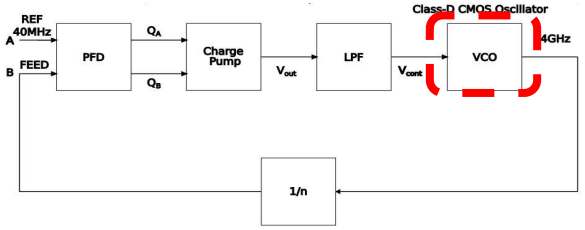
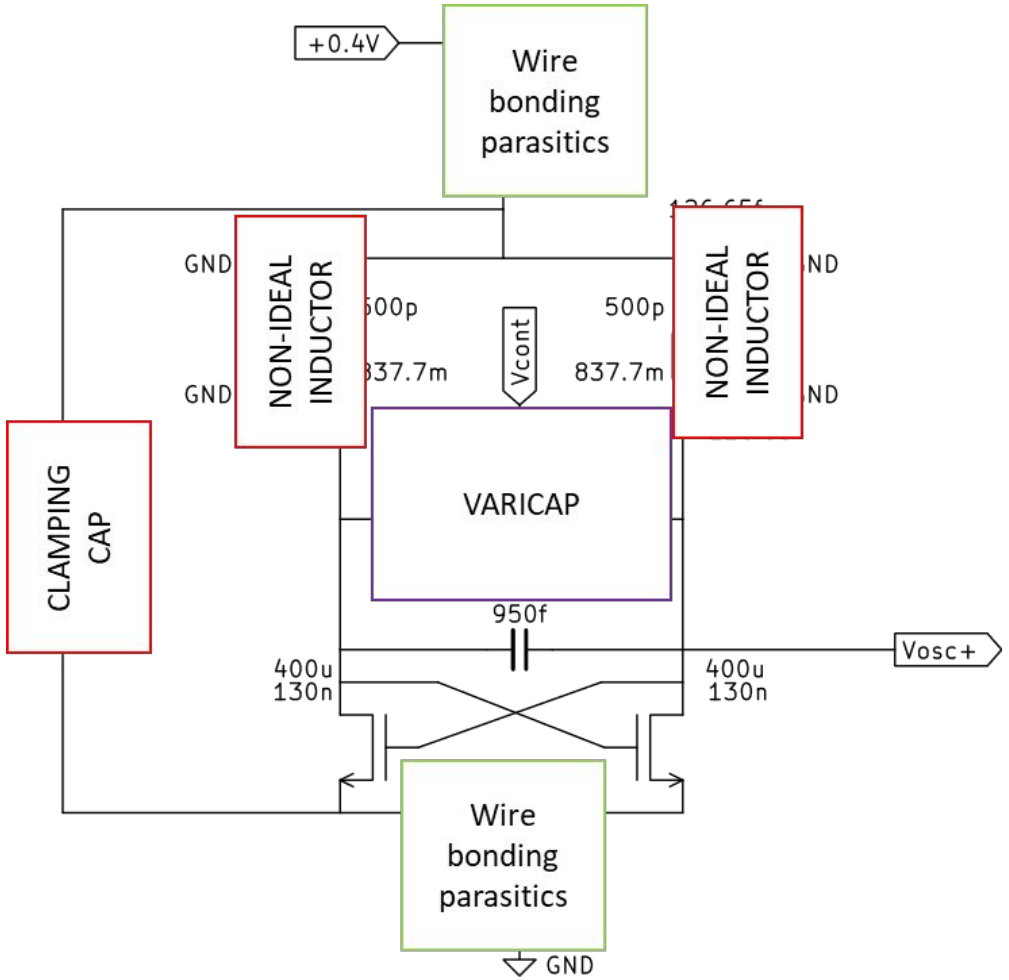


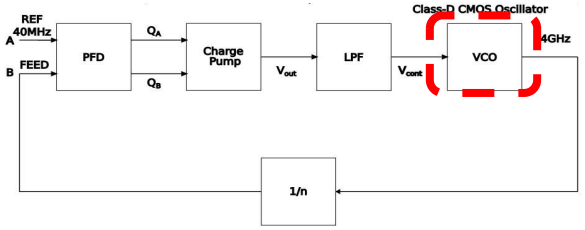
Fig. Class-D Oscillator with LC-tank.

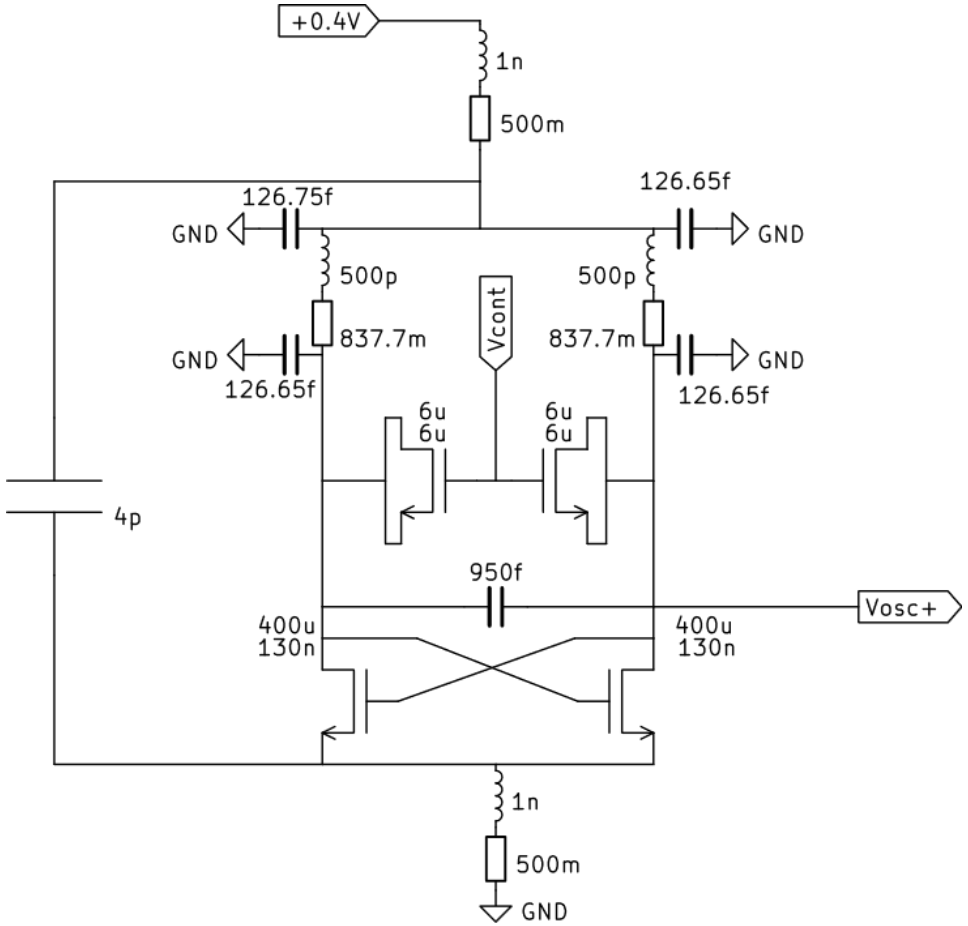
Practical Class-D VCO Schematic



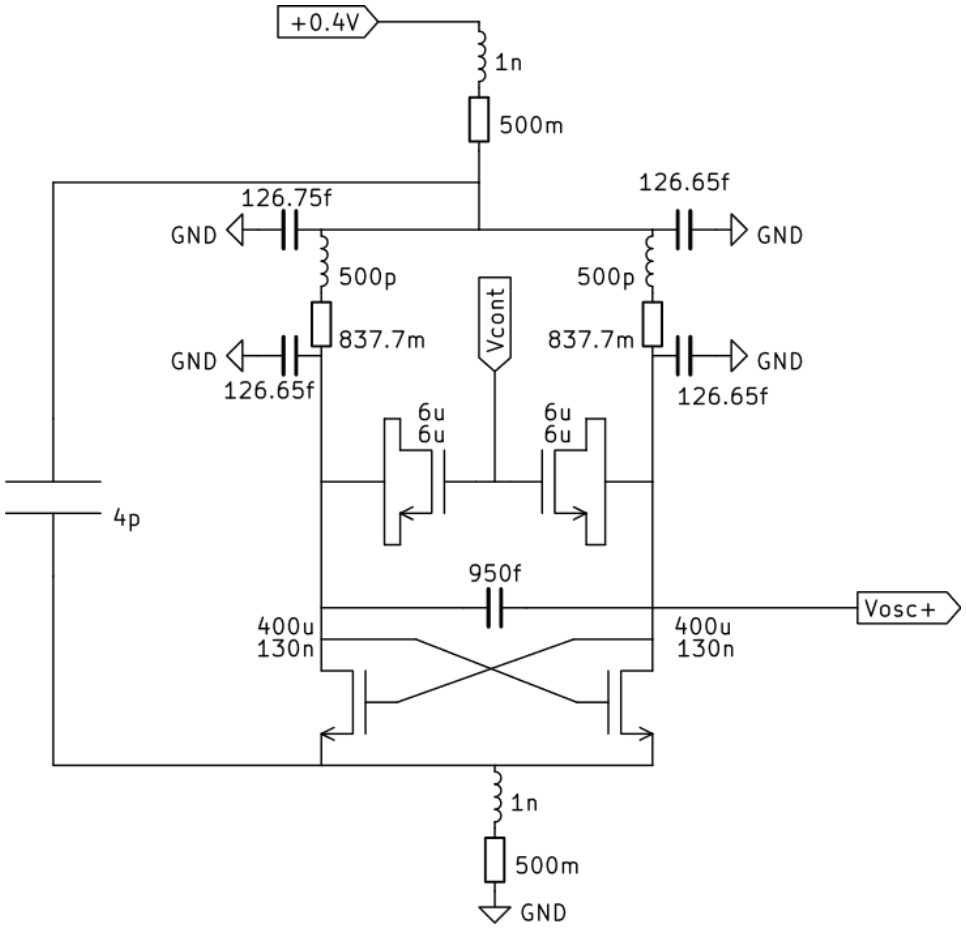


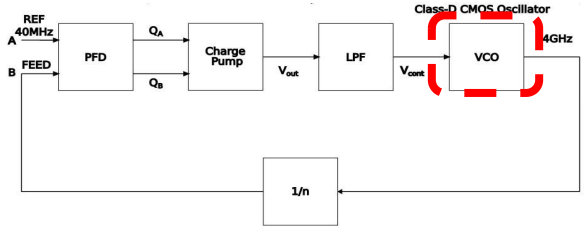
Practical Class-D VCO Schematic

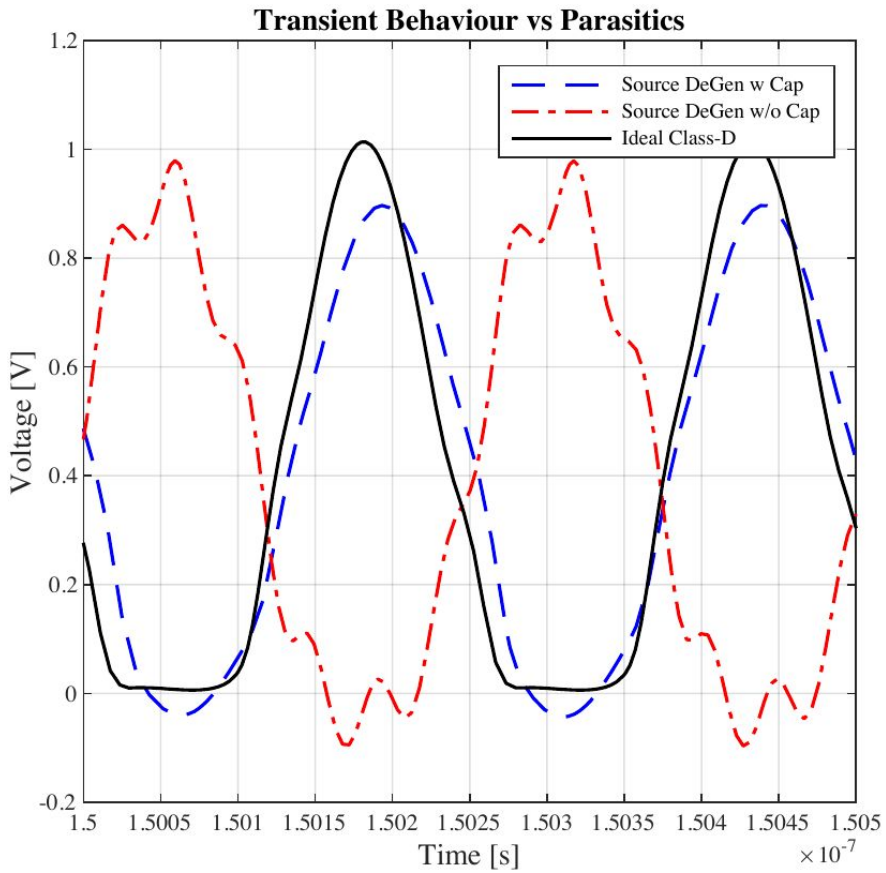




Practical Class-D VCO Schematic

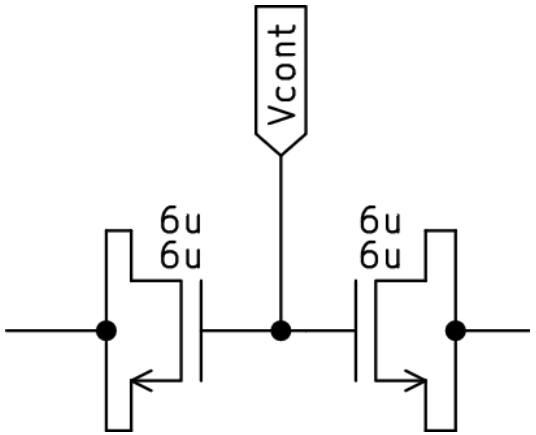


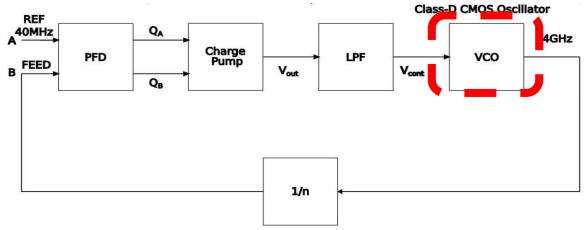


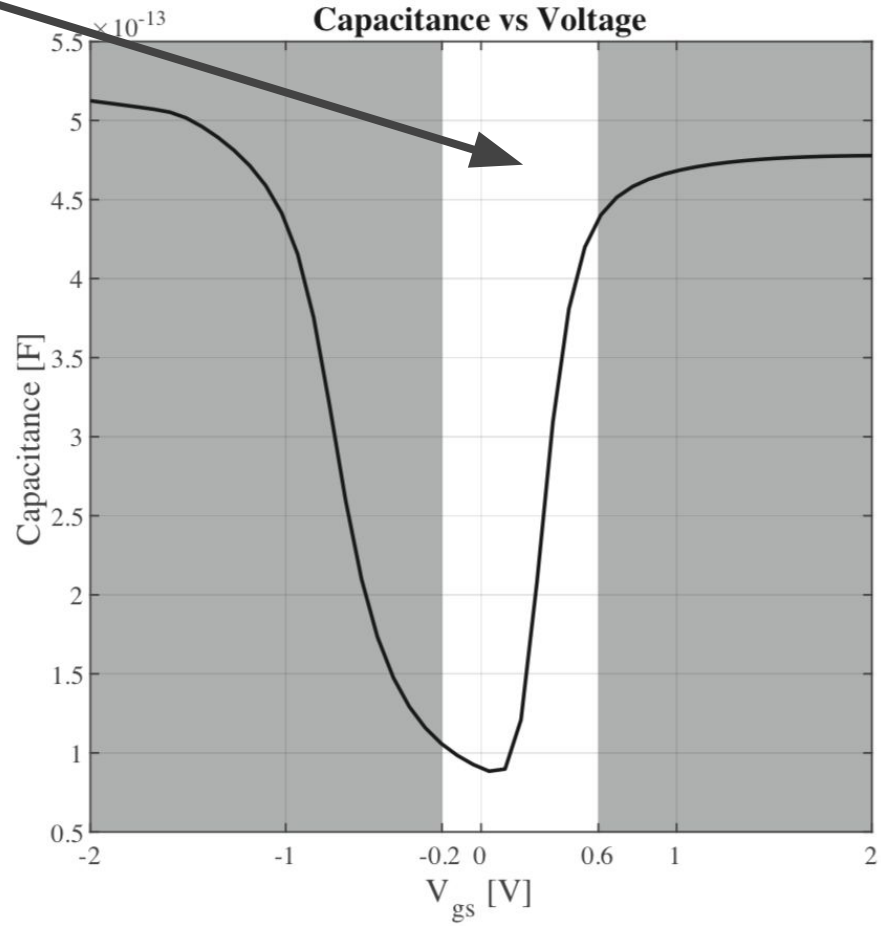


VCO - Varactor

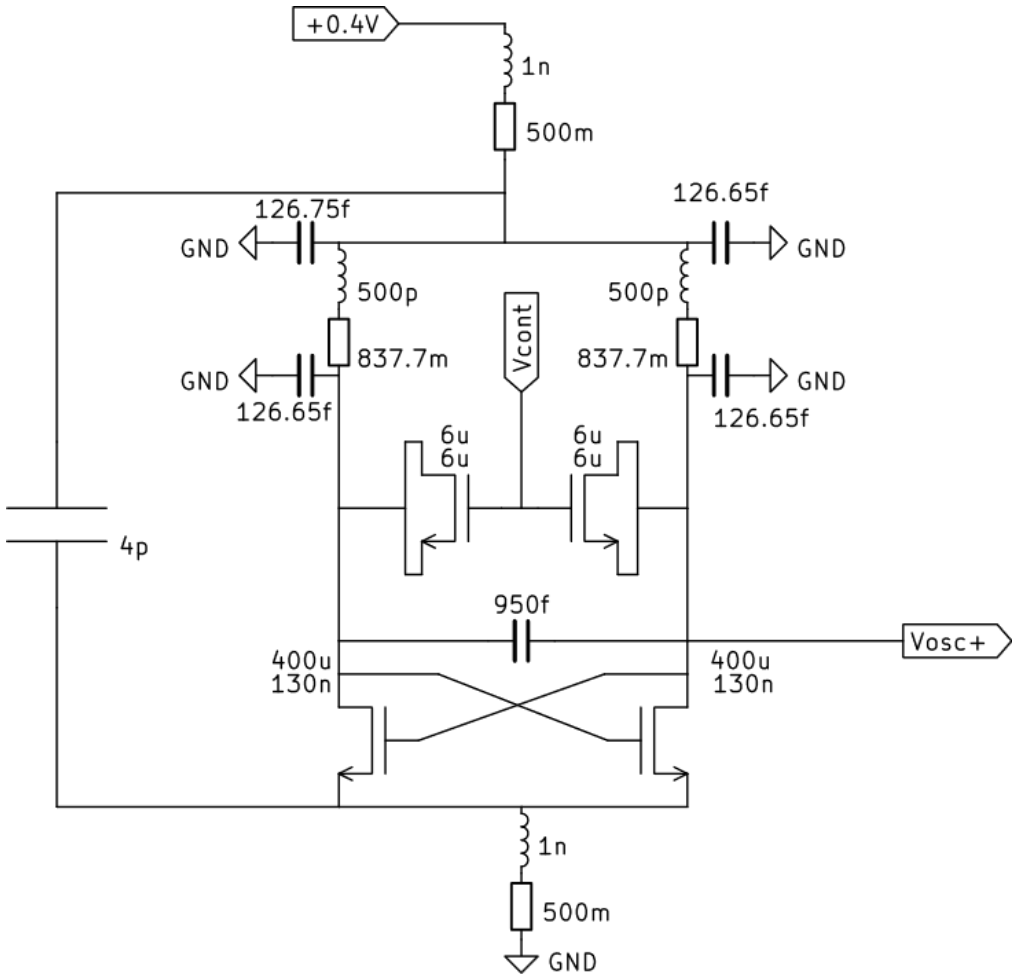
- V_{cont} ranges from [0.2V - 1V]
- +0.4 V_{dc} on bulk side of transistors
- Wide capacitance tuning range

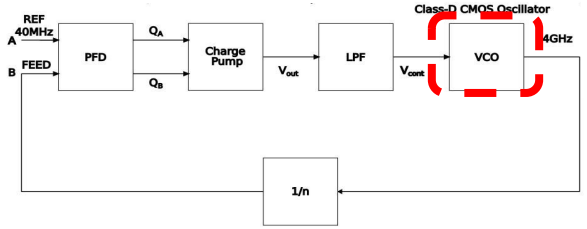


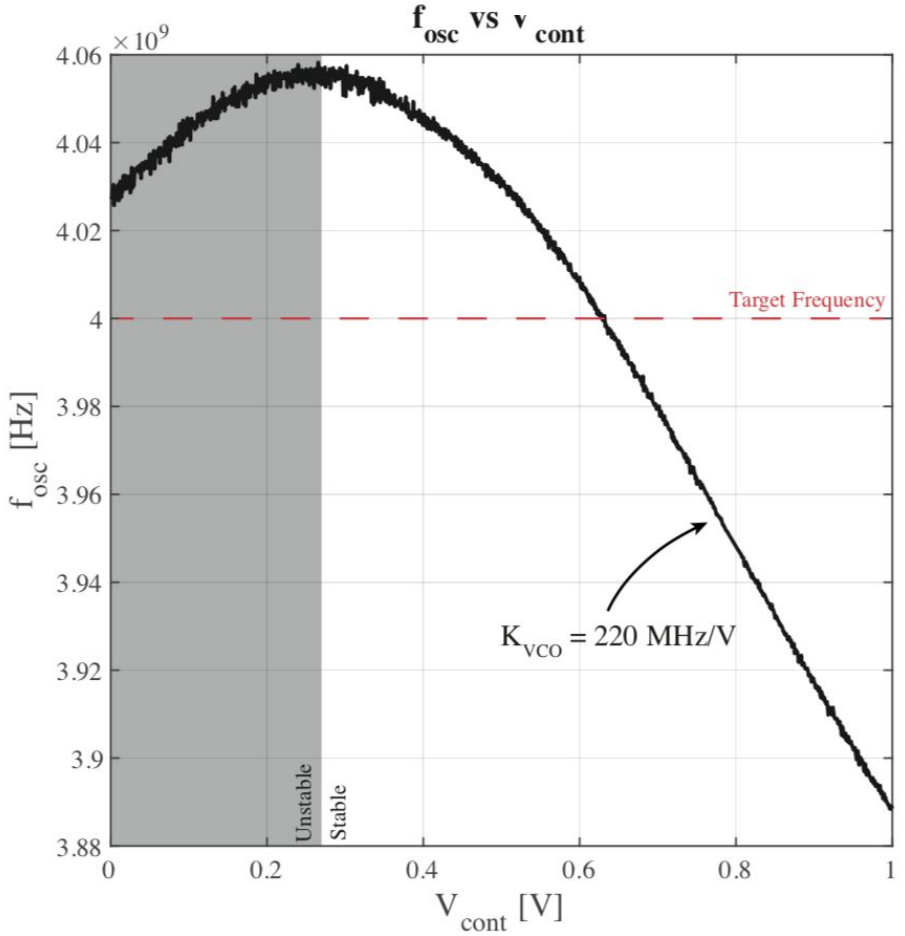




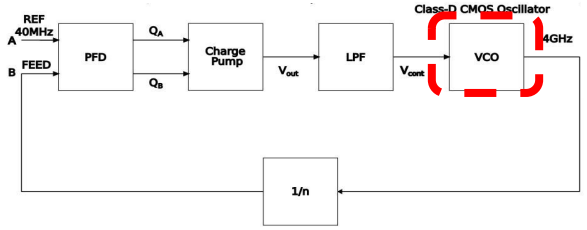
VCO - Varactor

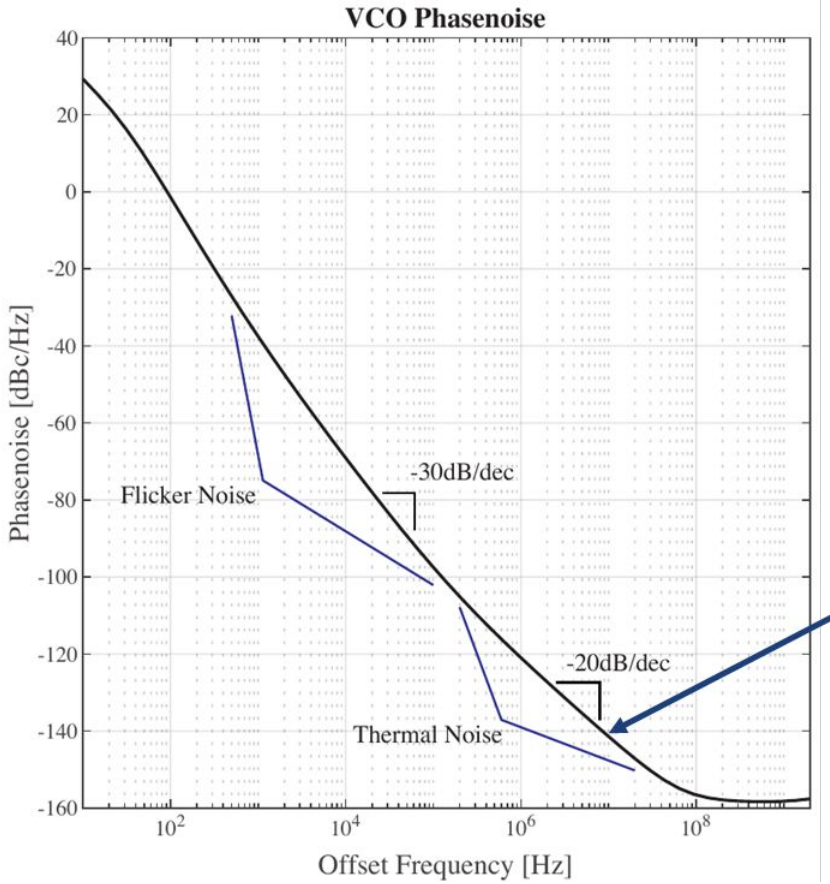






VCO - Figure of Merit





-141.312 at 10MHz

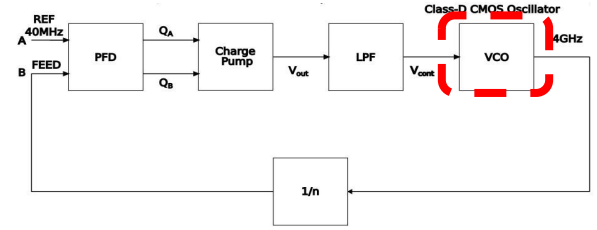
4GHz

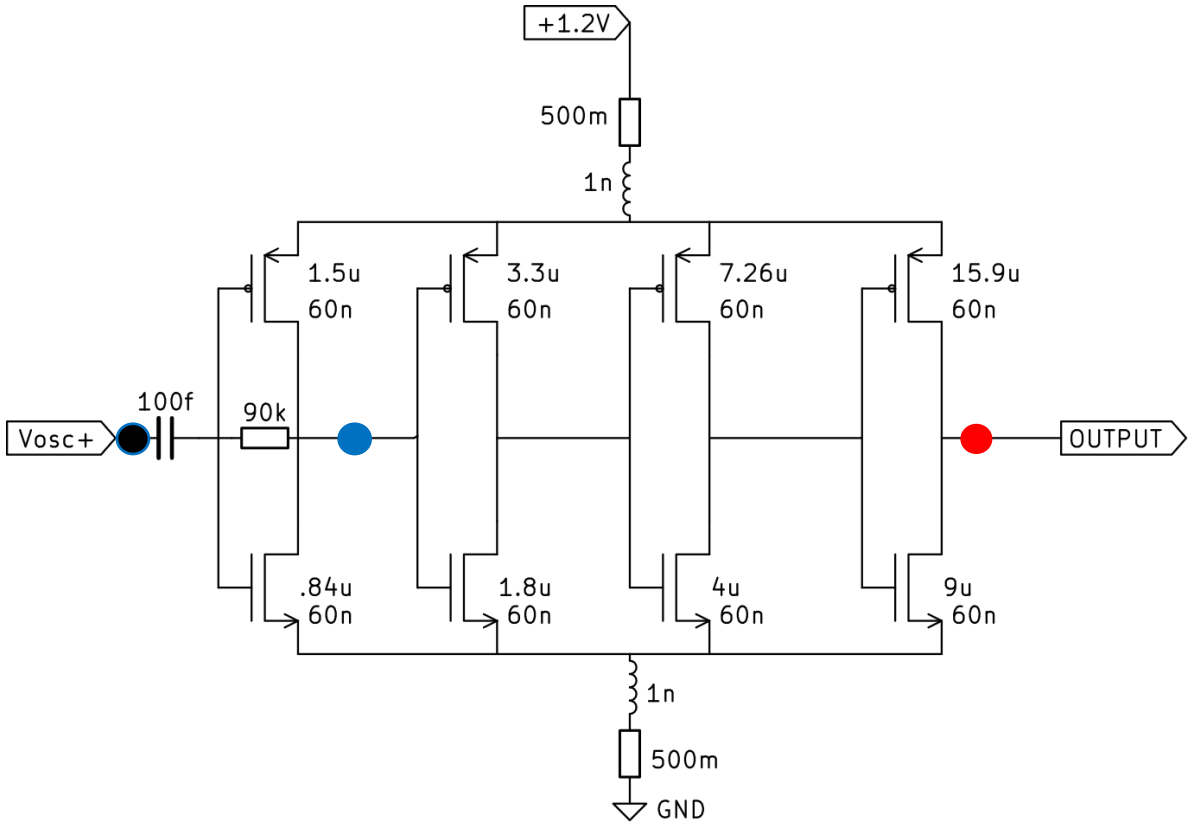
1.947mW

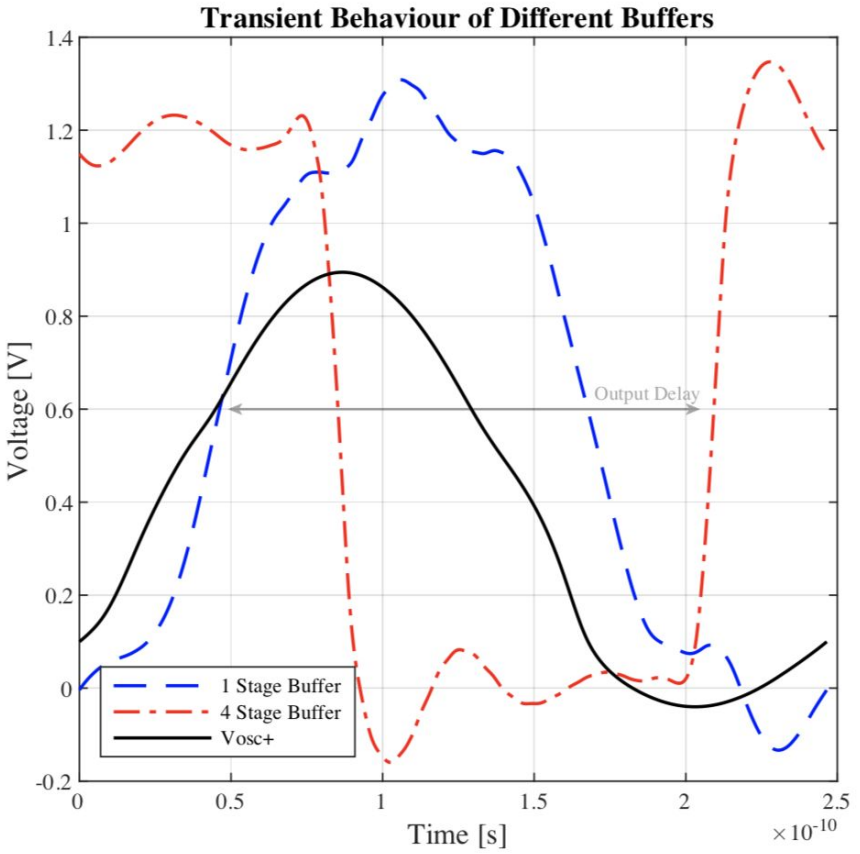
$$\text{FOM} = L(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) = -190.4dBc/Hz$$

10MHz

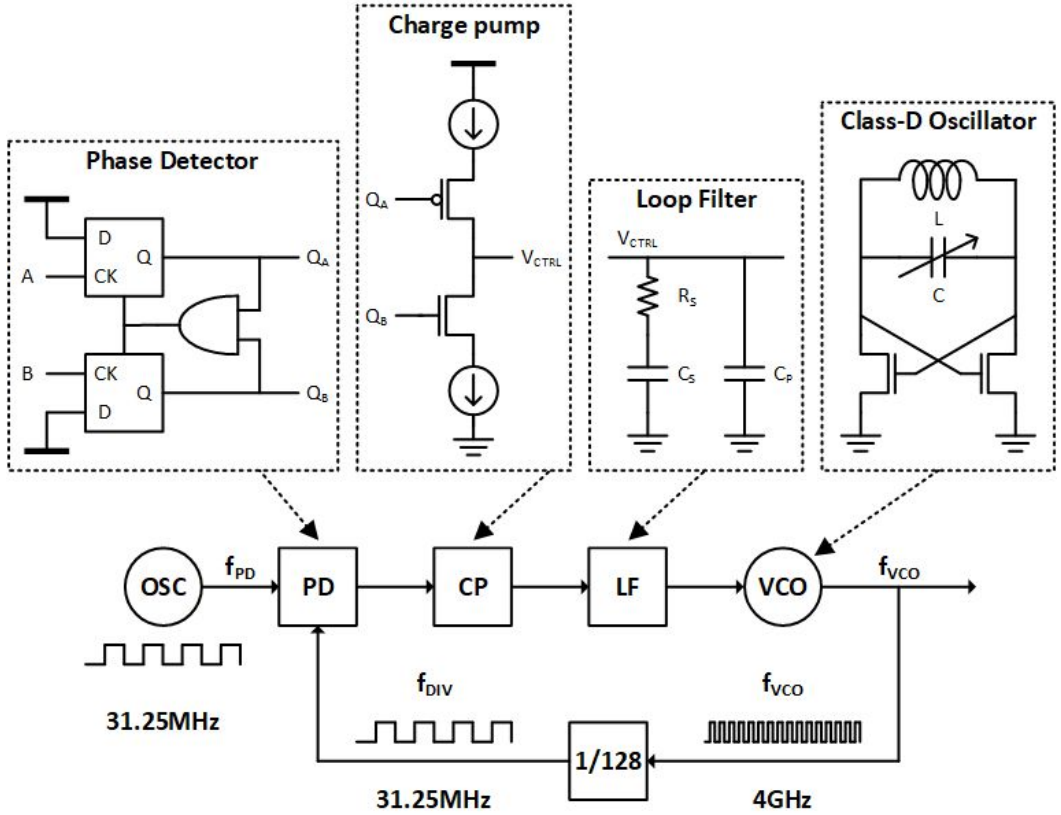
VCO - Output Buffers







PLL - Noise Contributions



$$H(s) = \frac{I_{CP} K_{VCO} (1 + \frac{s}{\omega_z})}{2\pi s^2 (C_S + C_P) N (1 + \frac{s}{\omega_p})}$$

* I_{CP}: $Chargepump\ current\ [A]$
* K_{VCO}: $VCO\ gain\ [Hz/V]$
* N: $Division\ ratio = \frac{F_{DIV}}{F_{VCO}}$
* $\omega_z = \frac{1}{R_S C_S}$
* $\omega_p \approx \frac{1}{R_S C_P}$

To optimize noise, the noise contribution of each building block needs to be accounted for

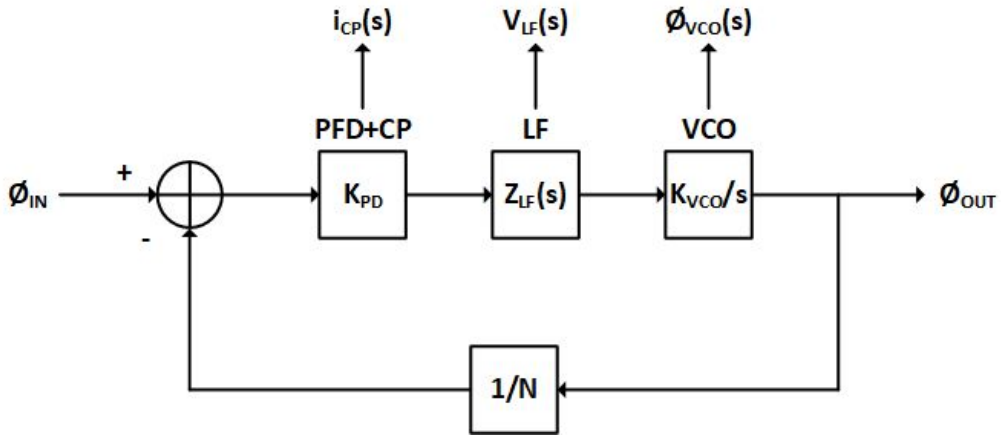
PLL - Noise Contributions

PLL Open Loop Transfer function

$$H_{ol}(s) = \frac{K_{PD} \cdot K_{VCO} \cdot Z_{LF}(s)}{N \cdot s}$$

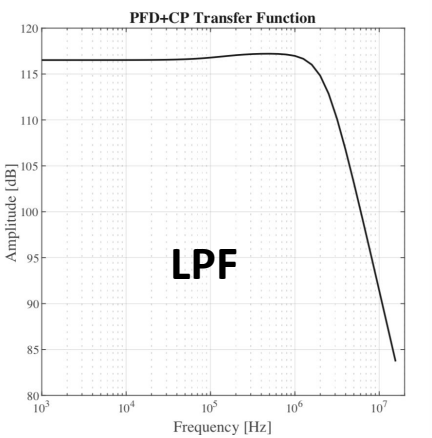
$$* K_{PD}: \frac{I_{CP}}{2\pi}$$

$$* Z_{LF}(s) = \frac{1 + sR_S C_S}{s(C_S + C_P)\left(1 + s\frac{C_S C_P R_S}{C_S + C_P}\right)}$$



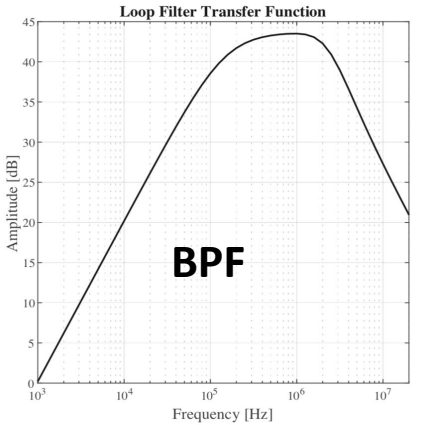
Charge Pump noise transfer function

$$\frac{\emptyset_{OUT}(s)}{i_{CP}(s)} = \frac{N}{K_{PD}} \frac{H_{ol}(s)}{1 + H_{ol}(s)}$$



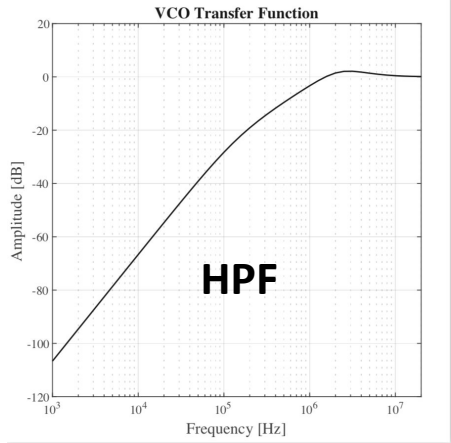
Loop filter noise transfer function

$$\frac{\emptyset_{OUT}(s)}{v_{LF}(s)} = \frac{K_{VCO}}{s} \frac{1}{1 + H_{ol}(s)}$$

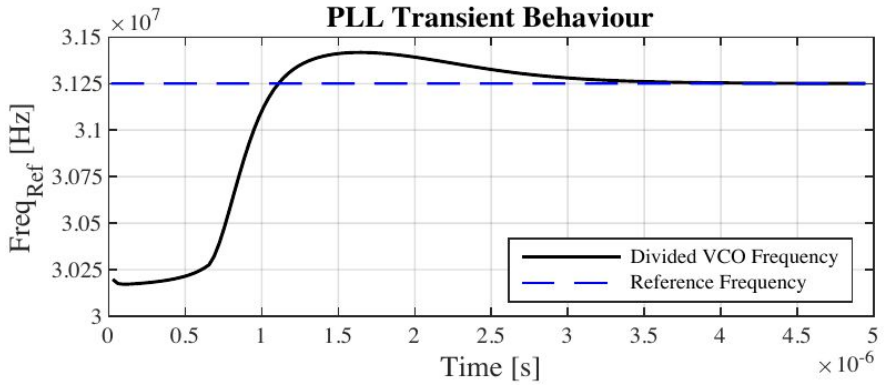


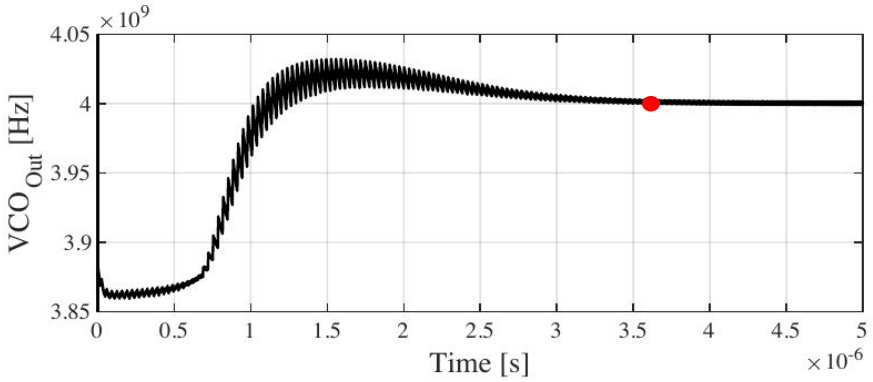
VCO noise transfer function

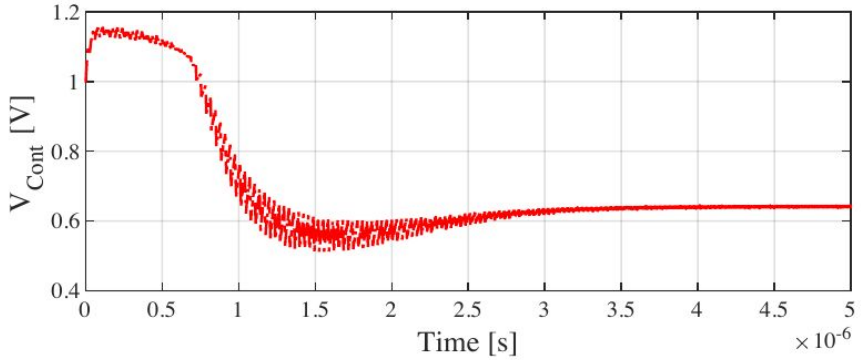
$$\frac{\emptyset_{OUT}(s)}{\emptyset_{VCO}(s)} = \frac{1}{1 + H_{ol}(s)}$$



Results – Transient Simulation I







Key figures

- $\tau_{lock} = 3.7\ \mu s$

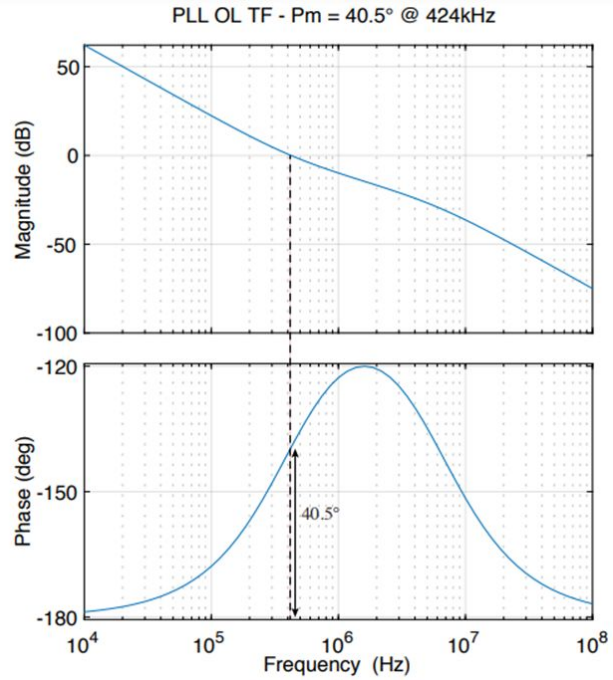
Power consumption

P_{tot} =	2.937mW
VCO	1.937mW
CP+PFD+FD	1mW

Phase margin 40.59°
Open loop BW 420KHz

Parameters

- $I_{cp} = 600\mu A$
- $K_{VCO} = 220\ MHz/V$
- $C_p = 2.33pF$
- $C_s = 30.1pF$
- $R_s = 12.3k$



PLL – Noise Simulation I

Parameters

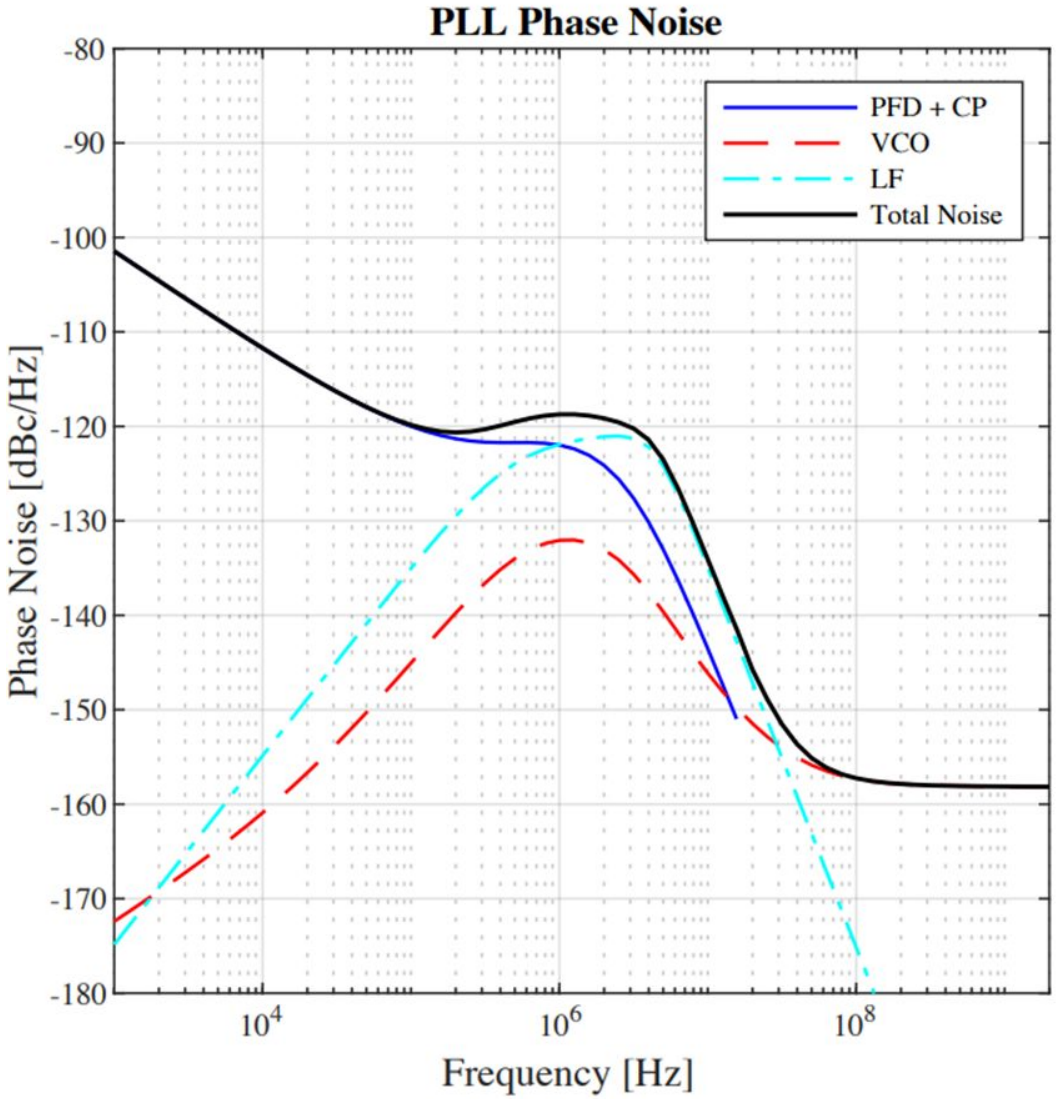
- $I_{cp} = 600\mu A$
- $K_{VCO} = 220\ MHz/V$

- $C_p = 2.33pF$
- $C_s = 30.1pF$
- $R_s = 12.3k$

Results (before optimisation)

- RMS Absolute Jitter $\sigma_a = \frac{1}{\sqrt{2}\pi f_0}\sqrt{\int_{1kHz}^{2GHz} L(f)\,df}$ = 143.16fs

- FoM_{PLL} = $10\log_{10}\left[\frac{\sigma_a^2 \cdot P_{PLL}}{1mW}\right]$ = -250.86 dBc/Hz



PLL – Noise Simulation II

Parameters

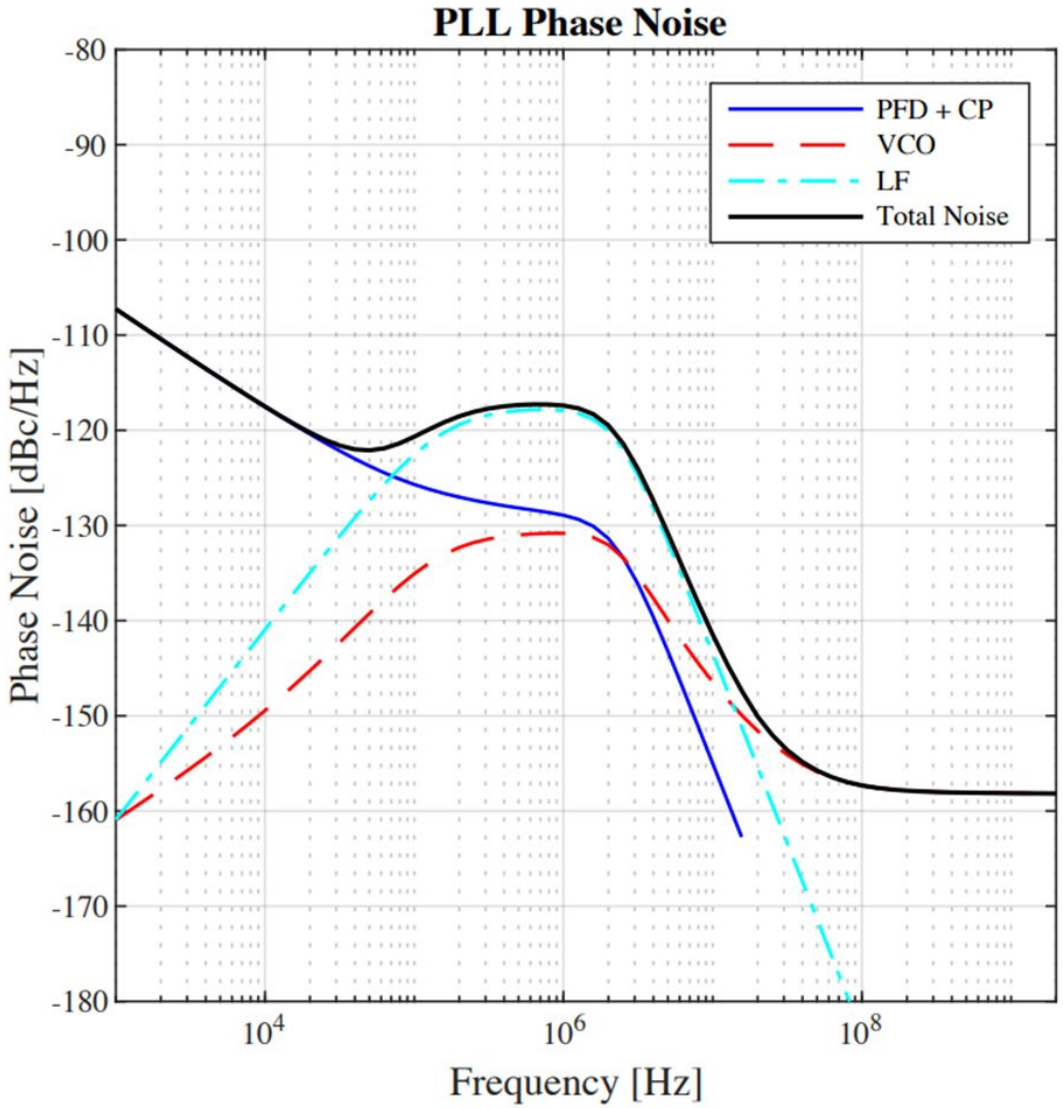
- $I_{cp} = 1.2mA$
- $K_{VCO} = 220\ MHz/V$

- $C_p = 9.35pF$
- $C_s = 233.9pF$
- $R_s = 5.05k$

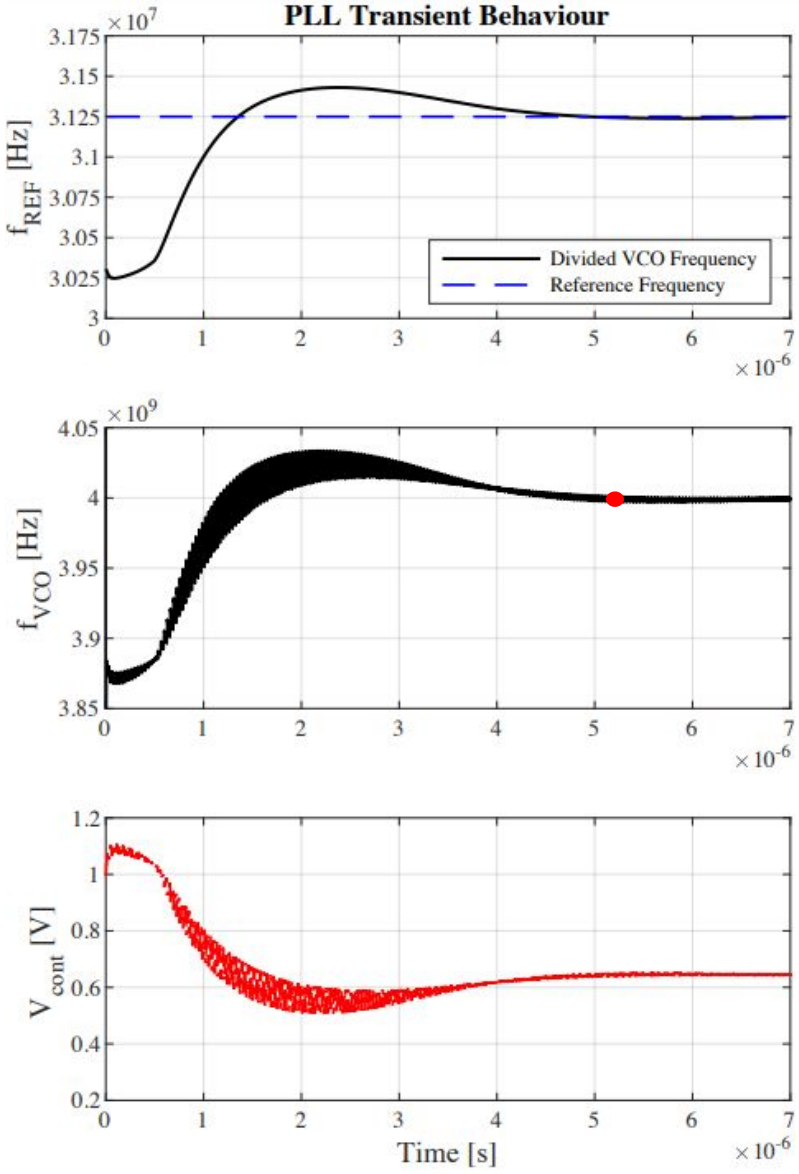
Results (before optimisation)

- RMS Absolute Jitter $\sigma_a = \frac{1}{\sqrt{2}\pi f_0}\sqrt{\int_{1kHz}^{2GHz} L(f)\,df}$ = 124.2fs

- FoM_{PLL} = $10\log_{10}\left[\frac{\sigma_a^2 \cdot P_{PLL}}{1mW}\right]$ = -252.1 dBc/Hz



Results – Transient Simulation II



Key figures

- $\tau_{lock} = 5.05\ \mu s$

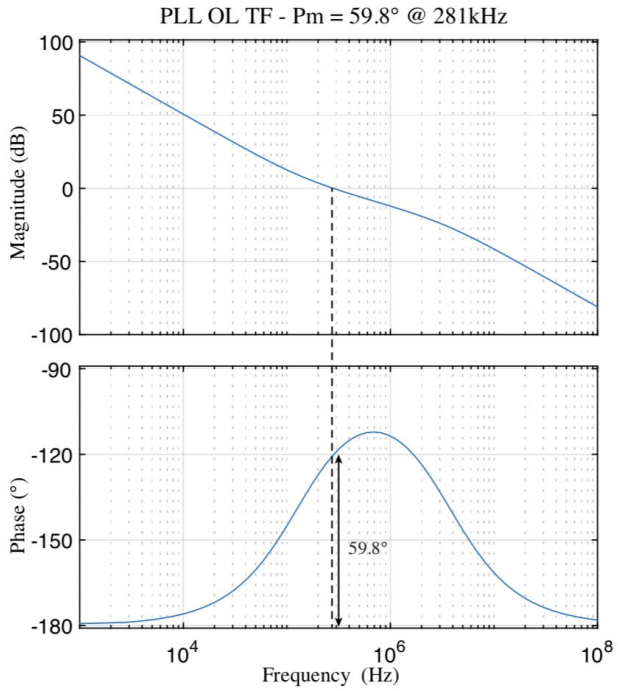
Power consumption

P_{tot} =	3.837mW
VCO	1.937mW
CP+PFD+FD	1.9mW

Phase margin 59.8°
Open loop BW 280KHz

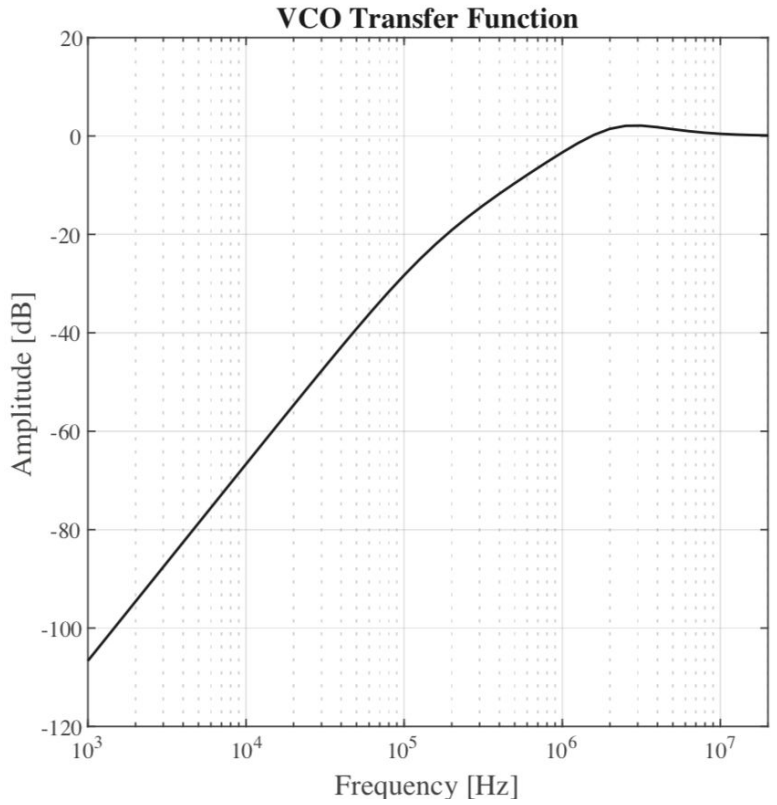
Parameters

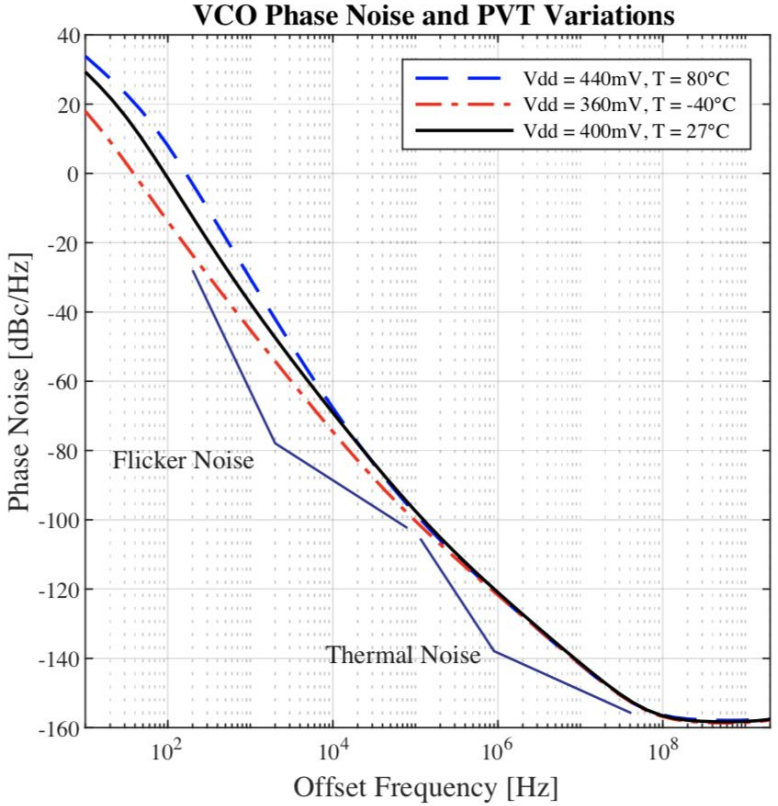
- $I_{cp} = 1.2mA$
- $K_{VCO} = 220\ MHz/V$
- $C_p = 9.35pF$
- $C_s = 233.9pF$
- $R_s = 5.05k$



Results - PVT Variations – Phase noise of the VCO

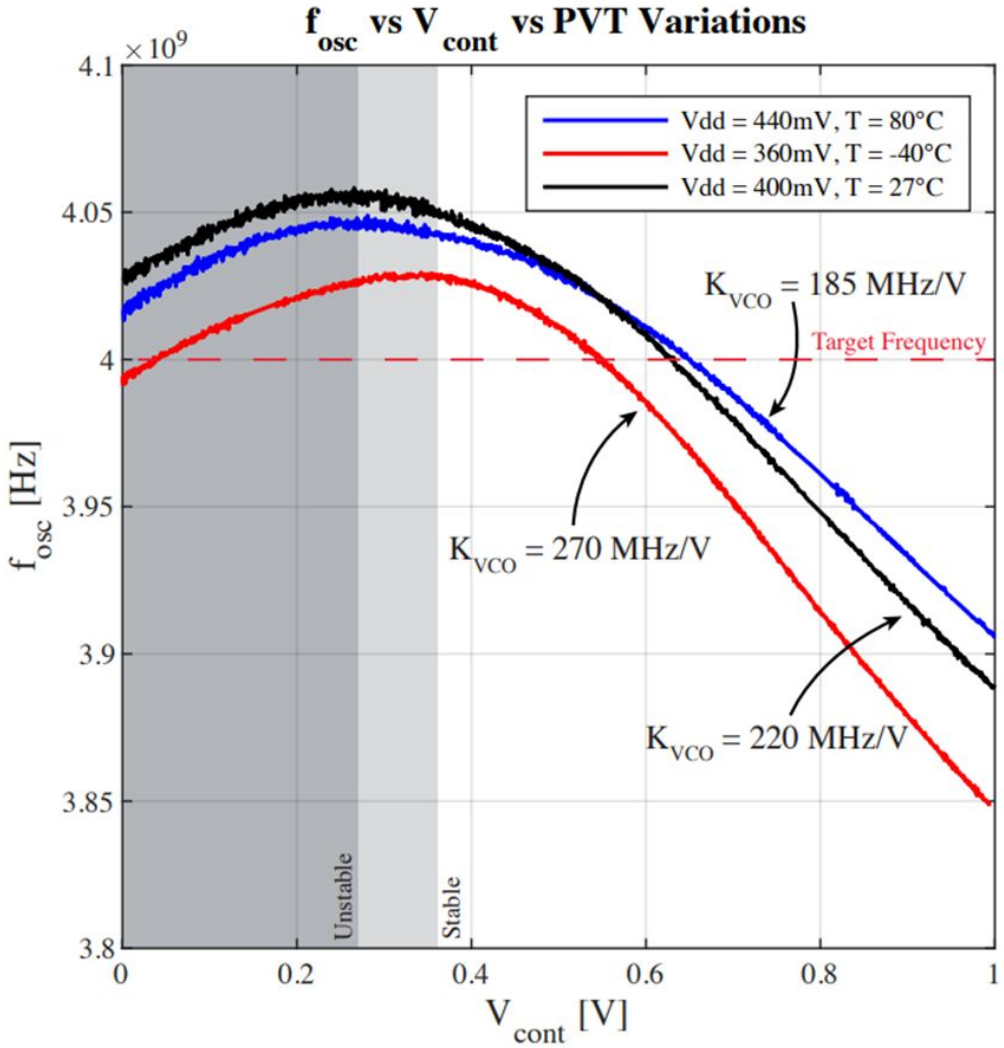
- Negligible effects on VCO phase noise
- Biggest changes in flicker noise region
    - Filtered out by VCO's output transfer function





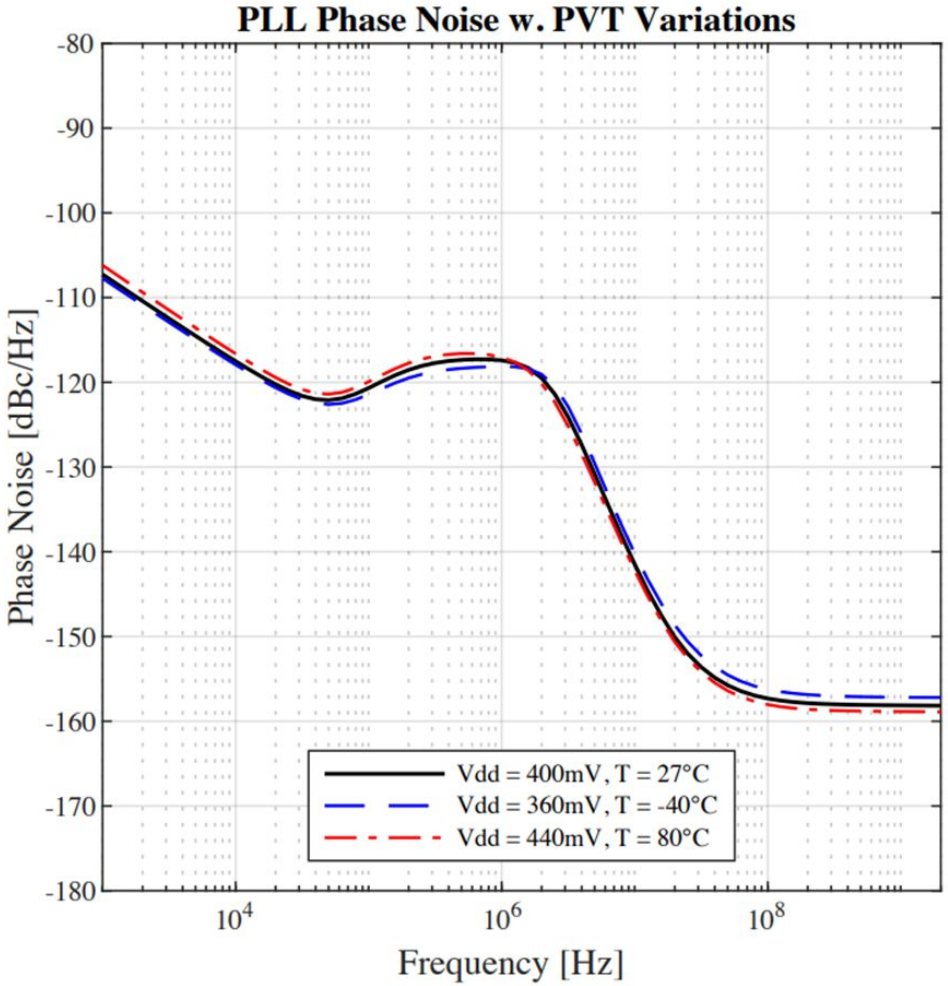
Results - PVT Variations – Varactor w.r.t K_{VCO}

- Substantial K_{VCO} change because of PVT variations
- Stable region gets smaller
- A change in K_{VCO} should have negative effects on PLL's noise performance



Results - PVT Variations – PLL Phase Noise

- Negligible effects on noise performance when considering PVT variations
- Loop Filter dominates all noise plots



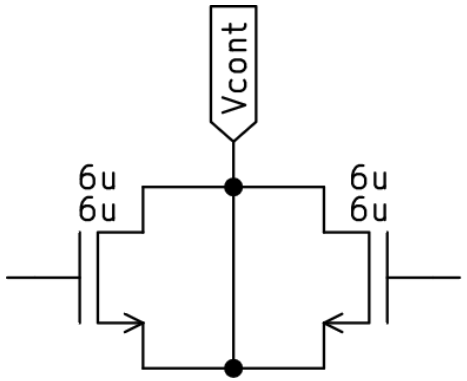
Further possible improvements

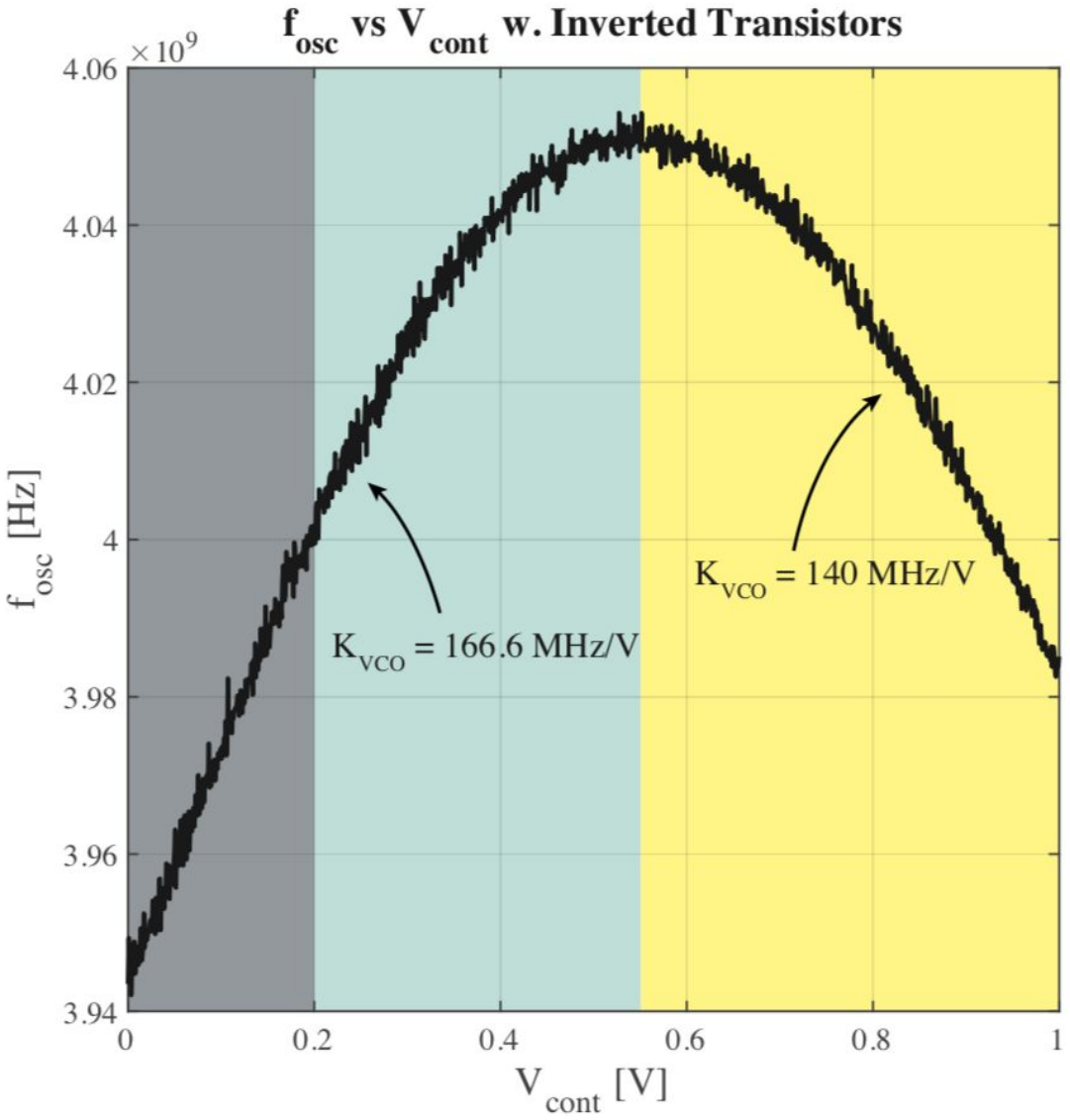
- Charge pump
  - Replace the ideal operational amplifier with a realistic design
- VCO
  - Try different varactor topologies for improved K_{VCO}
  - Adding coarse tuning options to the cap bank for wider tuning range
- BW optimization
  - VCO power↓, VCO noise↑with the same FoM
- Improve lock time
- Improve FoM

Questions?

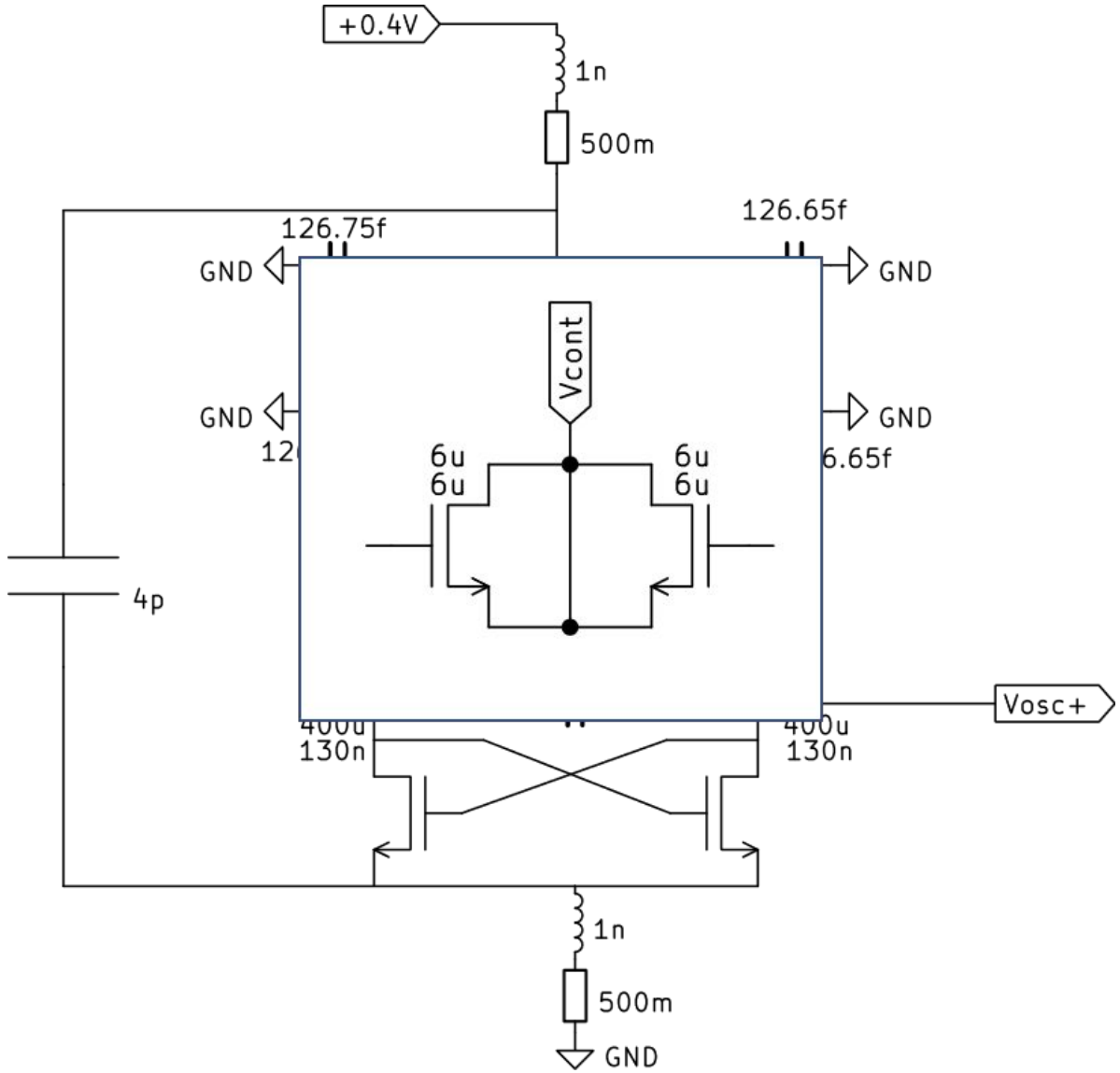
Appendix – Inverted varactors

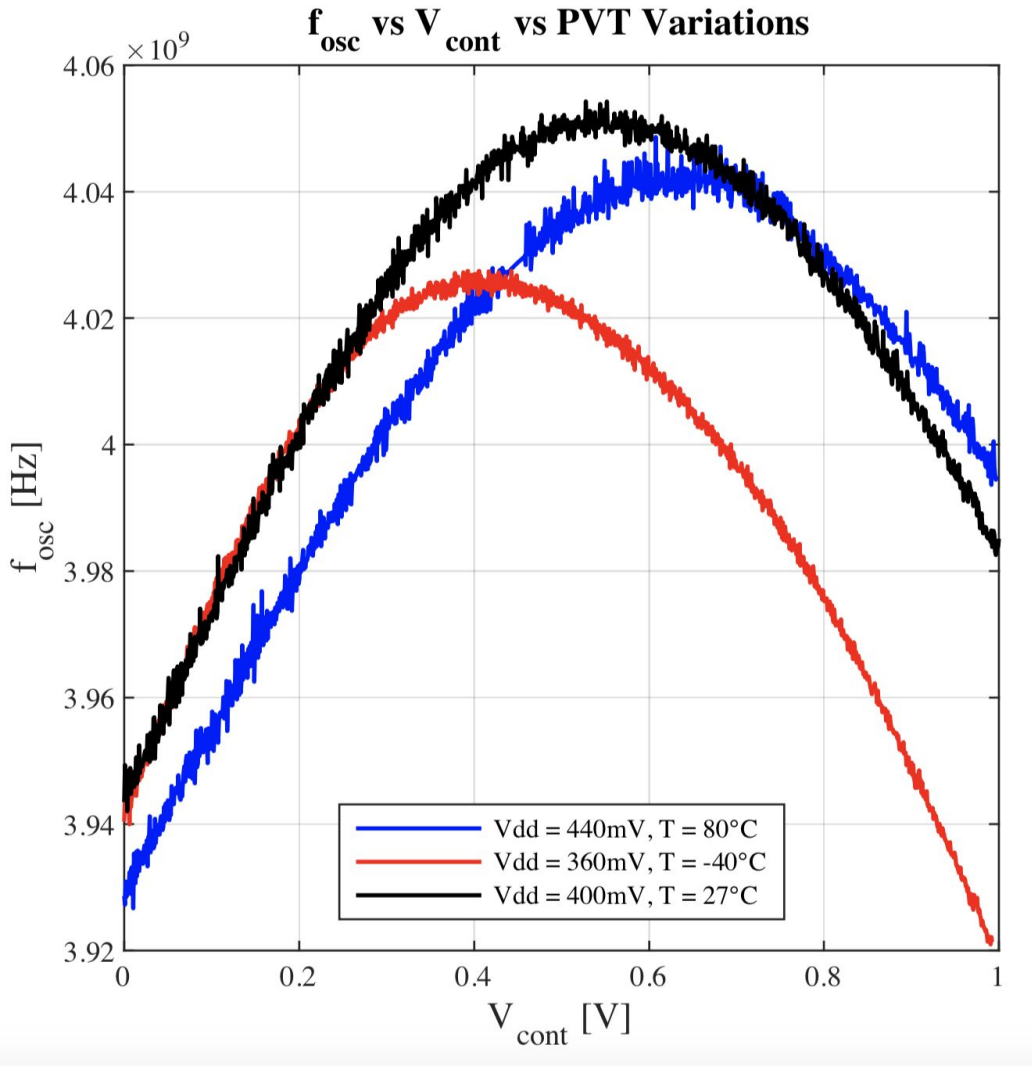
- Extremely small voltage range
- Easy to enter an unstable region of the PLL's operating region
- Low Kvco



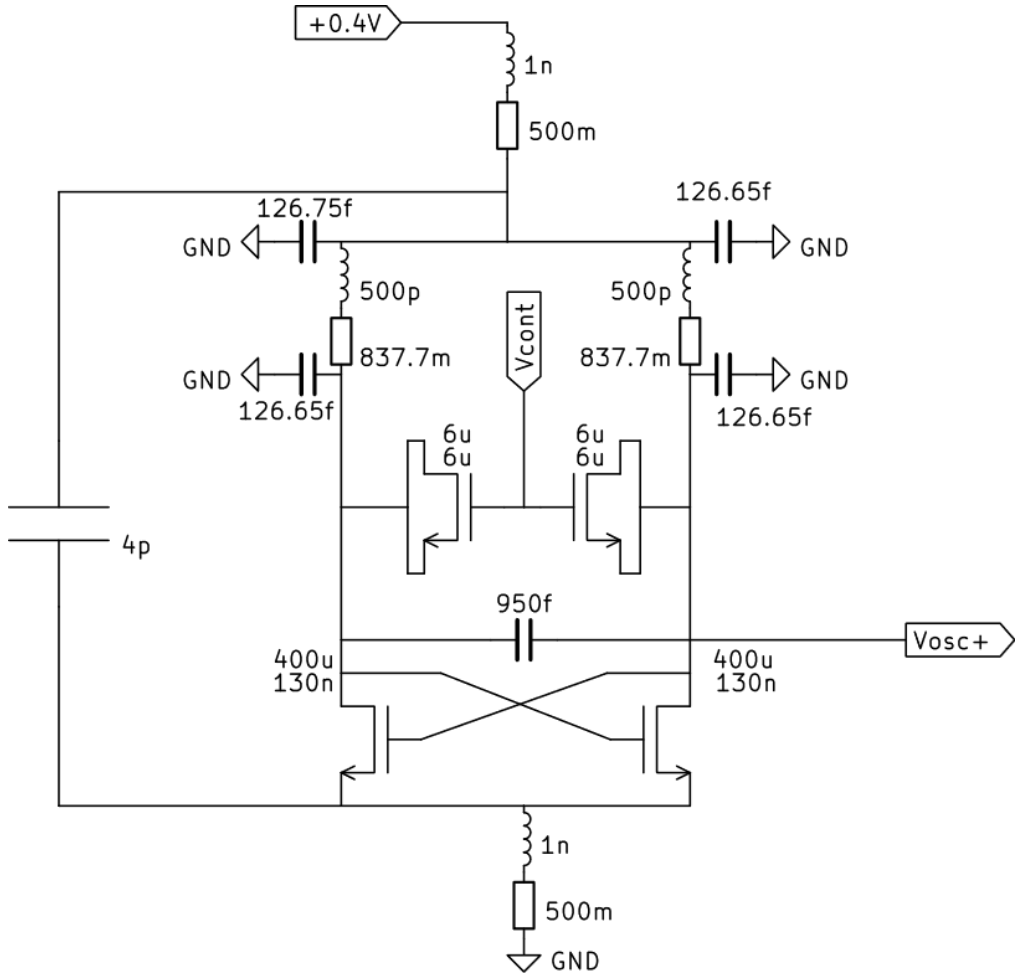


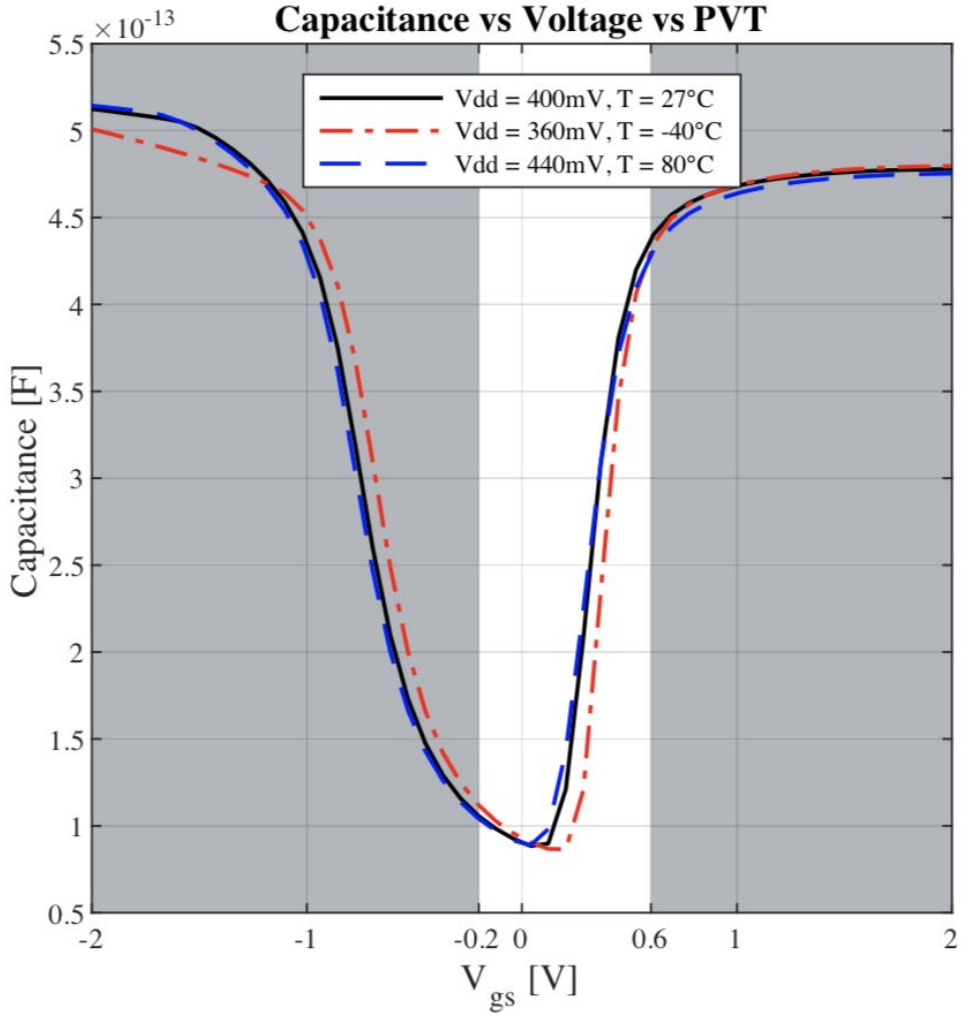
Appendix – Inverted varactors PVT



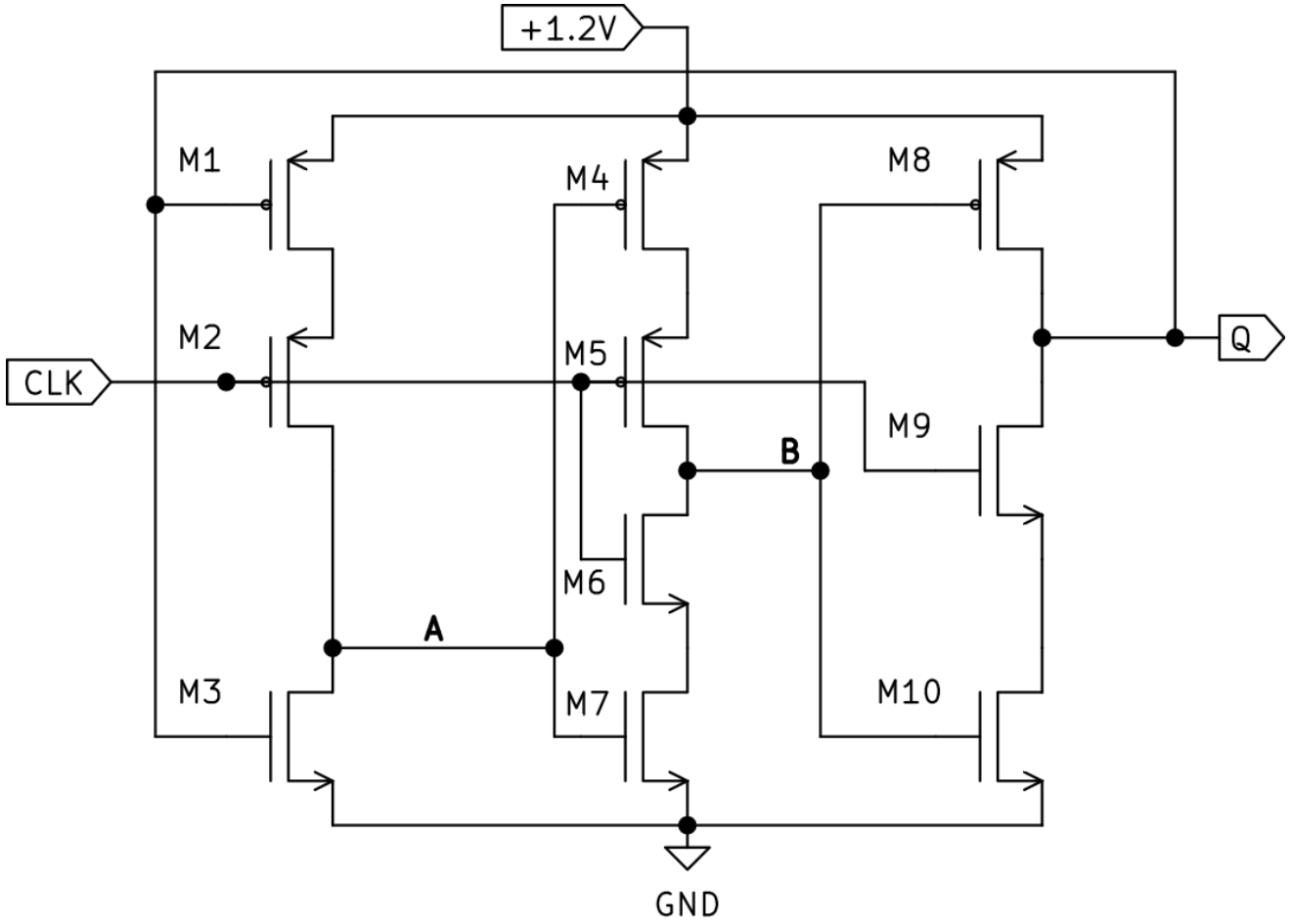


Appendix – Normal Varactors PVT



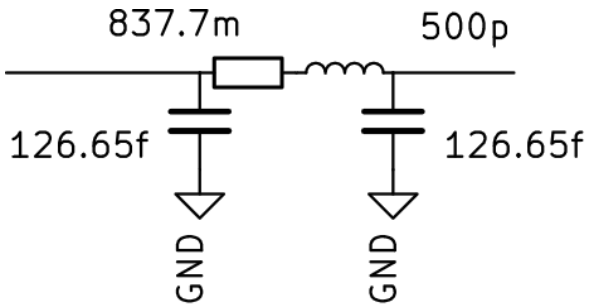


Appendix – TSPC Schematic

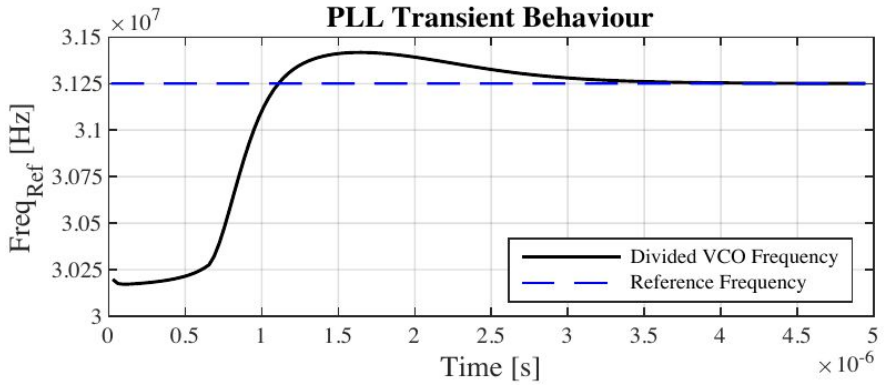


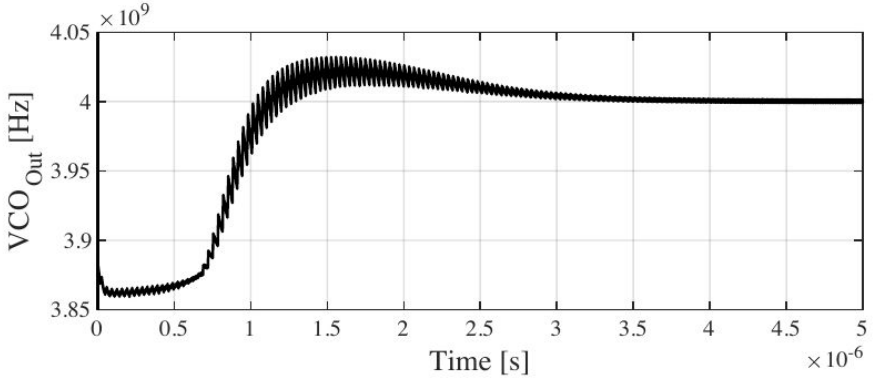
Appendix – Inductor Model

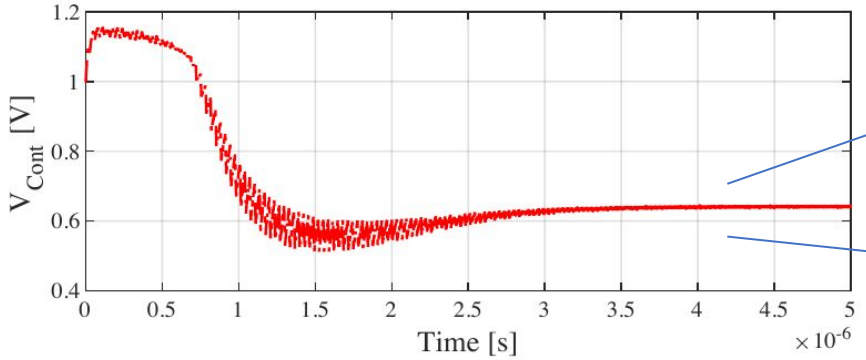
- Inductance value arbitrarily chosen to be L = 500 pH
  - Chosen to fit oscillation frequency of 4GHz
- «Normal inductor» assumed, with Q=15
- $\mathrm{R} = \frac{\omega \cdot L}{Q} = 837.7 m\Omega$
- A harmonic at 5x the oscillation frequency was assumed for the parasitic capacitance
- $C = \frac{1}{(5\omega)^2 \cdot L} = 126.65 fF$

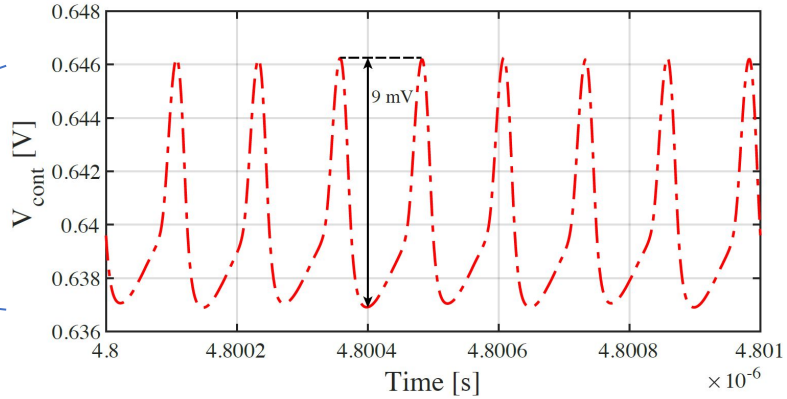


Appendix – Transient Ripple of V_{cont}

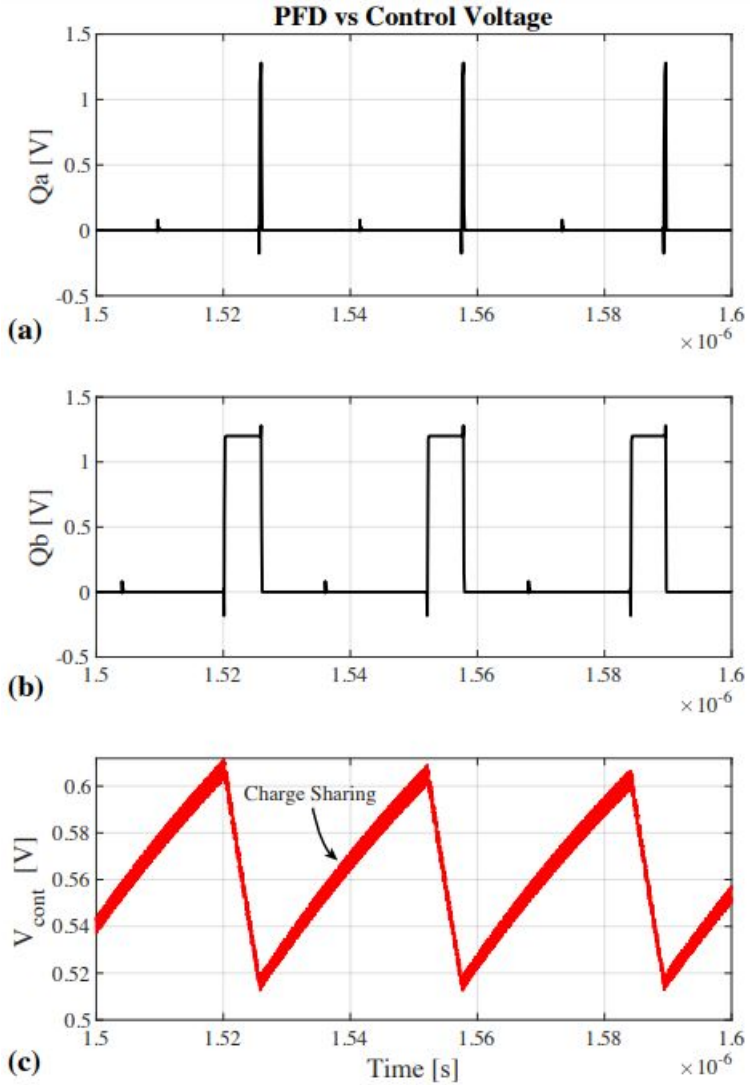








Appendix – PFD signals and charge sharing



Appendix – PFD signals and charge sharing

	ISSCC 2015 L.Kong	VLSI 2017 T.Seong
Technology (nm)	45	65
Architecture	Analog PLL	Analog PLL
Output Freq [Hz] **Tuning Range [Hz]**	2.4G 2G to 3G	3.008G
Mult. Factor, N	106	64
Int. rms Jitter [fs] **Int. Range [Hz]**	970 1K to 200M	357 1K to 80M
Ref. Spur [dBc]	-65	-71
Area [mm2]	4	4.6
Power [mW]	0.015	0.047