IMX7ULP-EVK-BB

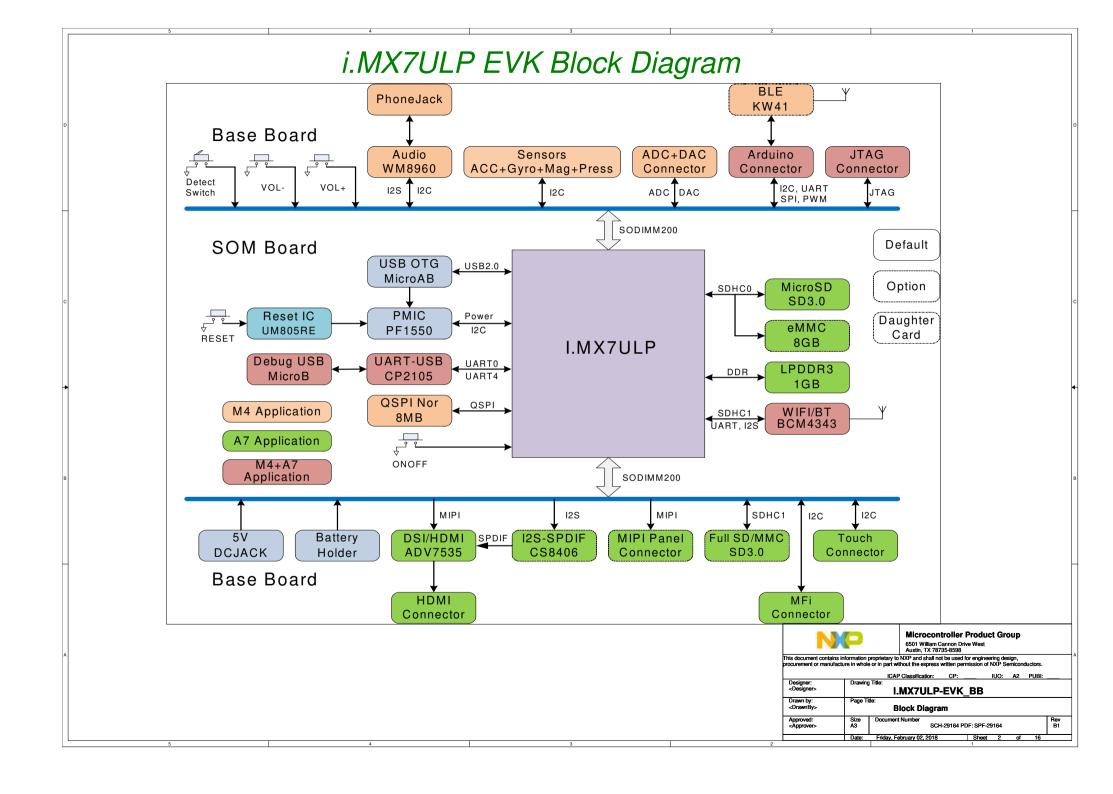
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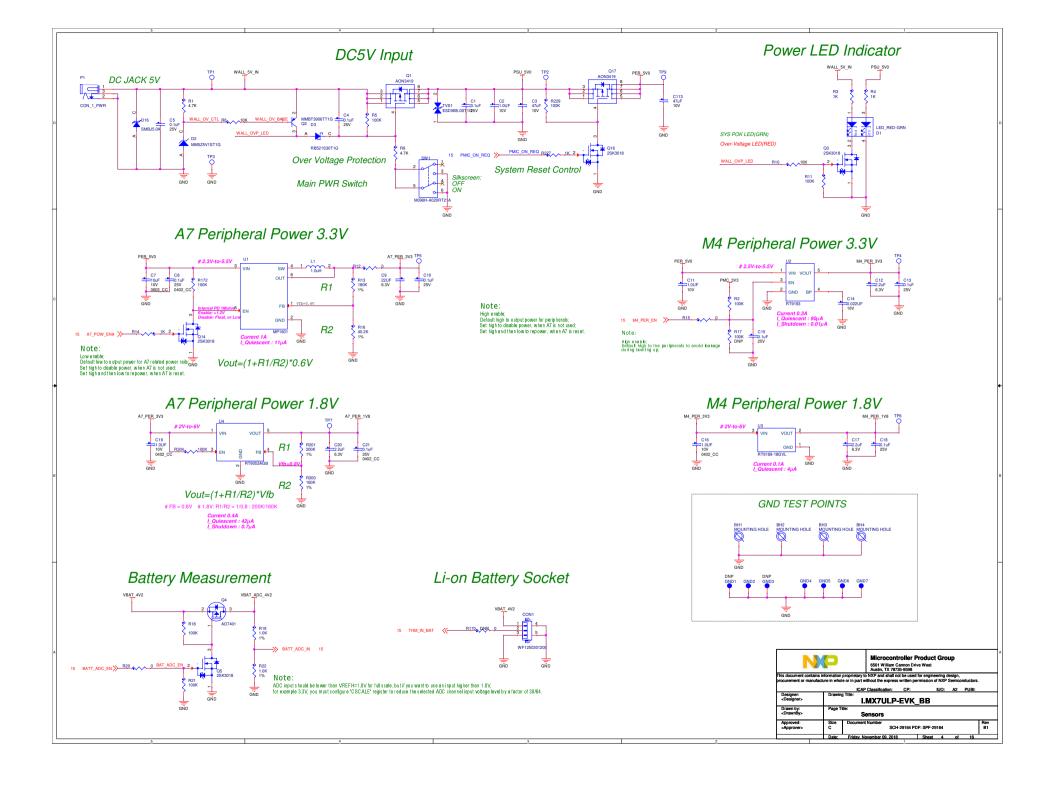
Revision History

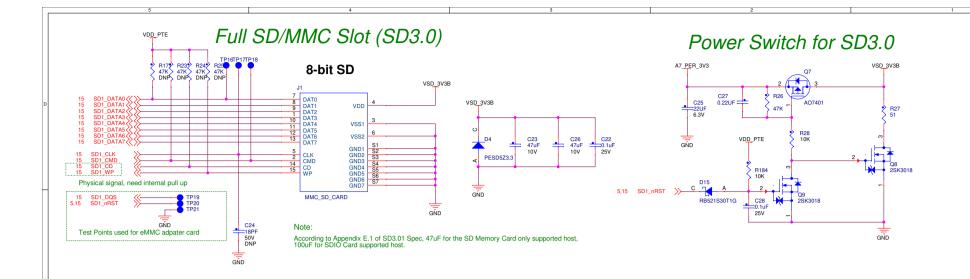
Rev. Code	Date	Description
A	2016/3/10	First Release
A1	2016/12/15	1. Add U15 and related circuit for MCLK workaround;
A2	2016/12/22	1. Correct HDMI_SCL/SDA connection; 2. Add R188-R191 for KW41 SPI interface; 3. Change Arduino jump resistors to 0603 package for easier manual soldering; 4. Add A7 option for Audio Codec, with R210-R212;
A3	2017/01/15	1. Correct PTA8/9 ADC channel mapping to CH5A/B; 2. Update MTPI-HDMI signal names; 3. Add J17 and related circuits to support external BT module; 4. Swap MIC/GND of Phonejack J5 to support CTIA Standard instead of CMTP; 5. Add 10K pull down on MFI_RST_B, as some MFI peripherals need this for MFI address selection; 6. Add Q16, Q17 for PMIC_OM_REQ to control peripheral 5V; 7. Add optional 1.8V input for ADC power supply;
В	2017/12/20	1. Remove CLKO(PTBO) to MCLK circuit, as BO fixed the issue; 2. Add I2C option for U9 WM8960 to A7 core;
B1	2017/02/01	1. Update the IOMUX table;



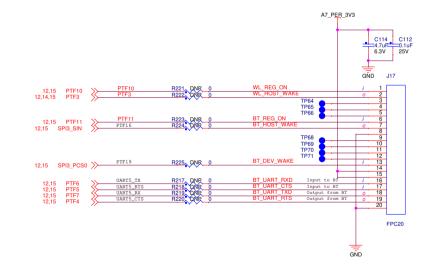


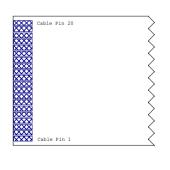
Power Distribution Diagram Power Control Diagram PMC 1V8 LDO M4 1.8V VDD PTB LDO M4 VLDO3 VLDO3 VDD_DIG0 VDDIO RESET1(A7) VDDIO VDD PTB Internal Drive I.MX7ULP M4 RESETBMCU RESET0 VLDO1 VDD PTA M4 Core (open drain) (M4+A7) INTB GPIO <---VSYS VBAT4V2 USB Adapter PMIC (open drain) powered by 1.8V, 5V@1A controlled by M4 SCL SCL 0.65-1.15V VDD_DIG1 LDO_A7 1.1V@1A (open drain) PMIC SDA SDA 1.2V@1A (open drain) I.MX7ULP I.MX7ULP VDD_DDR A7 Core WDI 1.8V@1A SW3 VLDO2 3.3/1.8V@0.4A VBAT4V2 1.8V LDO VSYS VDD PTC, Others ONKEY Ţ. ONOFF 3.3V VDD_PTF ONOFF Key 3.3/1.8V VDD_PTE ► PWRON PMIC_ON_REQ ◀----DCDC3V3 Power Path VSNVS Circuit WIFI 3.0V STANDBY PMIC STBY REQ ----VDDQ EWM_OUT_B VDD1 LPDDR3 RESET Key VDD2 LDO SD1_VSEL 3.3V VCC PTE SD/MMC eMMC/SD 3.3/1.8V resistor DCDC&LDOs A7_POW_EN# 3.3/1.8V LDO VIO A7 Peripherals WIFI/BT DCDC&LDOs M4 PER EN M4 Peripherals DCDC&LDOs DC5V@2A A7 Peripherals Power Adapter Other Peripherals On Base Board DCDC&LDOs **Microcontroller Product Group** M4 Peripherals 6501 William Cannon Drive West Austin, TX 78735-8598 This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semico Designer: <Designer> I.MX7ULP-EVK BB **Power Distribution Diagram** SCH-29164 PDF: SPF-29164 Friday, February 02, 2018 Sheet 3





BLUETOOTH SOCKET





NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the Murata WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

Microcontroller Product Group

6501 William Cannon Drive West

Austin, TX 78735-8998

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ICAP Classification: CP: IUO: A2 PUBI:

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Full SD/MMC Card &BT Interfce

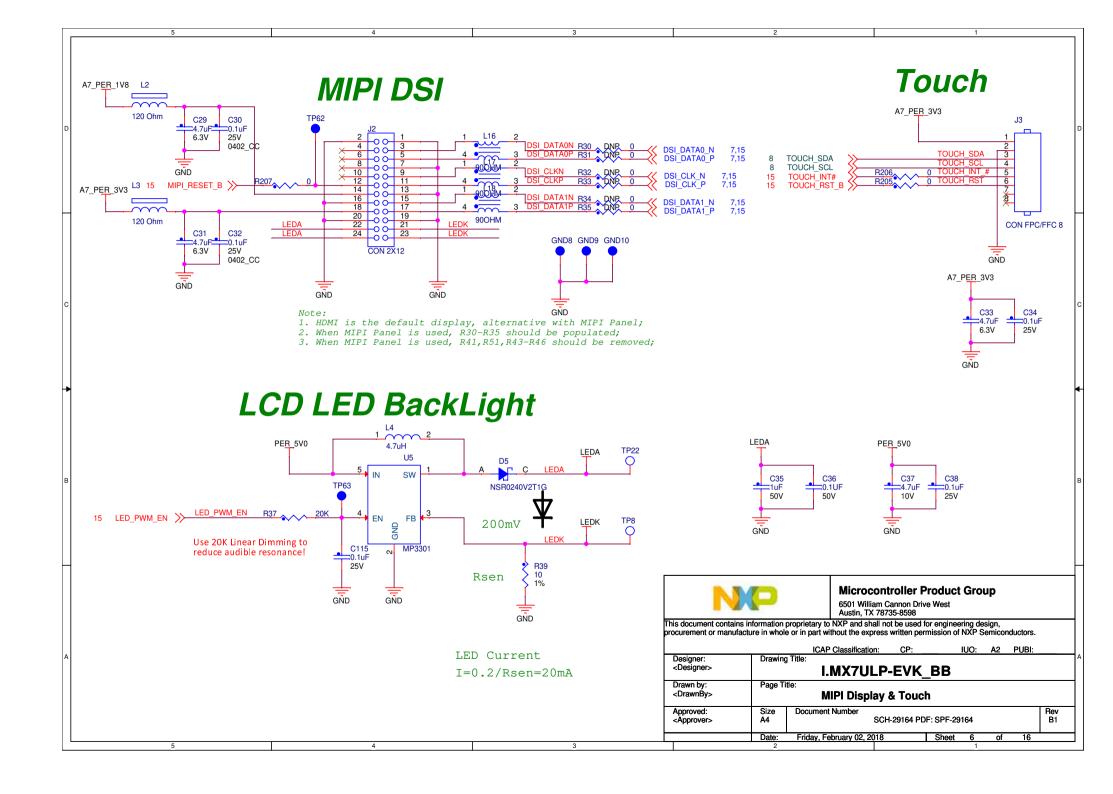
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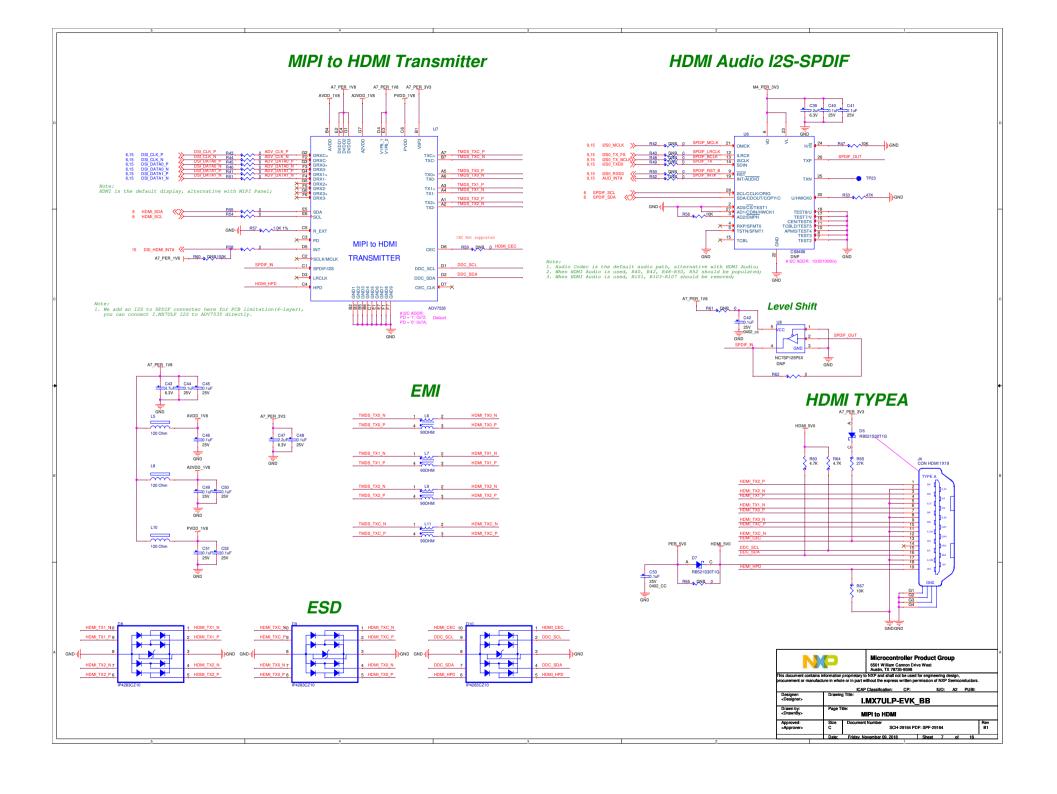
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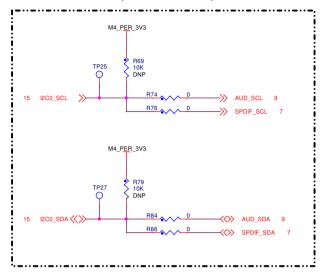
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Date: Friday, February 02, 2018 Sheet 5 of 16

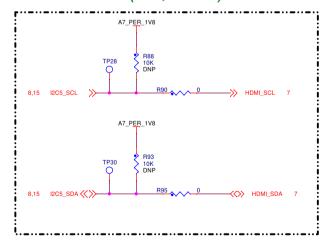




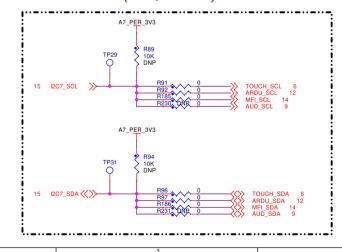
12C0(M4, 3.3V)



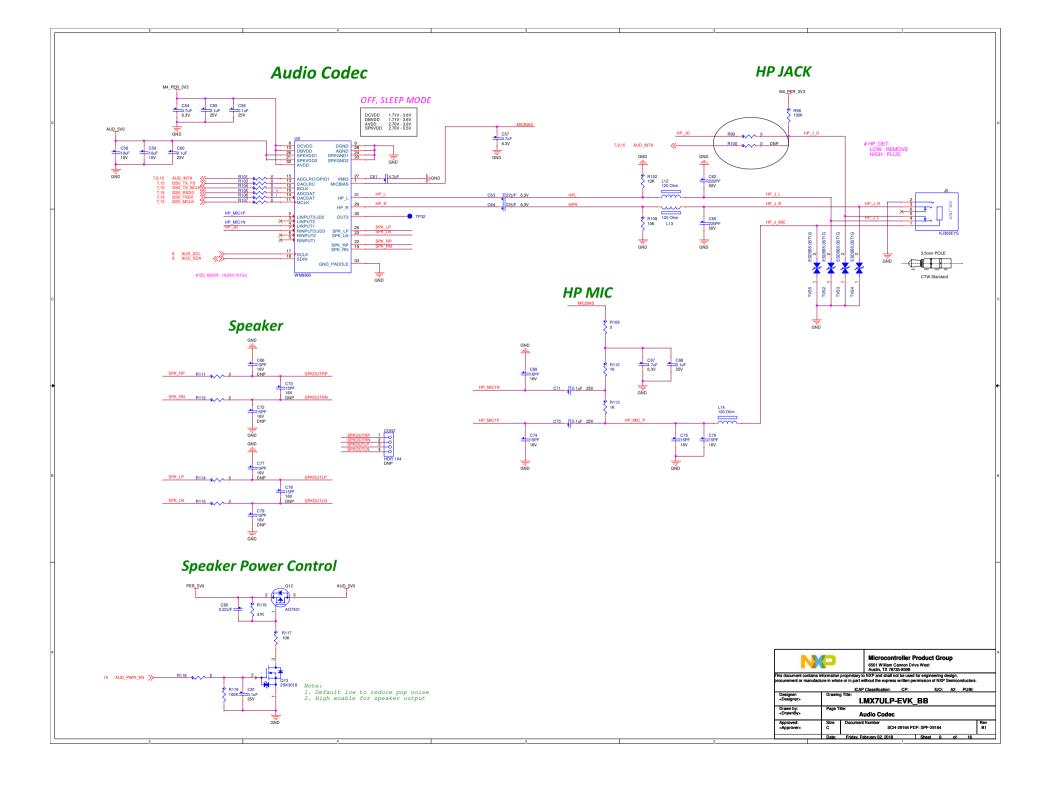
I2C5(A7, 1.8V)

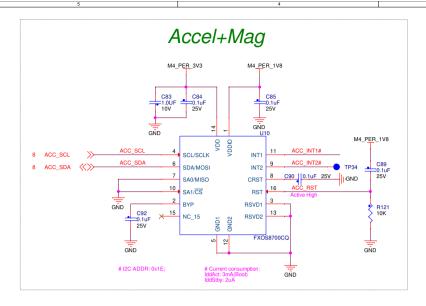


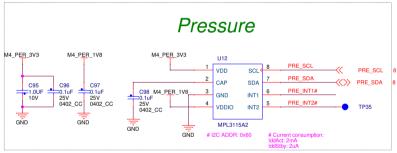
12C7(A7, 3.3V)



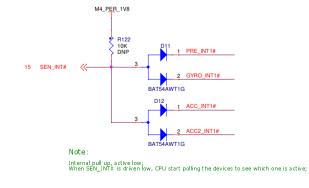
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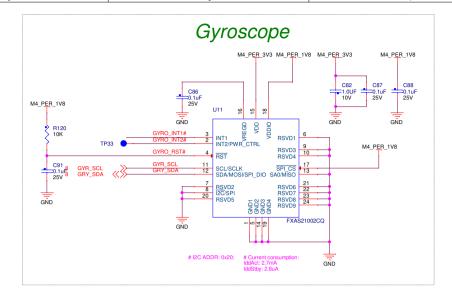


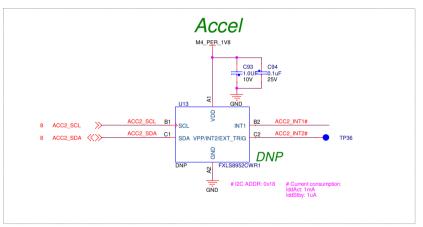


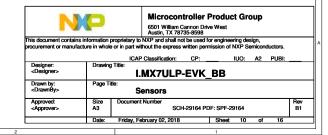


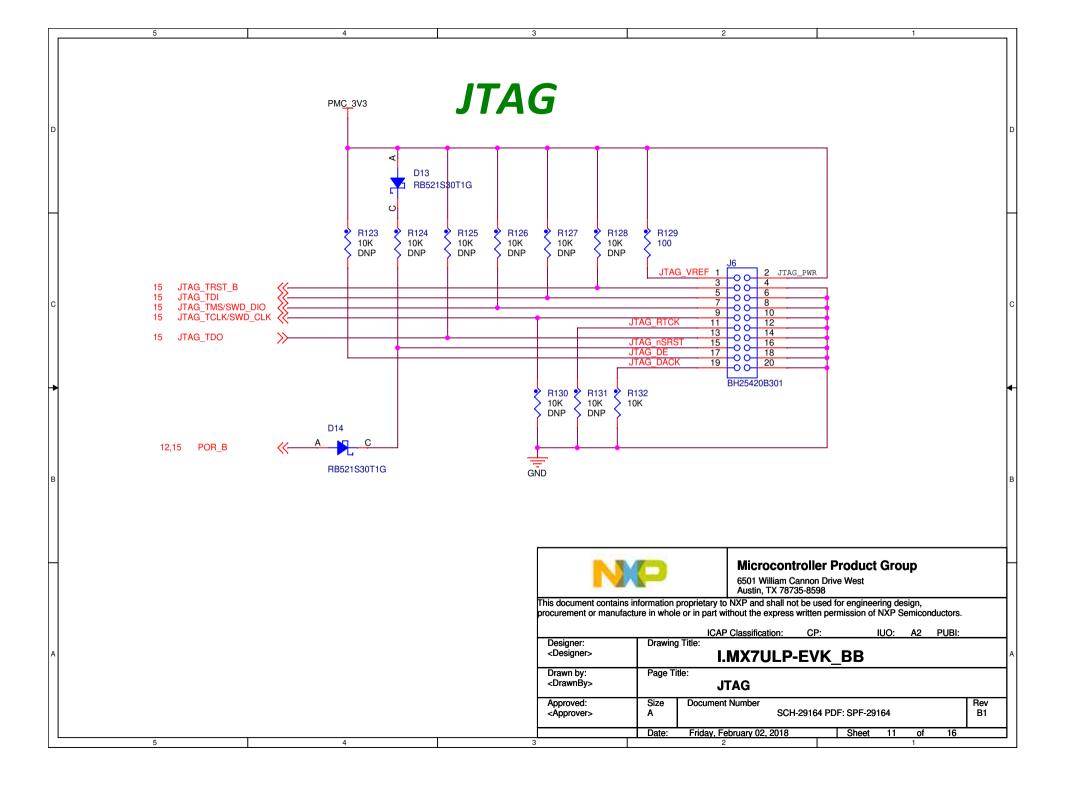
Interrupt

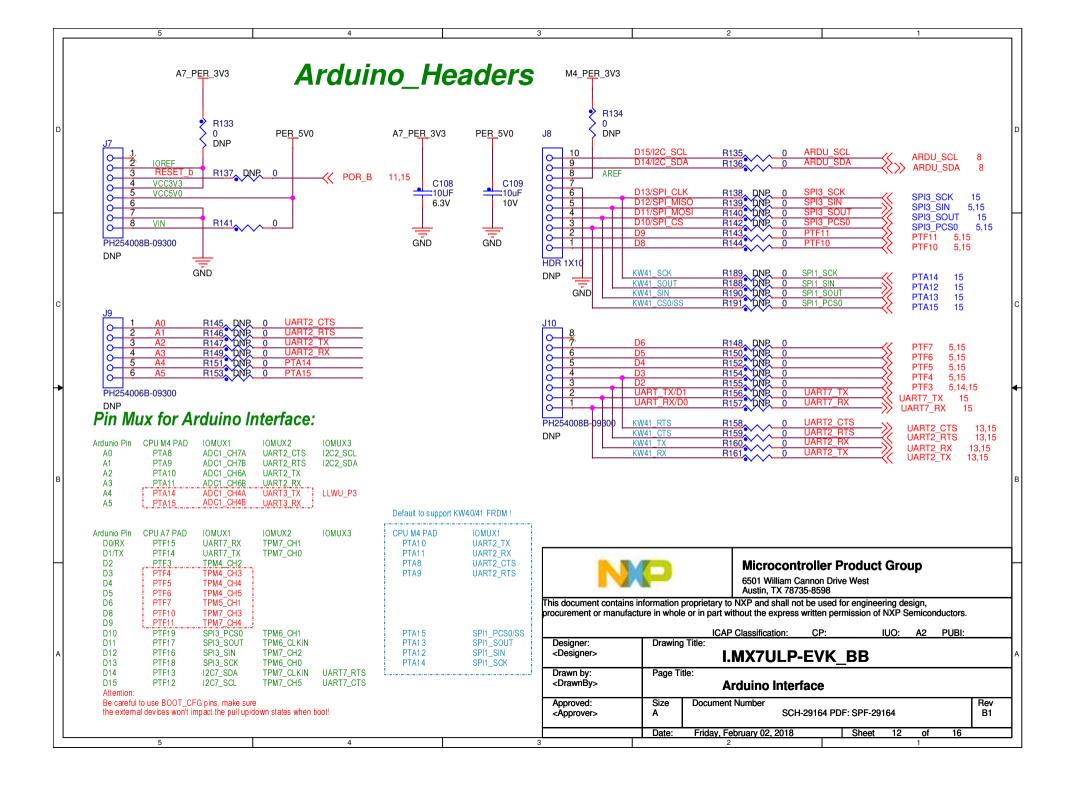


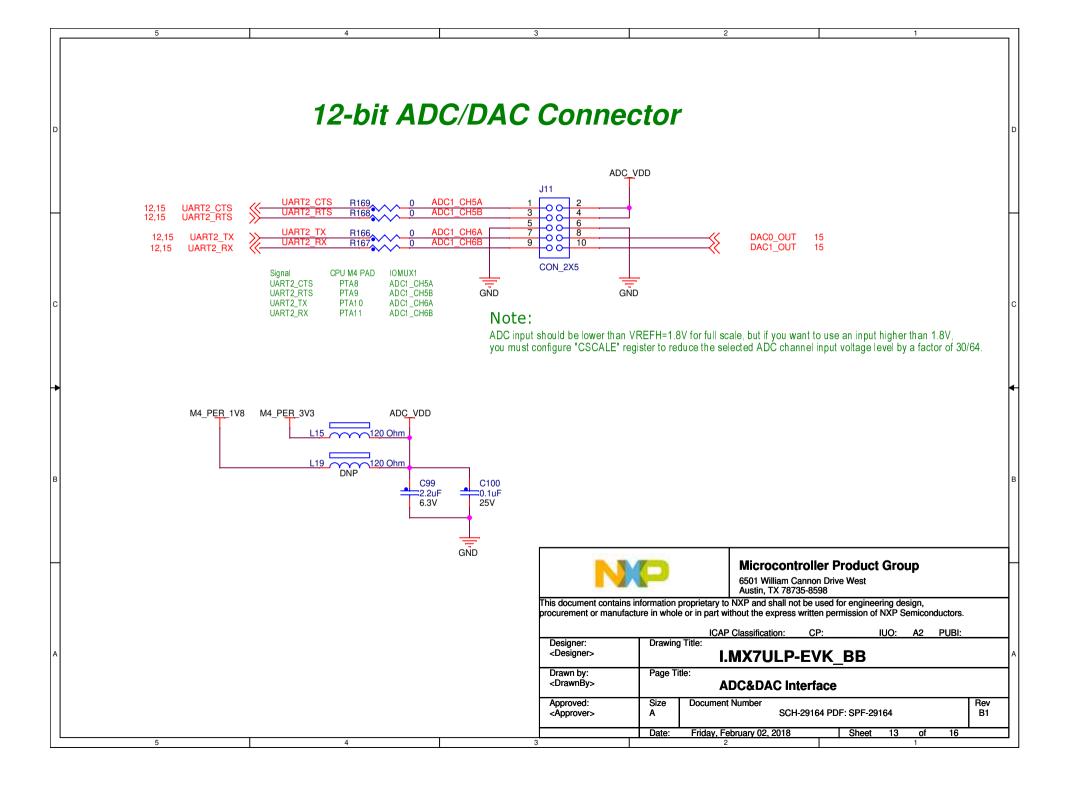


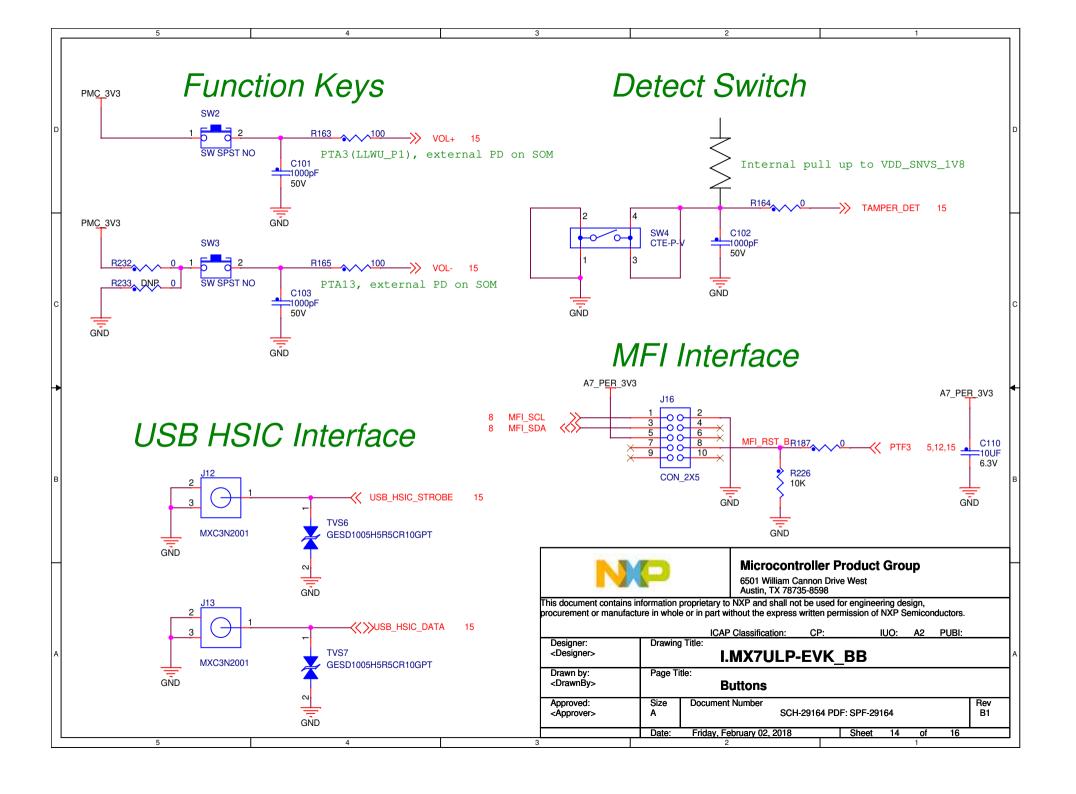


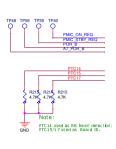


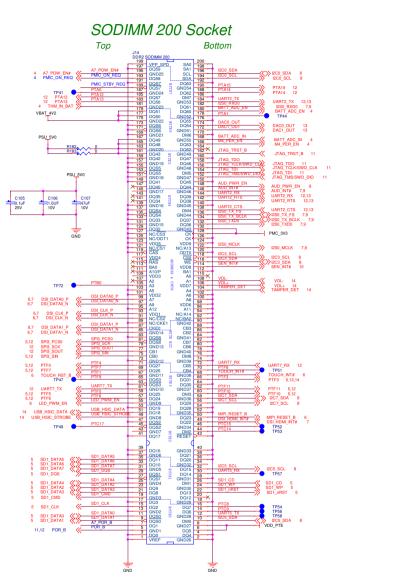














i.MX7ULP B0 IOMUX

NAME	Default	ALTo	ALTı	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT 13	ALT14	Boot Input	PAD DFU
PTA0 PTA1 PTA2 PTA3 PTA4 PTA5 PTA6 PTA7 PTA8 PTA10 PTA110 PTA112 PTA12 PTA14 PTA15	CMPO_HIL_3V CMPO_HIL_3V CMPO_HIL_3V CMPO_HIL_3V ADCI_CH3A ADCI_CH3A ADCI_CH3A ADCI_CH3A ADCI_CH5A ADCI_CH5	CM PO_INI_3V CM PO_INI_3V CM PO_INI_3V CM PO_INI_3V ADCI_CH 3A ADCI_CH 3A ADCI_CH 3A ADCI_CH 3A ADCI_CH 3A ADCI_CH 5A ADC	PTA0 PTA1 PTA2 PTA3 PTA4 PTA5 PTA6 PTA7 PTA8 PTA9 PTA11 PTA12 PTA13 PTA14 PTA15 PTA15	X100_00 X100_01	LPSPIO_PCS1 LPSPIO_PCS2 LPSPIO_PCS2 LPSPIO_PCS0 LPSPIO_SNI LPSPIO_SOUT LPSPIO_SOUT LPSPII_PCS1 LPSPII_PCS3 LPSPII_PCS3 LPSPII_SIN LPSPII_SOUT LPSPII_SOUT LPSPII_SOUT LPSPII_SOUT LPSPII_SOUT	PUARTO_CTS_D PUARTO_RTS_D PUARTO_RTS_D PUARTO_RTS PUARTO_RTS_D PUARTO_RTS_D PUARTI_GTS_D PUARTI_GTS_D PUARTI_RTS_D PUARTI_RTS_D PUARTI_RTS_D PUARTI_RTS_D PUARTI_RTS_D PUARTI_RTS_D PUARTI_TS_D PUARTI_TS_D PUARTI_TS_D PUARTI_TS_D PUARTI_TS_D PUARTI_TS_TS_D PUARTI_TS_D	LPIZCO_SCL LPIZCO_SOA LPIZCO_SHREQ LPIZCI_SCL LPIZCI_STA LPIZCI_JHREQ LPIZCZ_SOA LPIZCZ_HREQ LPIZCZ_HREQ LPIZCZ_HREQ LPIZCZ_SDA LPIZCZ_HREQ LPIZCZ_SDA LPIZCZ_HREQ LPIZCZ_SDA LPIZCZ_HREQ	TP MO_CLKIN TP MO_CHO TP M	1250_RX_BCLK 1250_RX_F5 1250_RXD1 1250_RXD1 1250_RXD1 1250_TX_BCLK 1250_TX_BCLK 1250_TXD0 1250_TXD0 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK 1250_RX_BCLK				CMP0_DUT NM10_b CMP0_DUT		LLWUO_PO LLWUO_P1 LLWUO_P2 LLWUO_P2 LLWUO_P3		BTO_CFG0 BTO_CFG1 BTO_CFG3 BTO_CFG3 BTO_CFG3 BTO_CFG5 BTO_CFG5 BTO_CFG6 BTO_CFG6 BTO_CFG6 BTO_CFG1 BTO_CFG1 BTO_CFG1 BTO_CFG13 BTO_CFG13 BTO_CFG13 BTO_CFG13 BTO_CFG13 BTO_CFG14 BTO_CFG15	H - Z Z Z Z Z Z Z Z Z
PTA17 PTA18 PTA19 PTA20 PTA21 PTA22 PTA23 PTA24 PTA25 PTA25 PTA26 PTA27 PTA28	CMP1_HIG_3V CMP1_HI3_3V ADCO_CH1 DA ADCO_CH1 DB ADCO_CH3A ADCO_CH3A ADCO_CH3B ADCO_CH8B ADCO_CH8B	CMP1_MIG_3V CMP1_MI3_3V CMP1_MI3_3V ADCO_CHIDA ADCO_CHIDB ADCO_CHIDB ADCO_CHISA ADCO_CHISA ADCO_CHISA ADCO_CHISA	PTA17 PTA18 PTA19 PTA20 PTA21 PTA22 PTA23 PTA24 PTA25 PTA25 PTA26 PTA27 PTA28	TX100_U2 TX100_U3 FX100_U5 FX100_U5 FX100_U6 FX100_U7 FX100_U8 FX100_U9 FX100_U11 FX100_U11 FX100_U12 FX100_U12	LPSPIO_SCK LPSPIO_PCSO LPSPIO_PCS1 LPSPIO_PCS1 LPSPIO_PCS2 LPSPIO_PCS2 LPSPII_PCS1 LPSPII_PCS2 LPSPII_PCS2	IPUARTO_RTS_b IPUARTO_TX IPUARTO_TX IPUARTO_RX IPUARTI_CTS_b IPUARTI_RTS_b IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTI_TS_b IPUARTI_TS_TS_b IPUARTI_TS_TS_b IPUARTI_TS_TS_b IPUARTI_TS_TS_b IPUARTI_TS_TS_b	LPIZCO SDA LPIZCO SDA LPIZCO HREQ LPIZCO SCL LPIZCO SDA LPIZCO SDA LPIZCO SDA LPIZCO HREQ LPIZCO SDA LPIZCO SDA LPIZCO SDA LPIZCO SDA LPIZCO SDA LPIZCO SDA LPIZCO SDA	TPM3_CH3 TPM3_CH4 TPM3_CH5 TPM0_CLKIN TPM0_CH0 TPM0_CH2 TPM0_CH2 TPM0_CH3 TPM0_CH4 TPM0_CH5 TPM0_CH5 TPM1_CH1	12.5 MCLK0 12.5 OTX_BCLK 12.5 OTX_BCLK 12.5 OTX_FS 12.5 OTX_BCLK 12.5 OTX DCLK 12.5 OT			JTAG_TMS/SWD_DIO JTAG_TDI JTAG_TDI	LPTMRO_ALT3 LPTMRO_ALT2	EWM_OUT_b	LLWUO_P4 LLWUO_P5 VLLS_M4_DEB0 LLWUO_P6 VLLS_M4_DEB11 VLLS_M4_DEB10	VILS_A7_DEB0 VILS_A7_DEB11 VILS_A7_DEB10		H - Z H - Z 4 7K PU
P TA29 P TA30 P TA31 P TB0 P TB1 P TB2 P TB3 P TB4 P TB5 P TB6 P TB6 P TB7 P TB8 P TB9 P TB9	ADCO_CHIA ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB ADCO_CHIB	ADCO_CHIA ADCO_CHIB ADCO_CHIDA ADCO_CHIDA ADCO_CHIGA ADCO_CHIGA ADCO_CHIGA ADCO_CHIIA ADCO_CHIIA ADCO_CHIIIA ADCO_CHIIIA ADCO_CHIIIA	PTA30 PTA31 PTB0 PTB1 PTB2 PTB3 PTB4 PTB5 PTB6 PTB7 PTB7 PTB8 PTB9	PX100 D15 PX100 D15 PX100 D17 PX100 D17 PX100 D18 PX100 D21 PX100 D21 PX100 D22 PX100 D23 PX100 D24 PX100 D25 PX100 D26 PX100 D26 PX100 D27 PX100 D27 PX100 D27	LPSPII_SOUT LPSPII_SOUT LPSPII_SCK LPSPII_PCSO LPSPIO_SIN LPSPIO_SOUT LPSPIO_SOUT LPSPIO_PCSO LPSPIO_PCSI LPSPIO_PCSI LPSPIO_PCSI LPSPIO_PCSI LPSPIO_PCSI LPSPII_SOUT LPSPII_SOUT LPSPII_SOUT LPSPII_SOUT LPSPII_SCK	IPUARTS_TX IPUARTS_TX IPUARTO_TX IPUARTO_TX IPUARTO_TX IPUARTI_TX IPUARTI_TX IPUARTI_TX IPUARTZ_TX IPUARTZ_TX IPUARTZ_RX IPUARTZ_RX IPUARTZ_RX IPUARTS_RX	LPI2CO_H REQ LPI2CI_H REQ LPI2CO_SCL LPI2CO_SDA LPI2CO_SCL	TP M2_CLKIN TP M2_CH0 TP M2_CH1 TP M3_CLKIN TP M3_CH0 TP M3_CH1 TP M3_CH2 TP M3_CH3 TP M3_CH4 TP M3_CH5 TP M0_CLKIN TP M0_CLKIN	1251_TKD0 1251_TKD0 1251_TKD1 1251_TK_F5 1251_TKD1 1251_TKD1 1251_TKD1 1251_TKD3 125_MCLK1 1251_TK_F5 1251_TK_F5 1251_TK_F5 1251_TK_D0 1251_TKD0 1251_TKD0	Q SPIA_DATA7 Q SPIA_DATA5 Q SPIA_DATA5 Q SPIA_SSI_B Q SPIA_SQ_B Q SPIA_DQS	СЬКОИТО	JTAG_TCLK/SWD_CLK JTAG_TRST_b TRACE_CLKO UT TRACE_D 0 TRACE_D 0 TRACE_D 2 TRACE_D 3 TRACE_D 3	LPTMRO_ALT1 CMP1_OUT RTC_CLKOUT LPTMR1_ALT2 SEC_VIO_B RTC_CLKOUT LPTMR1_ALT3 CMP1_OUT RTC_CLKOUT	EWM_IN EWM_OUT_b EWM_IN	LIWUO_P7 VILS_M4_DEB9 LIWUO_P8 VILS_M4_DEB8 LIWUO_P9 LIWUO_P10 LIWUO_P11 LIWUO_P12 VILS M4_DEB1	VILS_A7_DEB9 VILS_A7_DEB8	BT_MODEO BT_MODE1	100 K P D 4 7 K P D 4 7 K P D H - Z H - Z H - Z H - Z 100 K P D 100 K P D H - Z H - Z
PTB1 1 PTB1 2 PTB1 3 PTB1 4 PTB1 5 PTB1 6 PTB1 7 PTB1 8 PTB1 9 PTC0 PTC1 PTC2 PTC3 PTC3 PTC4	CMPD_III CMPD_III CMPD_III 3 ADCI_CH13B/CMP1_III ADCI_CH2B ADCI_CH2B ADCI_CH2B ADCI_CH2B ADCI_CH3B ADCI_CH	CM PO_HII CM PO_HII3 ADC1_CH 13A/CM P1_HII0 ADC1_CH 13B/CM P1_HII1 ADC1_CH 2A ADC0_CH AA ADC0_CH AA ADC0_CH SA ADC0_CH SA ADC0_CH SA	PTB11 PTB12 PTB13 PTB14 PTB15 PTB16 PTB17 PTB18 PTB19 PTC0 PTC1 PTC2 PTC3 PTC4	FXIOO_D29 FXIOO_D30 FXIOO_D31	LPSPHI_PCSO LPSPHI_PCSI LPSPHI_PCS2 LPSPHI_PCS2 LPSPHI_PCS3	LPUART2_TX LPUART2_RX LPUART4_CTS_b LPUART4_RTS_b LPUART4_TX LPUART4_TX	LPIZCA_SCL LPIZCA_SCA LPIZCA_SCL LPIZCA_SCA LPIZCA_SCA LPIZCA_HREQ LPIZCA_HREQ LPIZCA_SCL LPIZCA_SCA LPIZCA_HREQ	TP MO_CH1 TP MI_CKKIN TP MI_CH0 TP MI_CH0 TP MI_CH1 TP M2_CKIN TP M2_CH0 TP M3_CKIN TP M3_CKIN TP M3_CKIN TP M3_CKIN TP M3_CH1 TP M3_CH0 TP M4_CH0 TP M4_CH0 TP M4_CH0 TP M4_CH2 TP M4_CH2 TP M4_CH3 TP M4_CH3 TP M4_CH4 TP M4_CH4 TP M4_CH4	1251 RXD1 1251 RXD2 1251 RXD3	O SPIA_DATA4 O SPIA_SSI B O SPIA_SSI K O SPIA_DATA3 O SPIA_DATA3 O SPIA_DATA1 O SPIA_DATA1	Q SPIA_SCLK_b FB_AD 0 FB_AD 0 FB_AD 2 FB_AD 2	TRACE_D4 TRACE_D5 TRACE_D6 TRACE_D7 USBO_ID TRACE_D15 TRACE_D15 TRACE_D14 TRACE_D13 TRACE_D12 TRACE_D11	RTC_CLKO UT		VILS_M4_DEB1 VILS_M4_DEB2 VILS_M4_DEB3 VILS_M4_DEB3 VILS_M4_DEB5 ILWU0_P13 VILS_M4_DEB6 VILS_M4_DEB7 ILWU0_P15	VILS_A7_DEB1 VILS_A7_DEB2 VILS_A7_DEB3 VILS_A7_DEB3 VILS_A7_DEB5 VILS_A7_DEB5 VILS_A7_DEB7 DEBUG_MMX0 DEBUG_MMX1 DEBUG_MMX2 DEBUG_MMX2 DEBUG_MMX2 DEBUG_MMX2 DEBUG_MMX2		H Z H Z H Z Z H Z Z
P TC5 P TC6 P TC7 P TC8 P TC9 P TC1 0 P TC1 1 P TC1 2 P TC1 3 P TC1 4 P TC1 5 P TC1 6 P TC1 7 P TC1 8 P TC1 8	D ISABLED		PTC4 PTC5 PTC6 PTC7 PTC8 PTC10 PTC10 PTC11 PTC12 PTC13 PTC14 PTC15 PTC16 PTC16 PTC17 PTC18 PTC19 PTD10 PTD1	RXIO1_D0 RXIO1_D1 RXIO1_D2 RXIO1_D3 RXIO1_D5 RXIO1_D5 RXIO1_D6 RXIO1_D6 RXIO1_D1 RXIO1_D10 RXIO1_D11 RXIO1_D12 RXIO1_D13 RXIO1_D14 RXIO1_D15	LPSPIZ_PCS1 LPSPIZ_PCS2 LPSPIZ_PCS3 LPSPIZ_SIM LPSPIZ_SOUT LPSPIZ_SCW LPSPIZ_PCS0 LPSPIZ_PCS0 LPSPIZ_PCS0 LPSPIZ_PCS3 LPSPIZ_PCS3 LPSPIZ_SOUT LPSPIZ_SOUT LPSPIZ_SOUT LPSPIZ_SOUT	UPUARTY_CTS_D UPUARTY_TS_D LPUARTY_TX LPUARTY_TX LPUARTS_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D LPUARTT_CTS_D	LPIZCS_SCI LPIZCS_SDA LPIZCS_HREQ LPIZC6_SCI LPIZC6_SDA LPIZC6_HREQ LPIZC7_SDA LPIZC7_SDA LPIZC7_HREQ	TPM4_CH3 TPM4_CH4 TPM4_CH5 TPM5_CH1 TPM5_CLKIN TPM5_CLKIN TPM7_CH3 TPM7_CH4 TPM7_CH4 TPM7_CH5 TPM7_CH4 TPM7_CH0 TPM7_CH0 TPM7_CH0 TPM7_CH1 TPM7_CH1 TPM7_CH2 TPM6_CH0 TPM6_CH1		SD HCO_RESET_b SD HCO_CMD	18_04	TRACE_D11 TRACE_D10 TRACE_D10 TRACE_D10 TRACE_D17 TRACE_D27 TRACE_D3 TRACE_D3 TRACE_D3 TRACE_D3 TRACE_D2 TRACE_D2 TRACE_D2 TRACE_D2 TRACE_D2 TRACE_D3 TRACE_D1 USB0_JD	USB0_ID USB1_OC2 USB0_ID USB1_PWR2	VIU_DE VIU_DE		DEBUG_MUX1 DEBUG_MUX2 DEBUG_MUX2 DEBUG_MUX2 DEBUG_MUX5 DEBUG_MUX5 DEBUG_MUX5 DEBUG_MUX6 DEBUG_MUX6 DEBUG_MUX10 DEBUG_MUX11 DEBUG_MUX11 DEBUG_MUX13 DEBUG_MUX14 DEBUG_MUX14 DEBUG_MUX14 DEBUG_MUX17 DEBUG_MUX17 DEBUG_MUX17		H - Z H - Z
PTD1 PTD2 PTD3 PTD4 PTD5 PTD6 PTD7 PTD8 PTD9 PTD10 PTD10 PTD11 PTE0 PTE1 PTE2 PTE3 PTE3	D ISABLED		PTD 3 PTD 4 PTD 5 PTD 6 PTD 7 PTD 8 PTD 9 PTD 10 PTD 11 PTE 0 PTE 1 PTE 2 PTE 2 PTE 2 PTE 3 PTE 3	FXIO1_D31 FXIO1_D30 FXIO1_D29 FXIO1_D28 FXIO1_D27 FXIO1_D26	LPSPIZ_PCS1 LPSPIZ_PCS2 LPSPIZ_PCS3 LPSPIZ_SIN	LPUART4_CTS_b LPUART4_RTS_b LPUART4_TX LPUART4_RX LPUART5_CTS_b	LPIZC4_SCL LPIZC4_SDA LPIZC4_HREQ LPIZC5_SCL	TPM4_CLKIN TPM4_CH0 TPM4_CH1 TPM4_CH2 TPM5_CH1 TPM5_CKN		SDHCO_CCSH_D SDHCO_CLS SDHCO_DF SDHCO_DF SDHCO_DF SDHCO_D5 SDHCO_D2 SDHCO_D2 SDHCO_D2 SDHCO_D2 SDHCO_D1 SDHCO_D0 SDHCO SDHC	FB.A25 FB.A26					DEBUG_MUX20 DEBUG_MUX21 DEBUG_MUX22 DEBUG_MUX23 DEBUG_MUX23 DEBUG_MUX23 DEBUG_MUX23 DEBUG_MUX27 DEBUG_MUX27 DEBUG_MUX27 DEBUG_MUX29 DEBUG_MUX29 DEBUG_MUX29 DEBUG_MUX30 DEBUG_MUX30 DEBUG_MUX31 DEBUG_MUX31		H - Z Z H - Z Z H - Z Z Z H - Z Z Z Z Z Z Z Z Z
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PTF17 PTF18 PTF19	DISABLED DISABLED		PTF17 PTF18 PTF19	,xi01_015	LPSPI3_SOUT LPSPI3_SCK LPSPI3_PCS0			TPM6_CLKIN TPM6_CH0 TPM6_CH1			FB_AD 31		USB1_DATA7	VIU_D14 VIU_D15				HIZ

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