

Vidyavardhini's College of Engineering & Technology Department of Artificial Intelligence and Data Science (AI&DS)

Name:	Yash Ravindra Kerkar
Roll No:	67
Class/Sem:	SE/IV
Experiment No.:	9
Title:	Program for interfacing 8086 with 8255 PPI.
Date of Performance:	22/03/24
Date of Submission:	05/04/24
Marks:	
Sign of Faculty:	



Vidyavardhini's College of Engineering & Technology

Department of Artificial Intelligence and Data Science (AI&DS)

Aim: 8255 is configured in mode O is simple Inuput / Output Mode. Ports A,B,C are in mode 0. All the posts are in output mode and data is transmitted to the respective ports.

Apparatus: Microprocessor 8086 and 8255 PPI experimental setup kit

Theory:

The programmable Peripheral Interface chip 8255 has three 8-bit Input / Output ports i.e. Port A, Port B, Port C upper (PCU) and Port C lower (PCL). Direct bit set/reset capability is available for port C. 8255 is a very powerful tool for interfacing peripheral equipment to the microprocessor. It is flexible enough to interface with any I/o device without the need of external logic.

Procedure:

- 1. Connect 8086 kit to 8255 PPI kit using 50 pin FRU cable.
- 2. Default I/O address ranges are:

SELECTION	ADDRESS
Port A	30 H
Port B	31 H
Port C	32 H
Command Port	33 H

3. 80 H is the control word for 8255. It is set in simple I/O mode and all the ports are in output mode 0

D7	D 6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0
*	•	7	*	*	₩	\	*
Always 1	Grou	ın A	Port A	Port C1	Group B	Port B	Port C2
for I/O		de 0	(output)	(output)	(output)	(output)	(output)

- 4. The LED's connected to the pins at Port A glow according to the data transmitted on port A.
- 5. The LED's connected to the pins of port B glow according to the data transmitted on Port B.
- 6. The LED's connected to the pins of port C glow according to the data transmitted on Port C.



Vidyavardhini's College of Engineering & Technology Department of Artificial Intelligence and Data Science (AI&DS)

Program:

Segment: C000 Offset: C000

Memory	Opcode	Instructions	Comments	
C000	В0	MOV AL,80H	Mode 0, All ports in output mode	
C001	80		_	
C002	E6	OUT CWR, AL		
C003	33			
C004	В0	MOV AL, 55H	Data for Port A	
C005	55			
C006	E6	OUT PORT A,AL		
C007	30			
C008	В0	MOV AL,AAH	Data for port B	
C009	AA			
C00A	E6	OUT PORT B,AL		
C00B	31			
C00C	В0	MOV AL,0FH	Data for port C	
C00D	0F			
C00E	E6	OUT PORTC,AL		
C00F	32			
C010	CC	INT 3	Stop	



Vidyavardhini's College of Engineering & Technology

Department of Artificial Intelligence and Data Science (AI&DS)

Conclusion:

In this practical, we successfully demonstrated the interfacing of the 8086 microprocessor with the 8255 Programmable Peripheral Interface (PPI). By configuring the 8255 in Mode 0, we established a simple input/output environment. Through the manipulation of control words and data sent to the designated ports, we showcased the capability to interface with external devices connected to the 8255.

1. Explain the modes of 8255.

Ans. Mode 0 - Basic Input/Output (I/O):

In Mode 0, the 8255 functions as three 8-bit bidirectional ports (Port A, Port B, and Port C).

Port A (PA) and Port B (PB) are used for general-purpose I/O operations.

Port C (PC) is divided into two parts: PC0-PC3 and PC4-PC7.

PC0-PC3 can be configured as individual bits for I/O or combined to form a 4-bit bidirectional I/O port.

PC4-PC7 are used as control lines for various operations such as handshake signals, chip select, or strobe signals.

Mode 1 - Strobed Input/Output:

In Mode 1, Port A (PA) and Port B (PB) operate as input or output ports as in Mode 0.

Port C (PC) operates as two 4-bit ports: Group A (PC0-PC3) and Group B (PC4-PC7).

Group A can be configured for input or output independently of Group B.

Input data is latched into the corresponding latch register upon detection of a strobe signal.

Output data is transferred from the latch register to the output buffer upon detection of a strobe signal.

Mode 2 - Bidirectional Bus I/O:

In Mode 2, the 8255 functions as a bidirectional 8-bit data bus with handshake signals.

Port A (PA) is configured as an input or output port for data transfer.

Port B (PB) is used for handshake signals: Input/Output (I/O), Buffer Enable (BE), and Acknowledge (ACK).

Port C (PC) operates as two 4-bit ports: Group A (PC0-PC3) and Group B (PC4-PC7).

Group A is used for higher-order address bits or data transfer control signals.

Group B is used for lower-order address bits or additional data lines.

Handshake signals ensure synchronized data transfer between the microprocessor and external devices.



Vidyavardhini's College of Engineering & Technology

Department of Artificial Intelligence and Data Science (AI&DS)

2. Explain the format of control word of 8255 PIC

Ans. The control word of the 8255 Programmable Peripheral Interface (PPI) is a 8-bit value that is used to configure the operating mode and various features of the chip. The format of the control word varies depending on the mode of operation selected. Let's break down the format of the control word for each mode:

Mode 0 - Basic Input/Output (I/O):

For Mode 0, the control word consists of 8 bits.

Bit 7 (MSB): Always set to 1 to indicate that Mode 0 is selected.

Bits 6-4: Configuration bits for Port C.

Bit 6: 1 for PC7-PC4 as inputs, 0 for PC7-PC4 as outputs.

Bit 5: 1 for PC3-PC0 as inputs, 0 for PC3-PC0 as outputs.

Bit 4: 1 to enable PC7-PC4 as inputs with internal pull-up resistors, 0 to disable.

Bits 3-0: Not used, typically set to 0.

Mode 1 - Strobed Input/Output:

For Mode 1, the control word consists of 8 bits.

Bit 7 (MSB): Always set to 1 to indicate that Mode 1 is selected.

Bits 6-4: Configuration bits for Port C.

Bit 6: 1 for PC7-PC4 as inputs, 0 for PC7-PC4 as outputs.

Bit 5: 1 for PC3-PC0 as inputs, 0 for PC3-PC0 as outputs.

Bit 4: 1 to enable PC7-PC4 as inputs with internal pull-up resistors, 0 to disable.

Bits 3-0: Not used, typically set to 0.

Mode 2 - Bidirectional Bus I/O:

For Mode 2, the control word consists of 8 bits.

Bit 7 (MSB): Always set to 1 to indicate that Mode 2 is selected.

Bit 6: Not used, typically set to 0.

Bit 5: 1 to enable Port B as an input, 0 for output.

Bit 4: 1 to enable Port A as an input, 0 for output.

Bits 3-0: Not used, typically set to 0.